http://dustbunny.physics.indiana.edu/~paul/hallDrd

GlueX (Jefferson Lab Hall D) Electronics R&D

Indiana University Light Quark Physics Group

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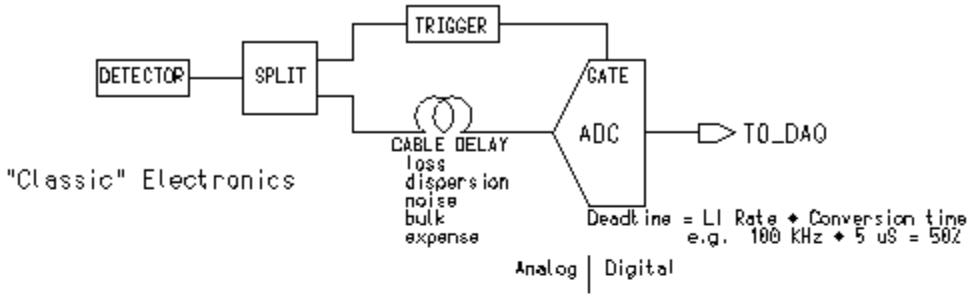
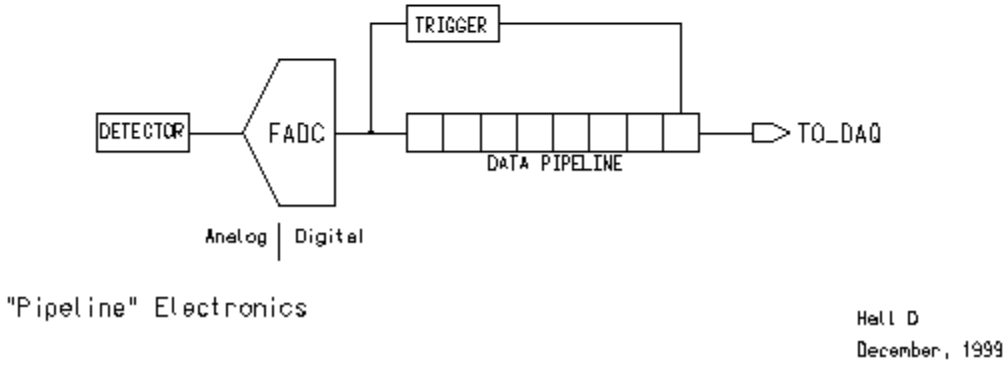
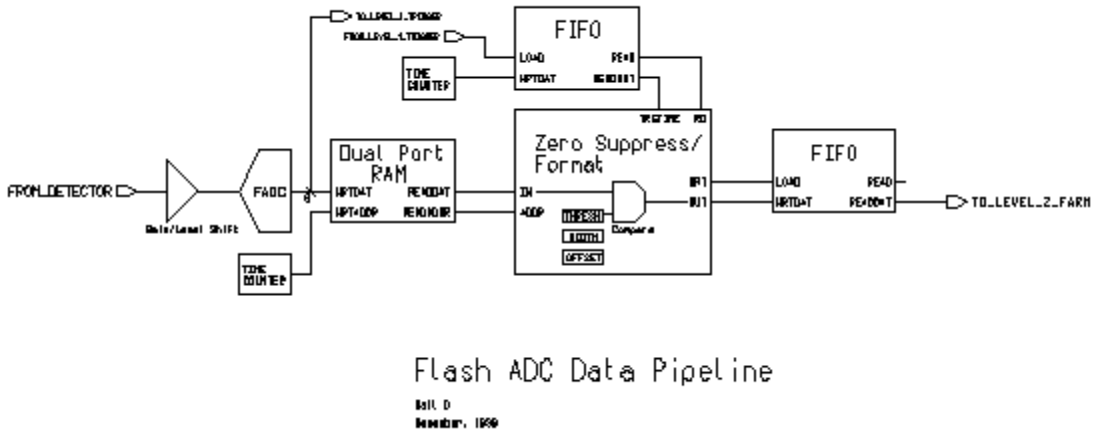
For the Jefferson lab GlueX experiment, we will be developing pipelined Flash ADC front end electronics. Traditionally, particle physics experiments delay detector signals in long coaxial cables to allow time for a trigger to be formed:





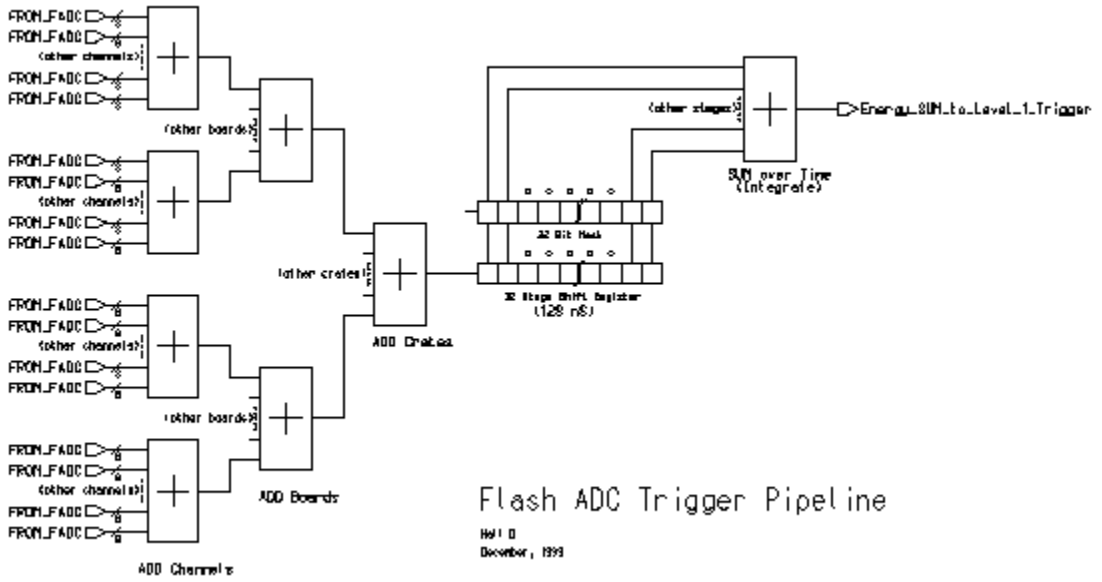
The pipeline approach continuously digitizes the detector data and stores the digital information. In parallel, the trigger uses the digital information to find interesting events. When the trigger condition is satisfied, time-delayed information is extracted from the pipeline for further processing by the data acquisition system.

The pipeline can be implemented with Dual Port Random Acess Memory:



The FADC data is continuously written into the Dual Port RAM. Upon receipt of a level 1 trigger, the data from the associated time slice is read from the other port. This scheme introduces no deadtime since new data continue to be written while the old data is read.

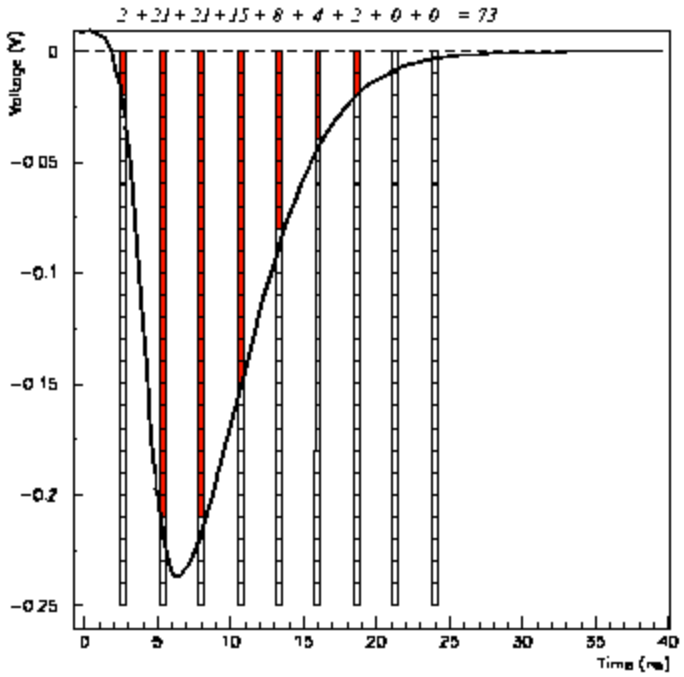
The FADC data is also used to form the level 1 trigger. A tree of adders sums information from the various channels in a detector system:



Within the next few years, this hardware will be prototyped at IU. Since the Hall D detector will require 10,000+ channels of this electronics, optimizing the cost is extremely important.

Flash ADCs are specified in terms of samples per second and number of bits of resolution. The individual samples can be added together to calculate the charge contained in a pulse:

Pulse Digitization



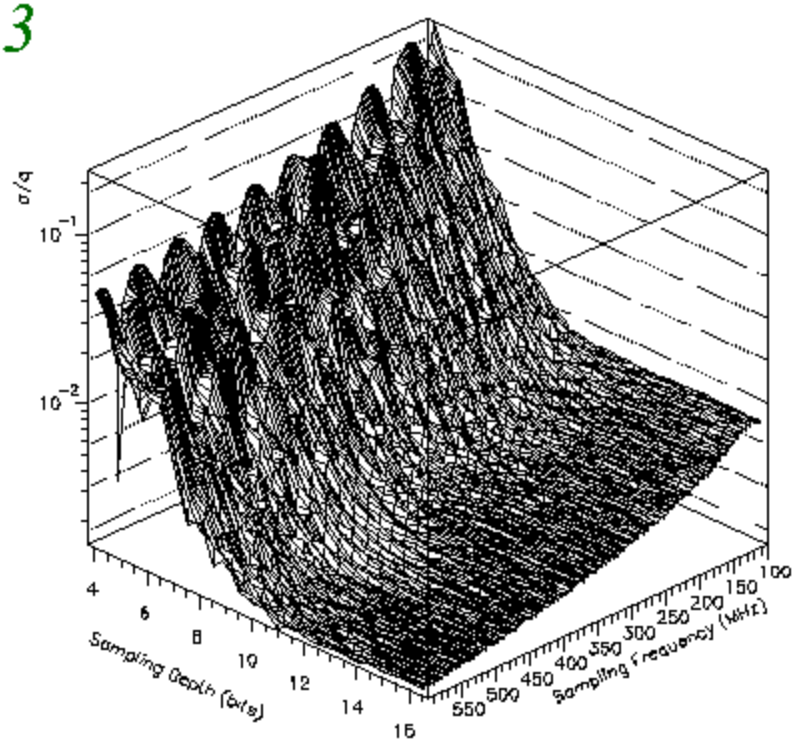
Our goal is to optimize the resolution at which the pulses are digitized by varying the sampling frequency and the sampling depth.

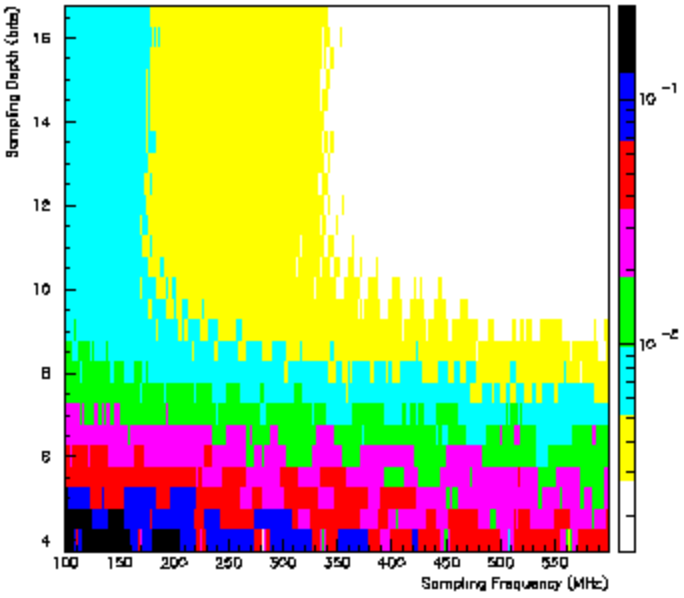
The sampling depth is related to the smallest voltage change to which the device is sensitive. A depth of n bits will provide 2^n divisions on the voltage scale

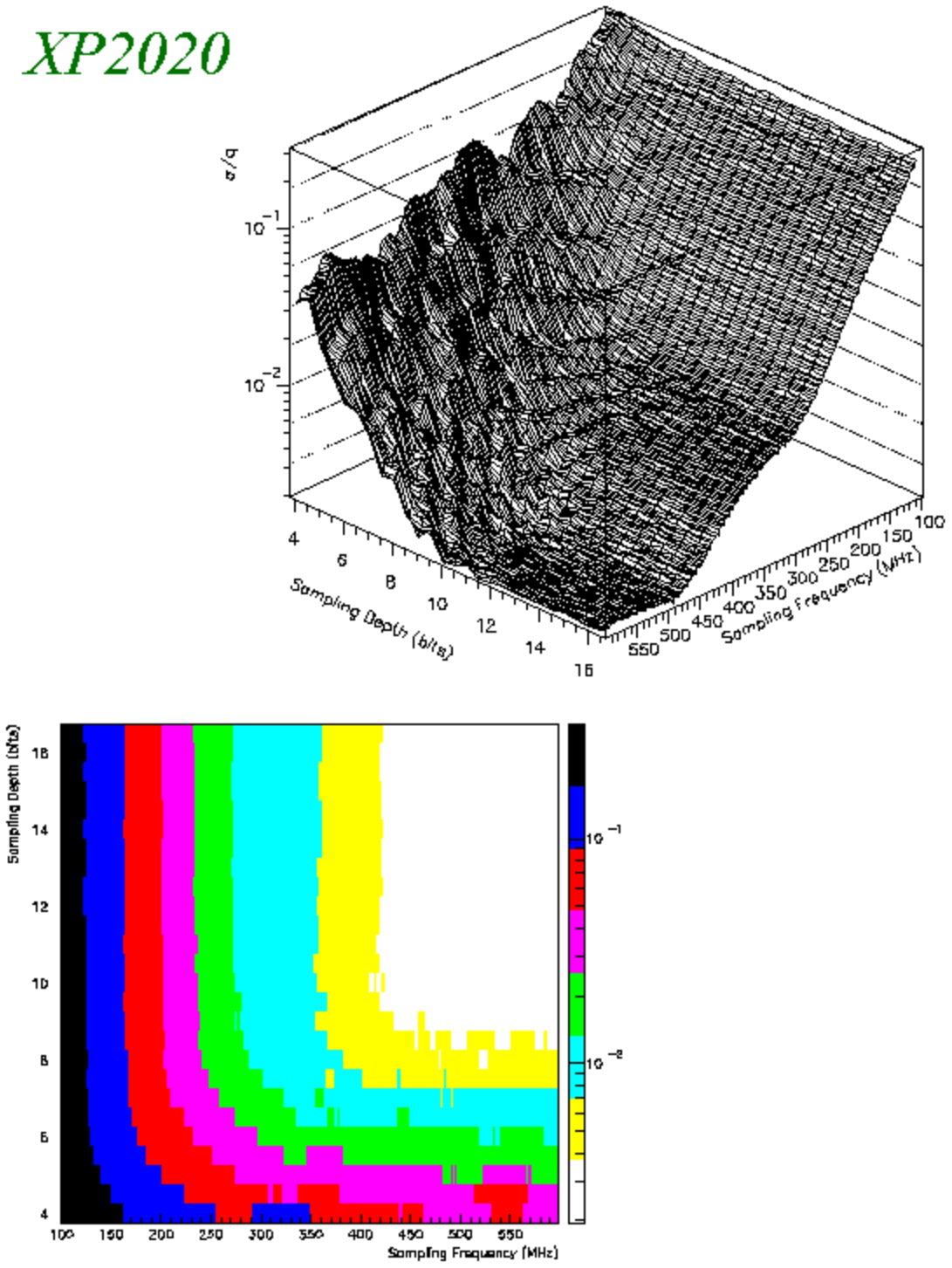
The sampling frequency is the rate at which the pulse is sampled. For shorter pulses higher frequencies are necessary.

We varied the sampling rate and bit depth for simulated pulses from a slow photomultiplier (FEU84) and a fast photomultiplier (XP2020). The variance in the charge measurement divided by the measured charge is plotted:

FEU 84-3

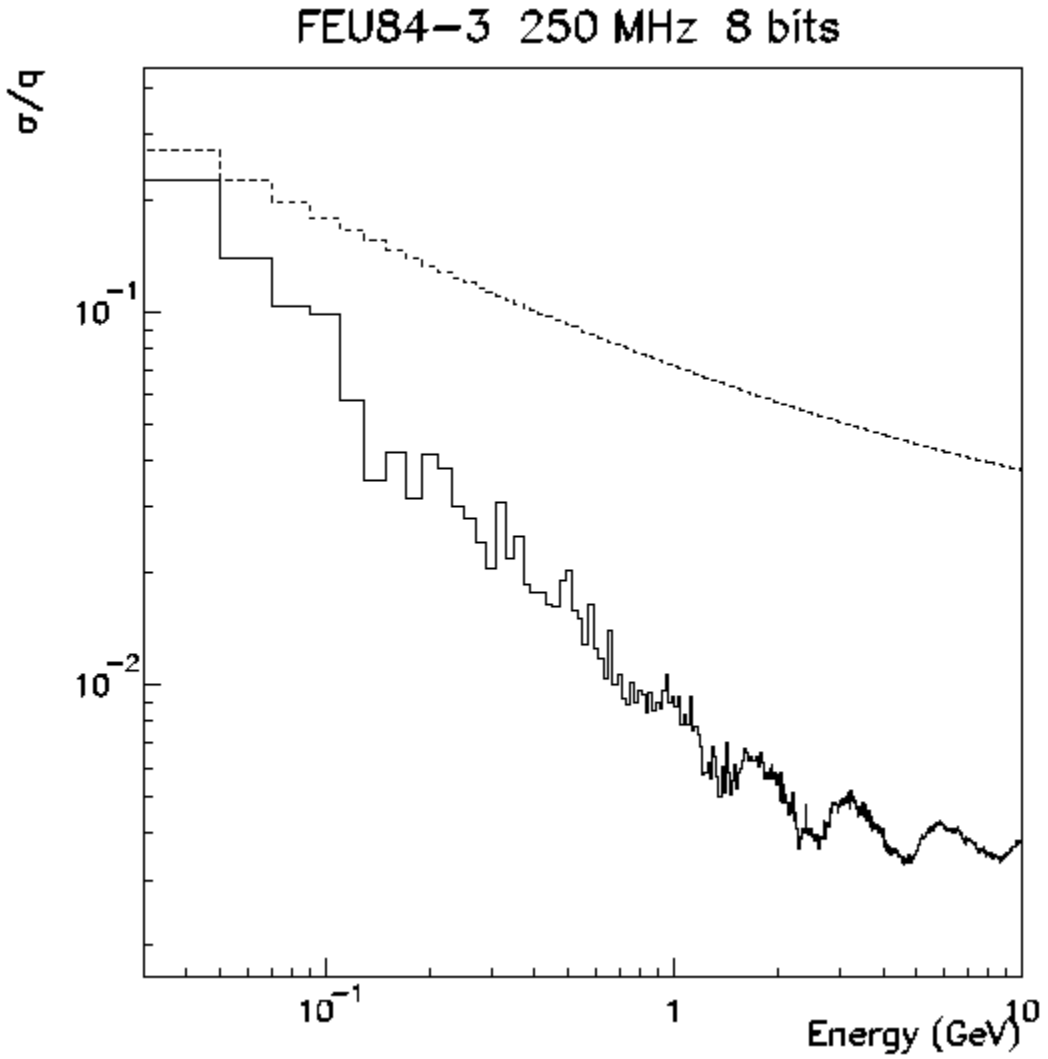

σ/q
10^{-1}
10^{-2}
4
6
8
10
12
14
16
Sampling Depth (bits)
100
150
200
250
300
350
400
450
500
550
Sampling Frequency (MHz)


Sampling Depth (bits)
16
14
12
10
8
6
4
100
150
200
250
300
350
400
450
500
550
Sampling Frequency (MHz)
10^{-1}
10^{-2}

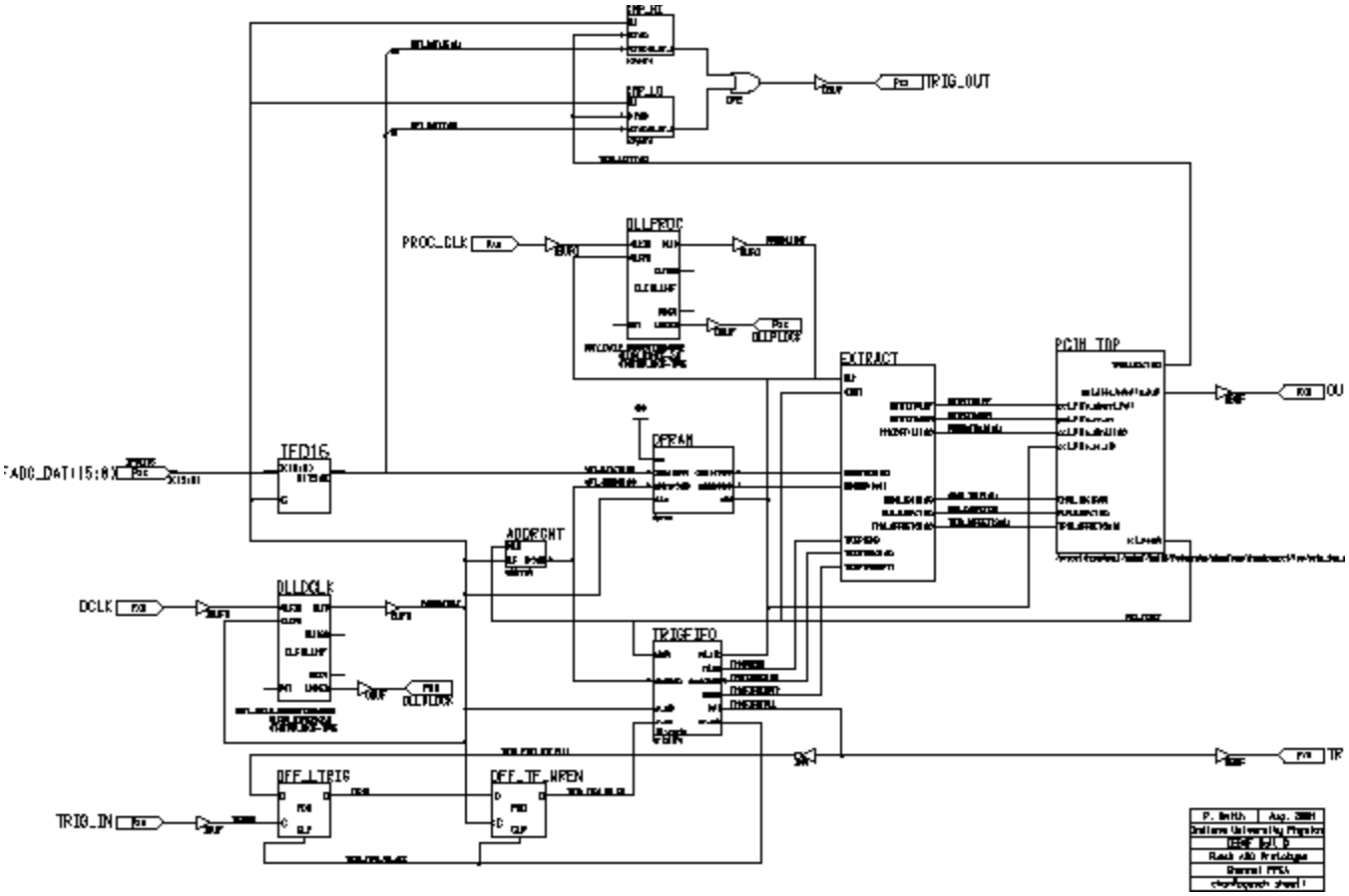


For the FEU84-3, summing the FADC samples results in an energy resolution better than the intrinsic

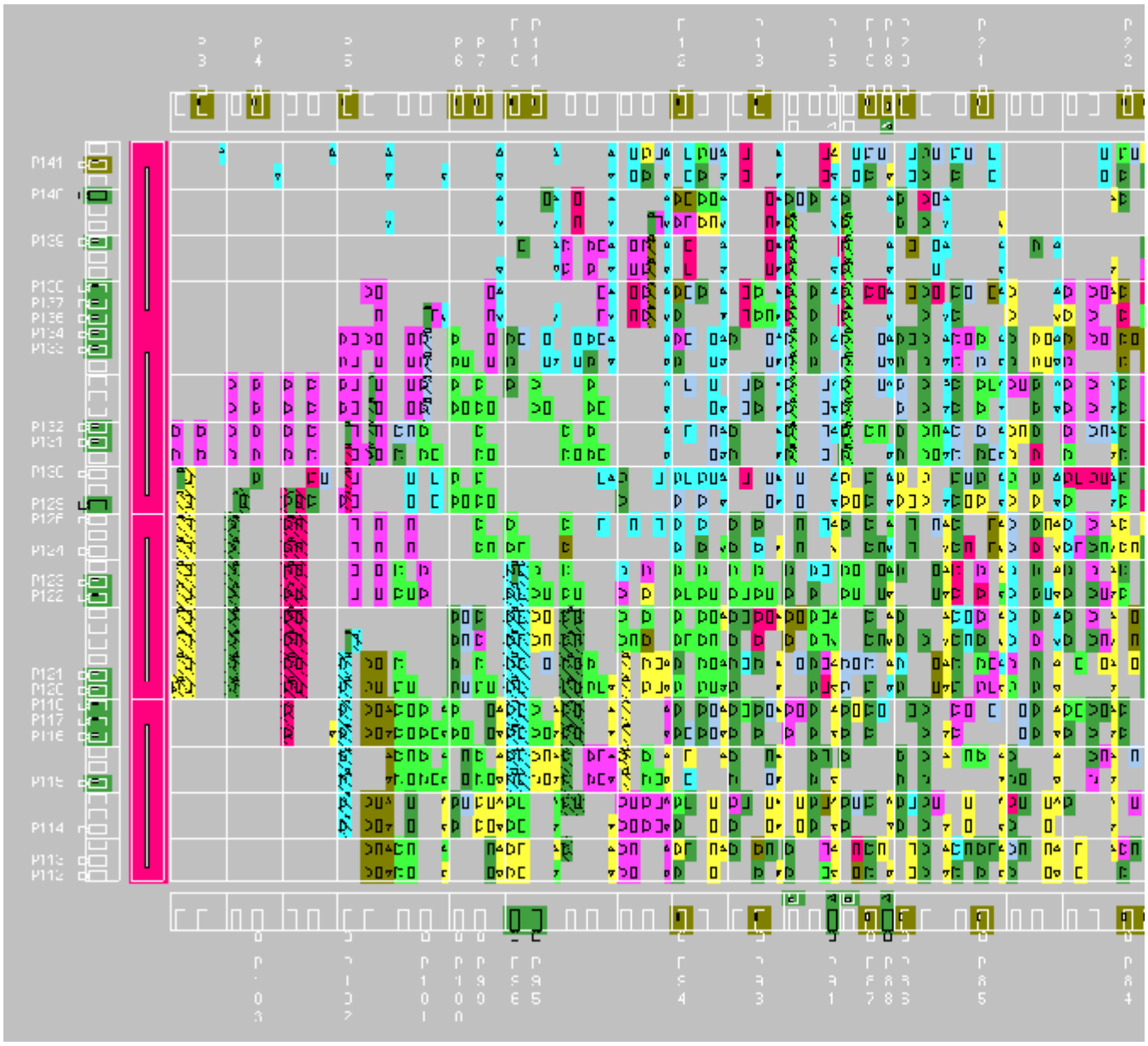
resolution of lead glass:



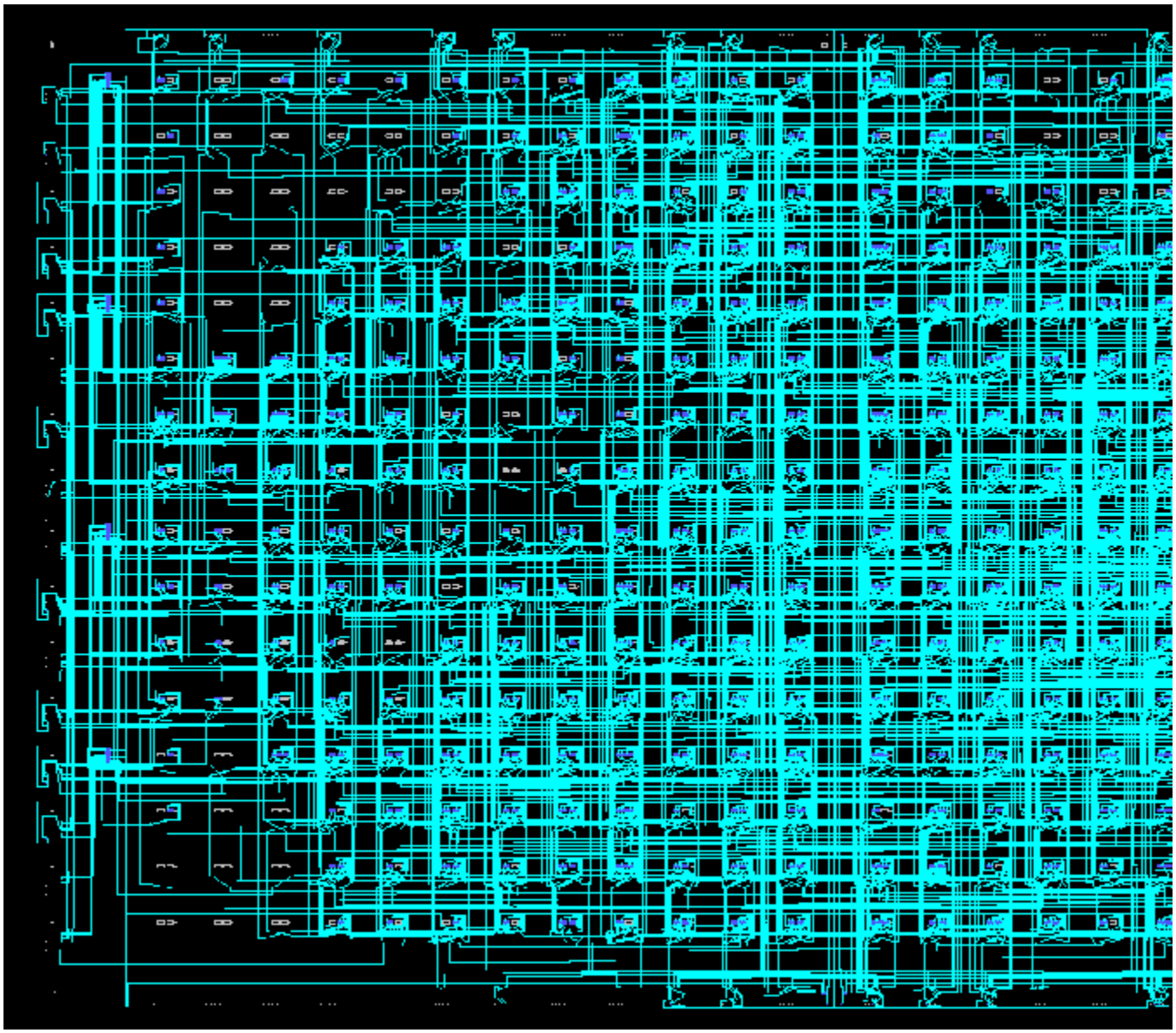
A Xilinx XC2S50 gate array which implements the dual port RAM buffering, feature extraction, and an interface to the PCI bus has been designed and simulated. Here is a block diagram:



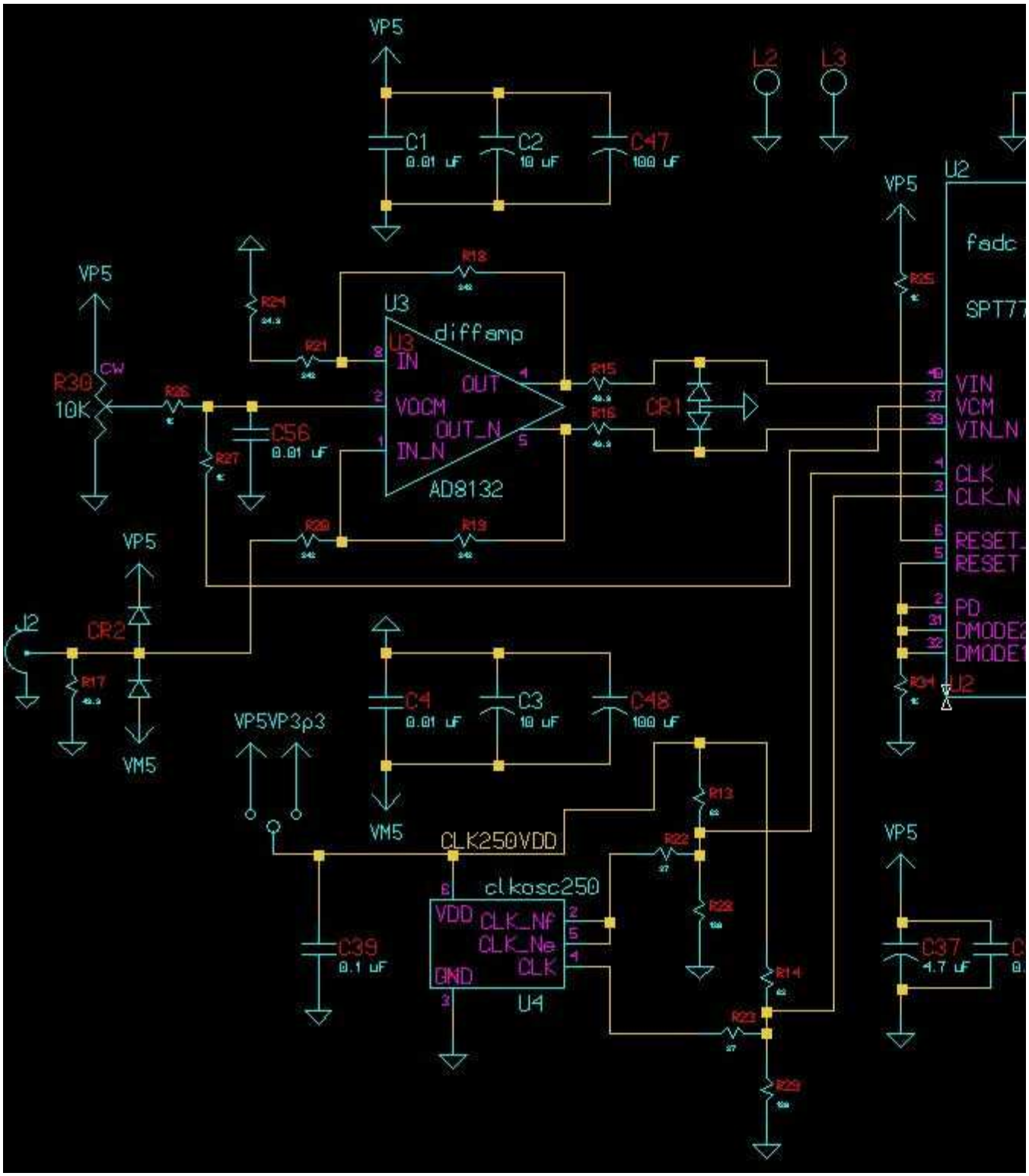
Here is a "floorplan" of the gate array:

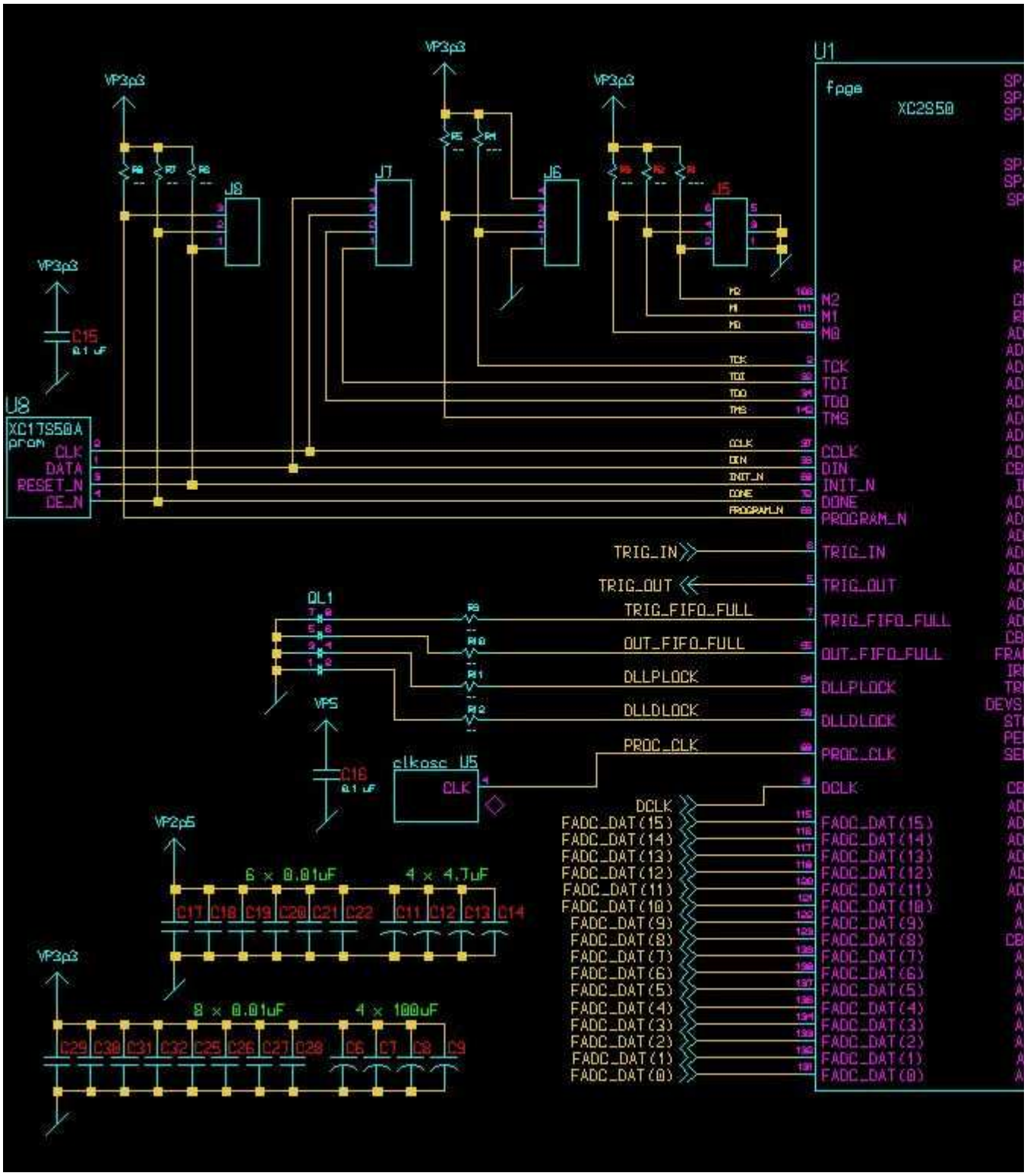


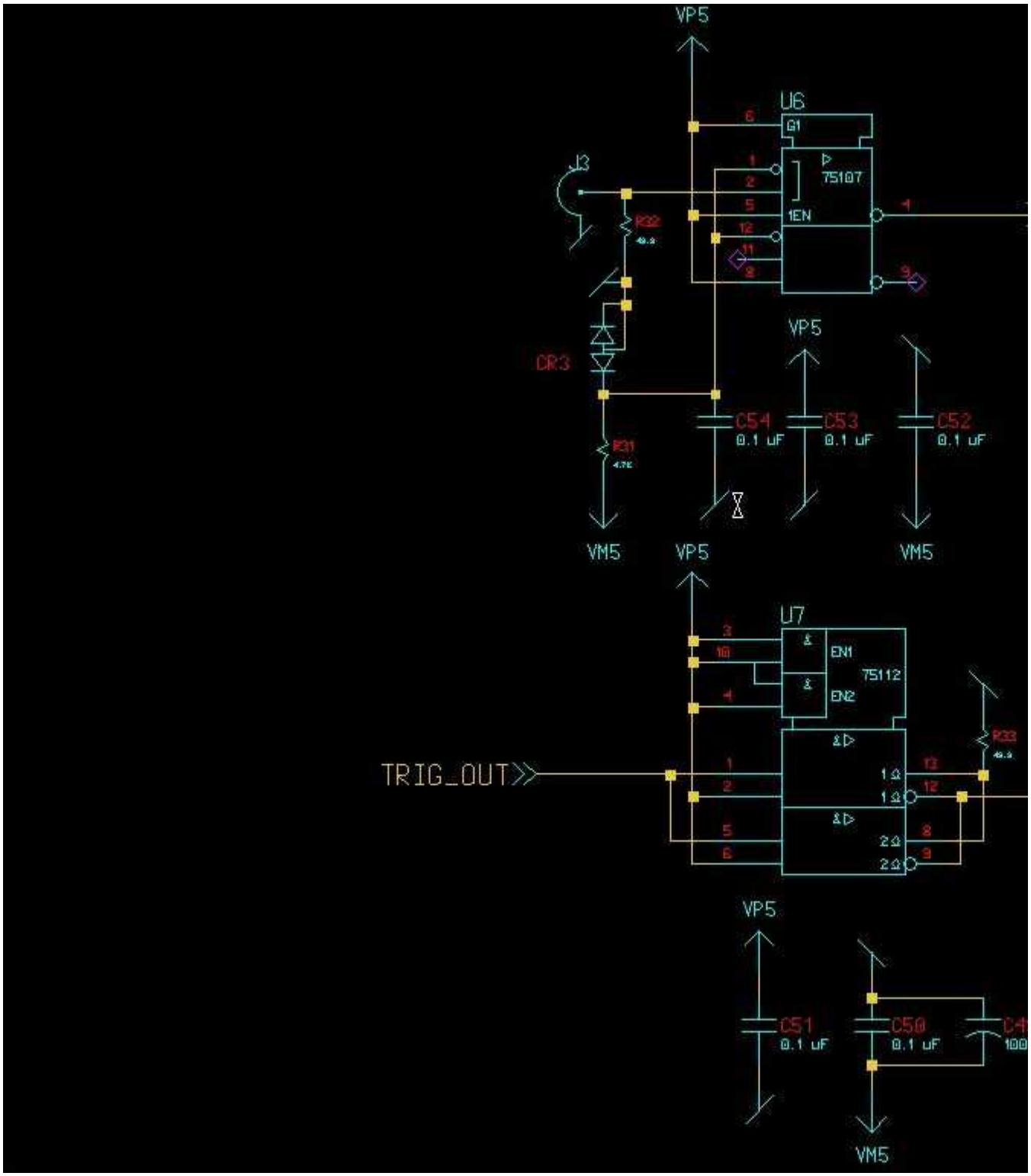
Here is the routing for the gate array:

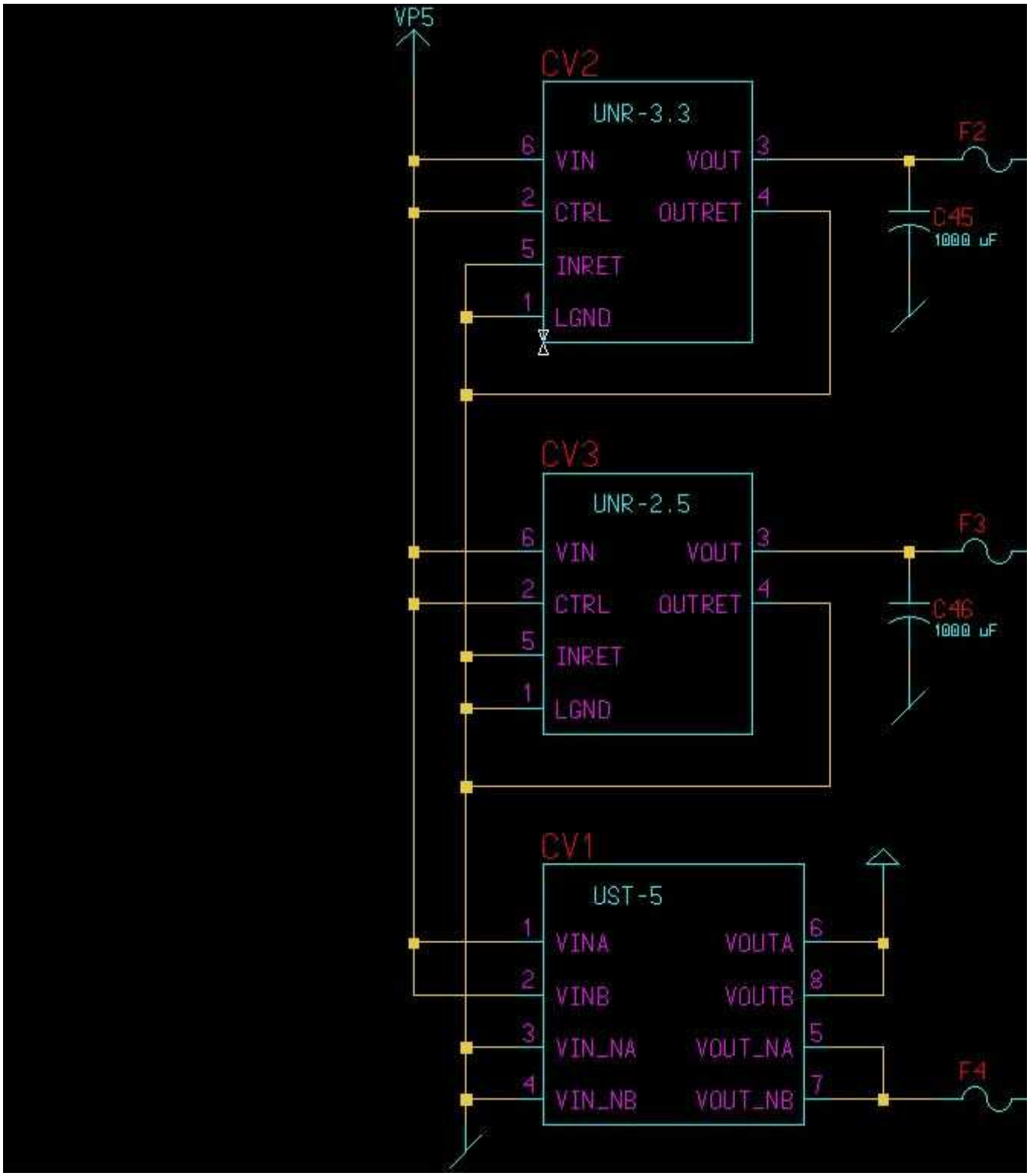


Here are schematics of a PCI card to test the FADC and Xilinx gate array:

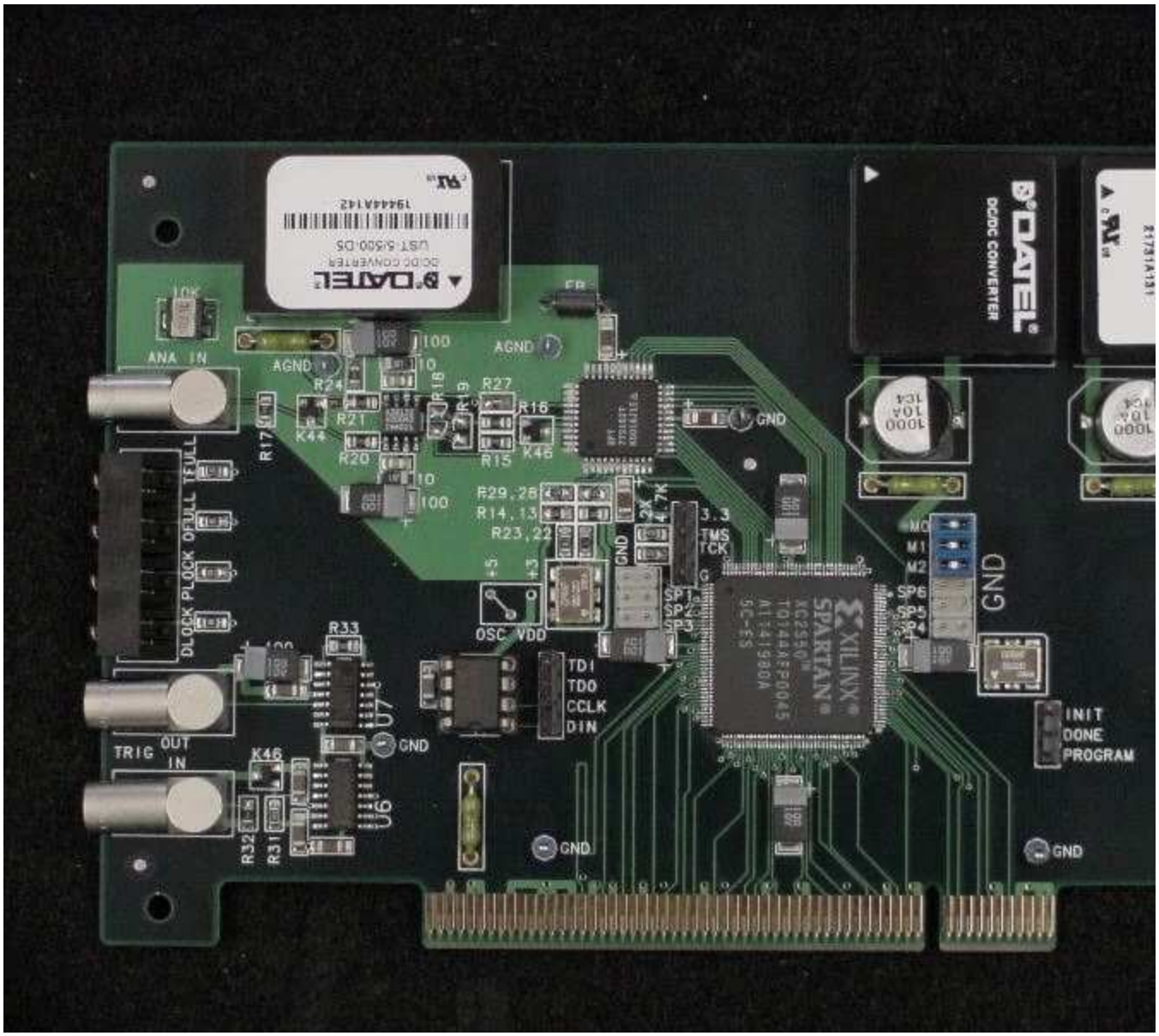

VP5
C1
0.01 uF
C2
10 uF
C47
100 uF
L2
L3
U2
VP5
fadc
SPT77
VP5
R30
10K
CW
R26
R27
C56
0.01 uF
R24
R21
R18
U3
diffamp
U3
IN
OUT
VOCM
OUT_N
IN_N
AD8132
R15
R16
CR1
R25
VIN
VCM
VIN_N
CLK
CLK_N
RESET_
RESET
PD
DMODE2
DMODE1
R34
U2
R20
R19
VP5
J2
CR2
R17
VM5
C4
0.01 uF
C3
10 uF
C48
100 uF
VP5VP3p3
VM5
CLK250VDD
clkosc250
VDD
CLK_Nf
CLK_Ne
CLK
GND
U4
C39
0.1 uF
R13
R22
R28
R14
R23
R29
VP5
C37
4.7 uF

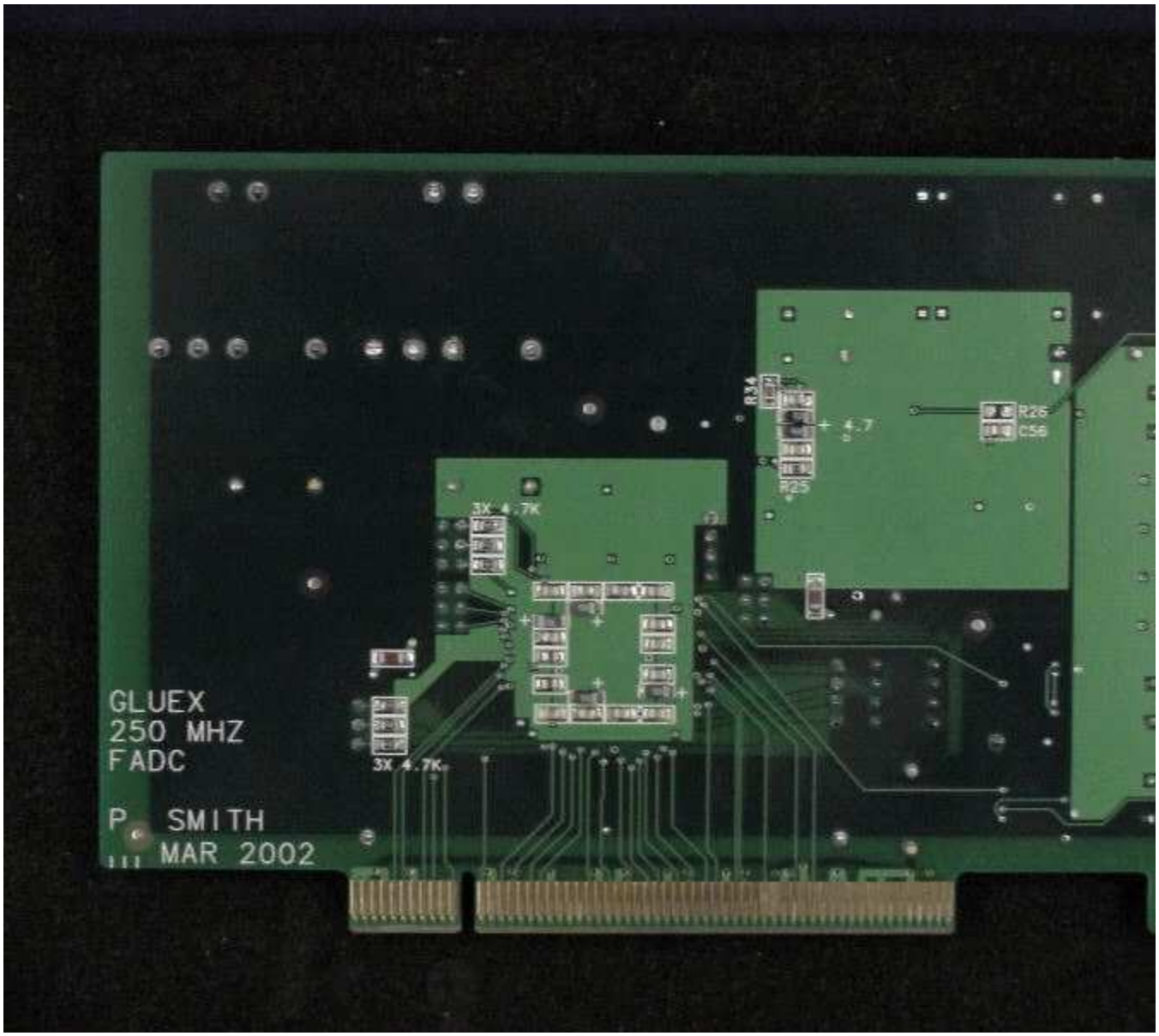

U1
fpga
XC2S50
VP3p3
J8
J7
J6
J5
C15
0.1 uF
U8
XC17S50A
prom
CLK
DATA
RESET_N
OE_N
M2
M1
M0
TCK
TDI
TDO
TMS
CCLK
DIN
INIT_N
DONE
PROGRAM_N
TRIG_IN
TRIG_OUT
TRIG_FIFO_FULL
OUT_FIFO_FULL
DLLPLOCK
DLLDLOCK
PROC_CLK
DCLK
FADC_DAT(15)
FADC_DAT(14)
FADC_DAT(13)
FADC_DAT(12)
FADC_DAT(11)
FADC_DAT(10)
FADC_DAT(9)
FADC_DAT(8)
FADC_DAT(7)
FADC_DAT(6)
FADC_DAT(5)
FADC_DAT(4)
FADC_DAT(3)
FADC_DAT(2)
FADC_DAT(1)
FADC_DAT(0)
QL1
VP5
C16
0.1 uF
clkosc U5
CLK
VP2p5
6 x 0.01uF
4 x 4.7uF
C17 C18 C19 C20 C21 C22 C11 C12 C13 C14
8 x 0.01uF
4 x 100uF
C29 C30 C31 C32 C25 C26 C27 C28 C6 C7 C8 C9


VP5
U6
75107
1EN
J3
R32
CR3
C54
0.1 uF
C53
0.1 uF
C52
0.1 uF
R31
VM5
VP5
VM5
U7
EN1
75112
EN2
TRIG_OUT
R33
VP5
C51
0.1 uF
C50
0.1 uF
VM5



Here is the printed circuit:


DATEL
DC/DC CONVERTER
ANA IN
AGND
R24
R21
R20
R17
K44
R18
R19
R27
R16
R15
K46
R29,28
R14,13
R23,22
GND
3.3
TMS
TCK
SP1
SP2
SP3
OSC VDD
TDI
TDO
CCLK
DIN
XILINX
SPARTAN
M0
M1
M2
SP6
SP5
SP4
INIT
DONE
PROGRAM
R33
U7
U6
TRIG
OUT
IN
K46
R32
R31
DLOCK PLOCK OFULL TFULL



Higher resolution and printable versions of the figures are available here.
Sample waveforms are available here.
Register assignments and programming information is available here.
Linux driver software is available here.
More information about the GlueX experiment is available here.