Hall D Trigger

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Hall D Collaboration Meeting

Outline

- The Challenge
- Level 1
- Level 3

Hall D - The Numbers

According to Design Report (Table 4.7 - 9 Gev)

- Tagged Photon Rate 300 MHz
- Total Hadronic Rate 365 KHz
- Tagged Hadronic Rate 14 KHz

Conclusions:

- Trigger needs better than 25-1 rejection
- “Tag event” is nearly useless in trigger

Hall D – The Triggering Challenge

Factor of 25 is tough

- Requires essentially "full reconstruction" to separate on photon energy!!
- Hard to design hardware "up-front" to do this
- Hard to do it in 1 pass
- Hard to do it fast

Conclusion

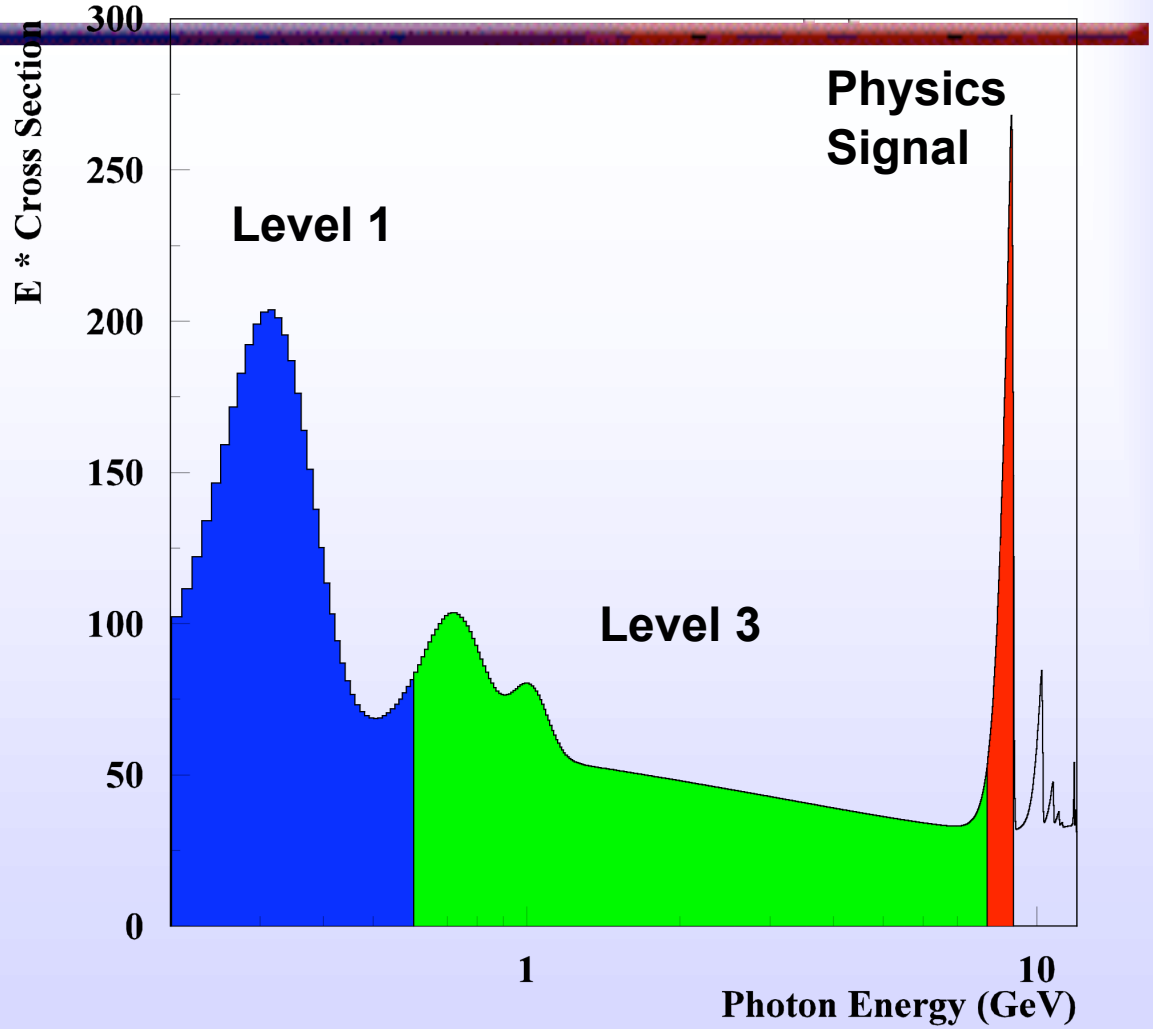
- Do it in 2 stages - 1 hardware 1 software

Photon Rates

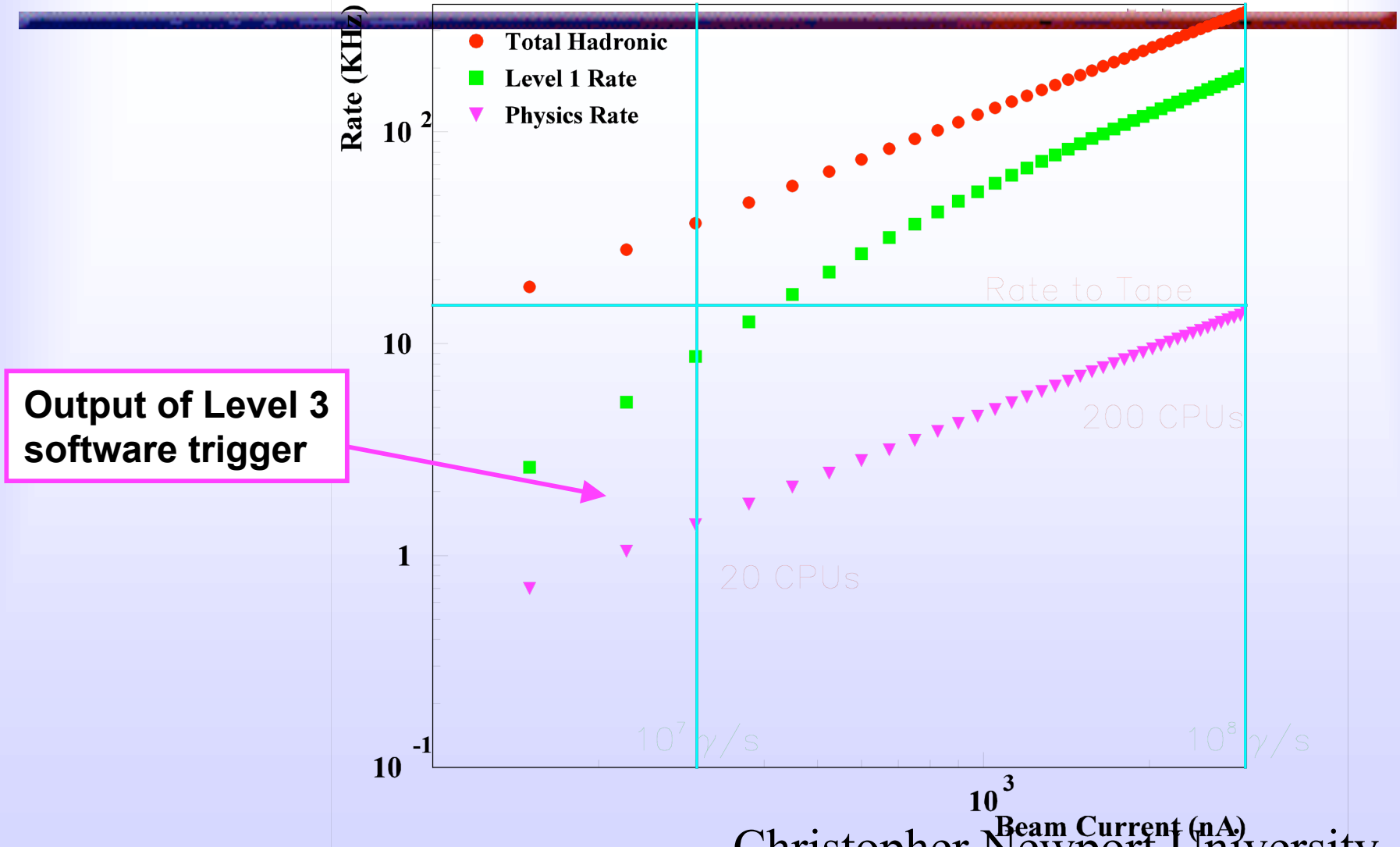
Start @ 10^7 γ/s
Open and unbiased trigger
Design for 10^8 γ/s
15 KHz events to tape

Level 1 trigger system
With pipeline electronics

Software-based
Level 3 System



Trigger Rates



Output of Level 3 software trigger

L1 Trigger – Why is it Hard?

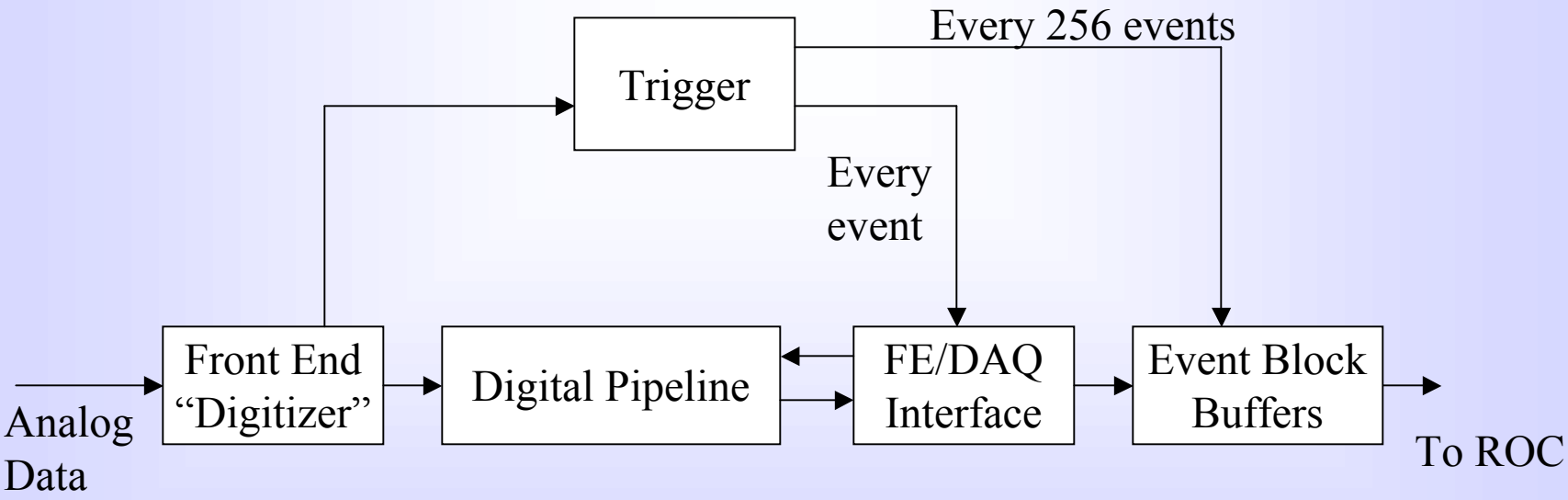
- Lots of low energy photons with high cross sections
- At high tag rates, tagger doesn't help
- Many final states are interesting
  - Some are mostly charged particles
  - Some are mostly neutral particles
  - $\gamma\, p \rightarrow X(1600)\, n \rightarrow \rho^0\, \pi^+\, n \rightarrow n\, \pi^+\, \pi^-\, \pi^+$
  - $\gamma\, p \rightarrow X(1600)\, n \rightarrow Eta^0\, \pi^+\, n \rightarrow n\, \pi^+\, \gamma\, \gamma$
  - $\gamma\, p \rightarrow X(1600)\, \Delta^0 \rightarrow \pi^+\, \pi^-\, \pi^+\, n\, \pi^0 \rightarrow \pi^+\, \pi^-\, \pi^+\, n\, \gamma\, \gamma$
  - $\gamma\, p \rightarrow \rho^0\, p \rightarrow \pi+\, \pi^-\, p$

L1 Trigger – What would you like?

- Cut events with E_γ < 2-5 GeV
  - Some function of available params (energies, tracks)
  - Minimum/Maximum/Exact number of tracks in:
    - Start Counter
    - Forward TOF
  - Minimum or Maximum for energy in:
    - Barrel Calorimeter
    - Forward Calorimeter
  - Complex function which incorporates all of these
- Time window for matches
- Output delay from trigger/timestamp match

Level 1 Trigger and DAQ

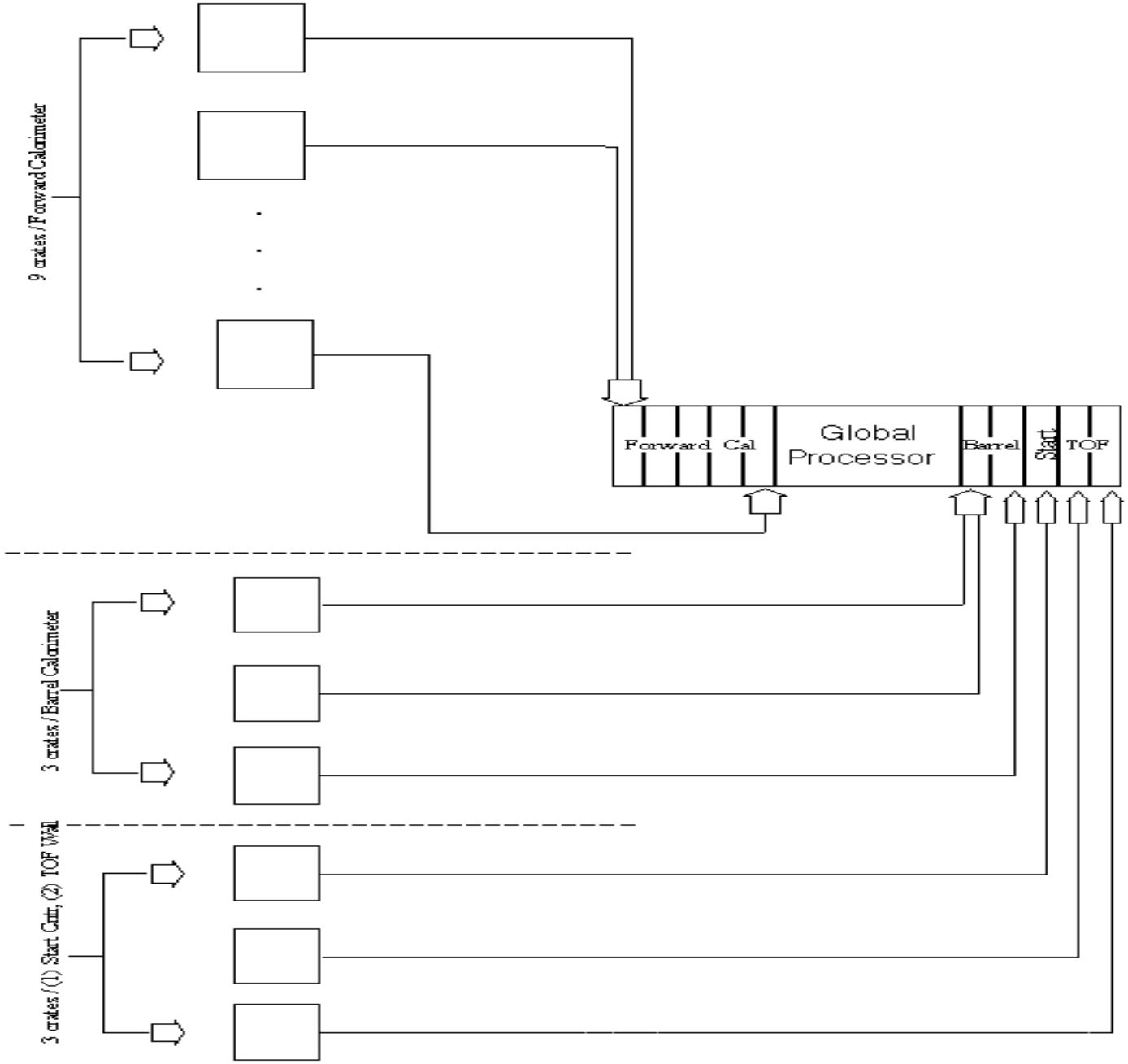
- Front ends fully pipelined
- Trigger "spies" on data and is also pipelined
- Trigger causes "event extraction" from pipeline



L1 Trigger – Current plans

- Four separate subsystems
  - Start Counter - compute number of tracks
  - Forward TOF - compute number of tracks
  - Barrel Calorimeter - compute energy
  - Forward Calorimeter - compute energy
- Each subsystem computes continuously
  - Goal - At speed of the FADC pipelines - 250 MHz (hard)
- Global Trigger Processor "combines" all four subsystems
  - 4 level hierarchy: Board -> Crate -> Subsystem -> Global

Gluex Energy Trigger - III



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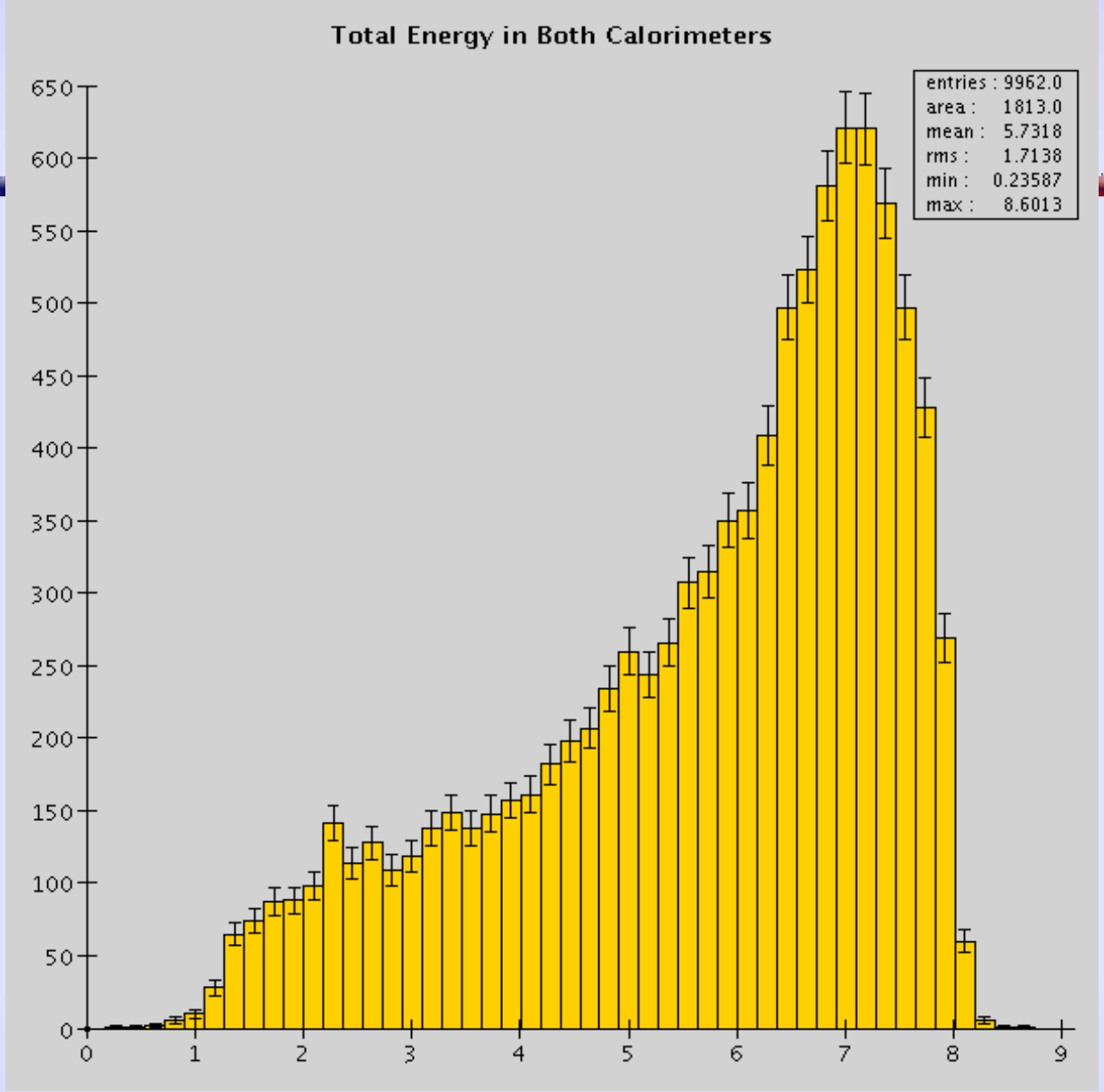
Timing

– Flight/Detector Time	32 ns
– PMT latency	32 ns
– Cables to FEE	32 ns
– FEE to trigger out	64 ns
– Crate sum	64 ns
– Link to subsystem	128 ns
– Subsystem trigger processing	256 ns
– Transfer SER to GTP (64 bits)	256 ns
– GTP	512 ns
– Level 1 output to FEE	128 ns

TOTAL = 1.504 μS - design FEE for 3 μs (~768 stage)!

James Hubbard's "Proof of Concept"

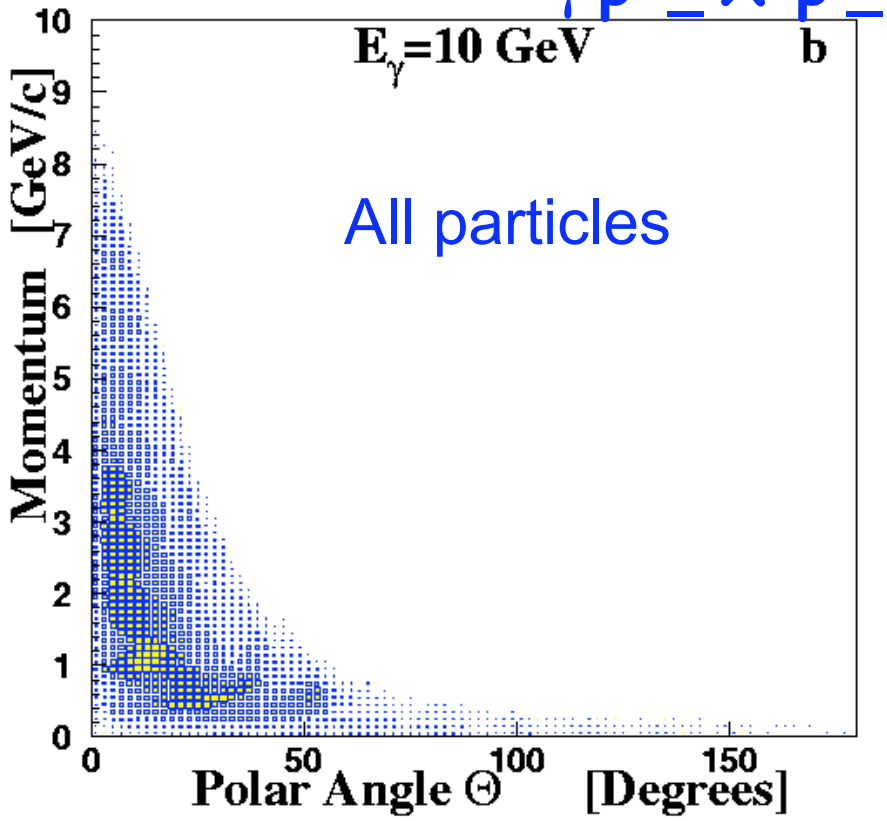
- Genr8 – create events
- HDGeant – simulate events
- hddm-xml – convert output to XML
- JAXB – create Java objects for XML description
- JAS – for analysis
- Function Optimization – for GLUEX

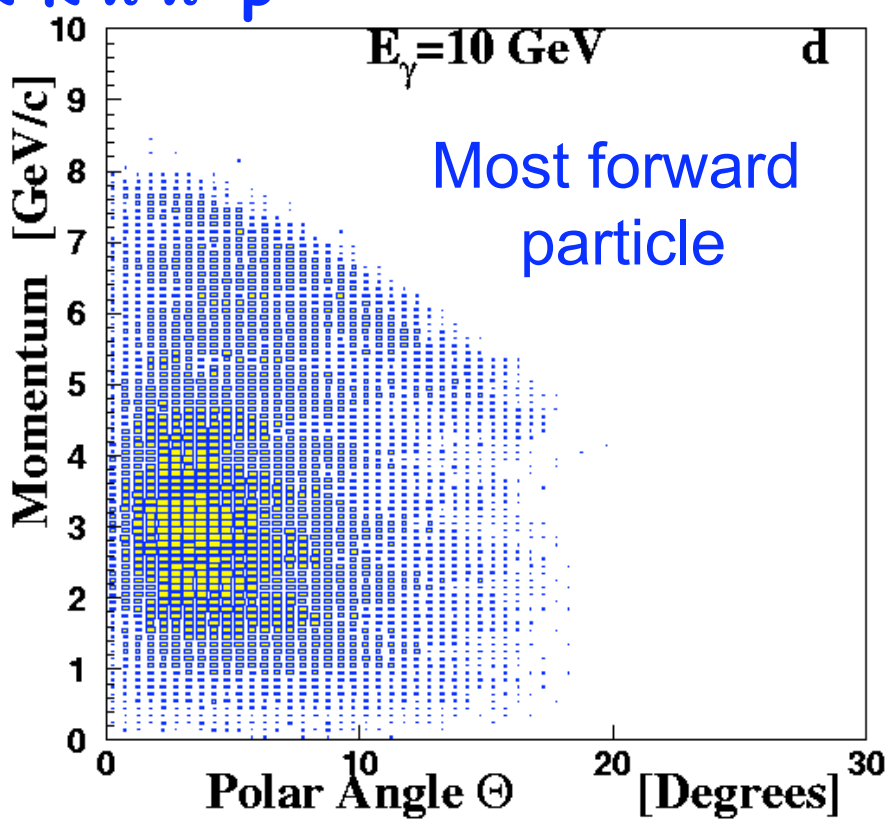


Christopher Newport University

Particle Kinematics

$\gamma p \_ X p \_ K^+K^-\pi^+\pi^- p$





Reactions

- 12 datasets (~120,000 events)
  - 4 Reactions simulated at 9 GeV
    - γ p -> X(1600) n -> ρ^0 π^+ n-> n π^+ π^- π^+
    - γ p -> X(1600) n -> Eta^0 π^+ n -> n π^+ γ γ
    - γ p -> X(1600) Δ^0 -> π^+ π^- π^+ n π^0 -> π^+ π^- π^+ n γ γ
    - γ p -> ρ^0 p -> π+ π^- p
  - 3 of 4 are simulated at 1 and 2 GeV
  - 2 Background Delta Reactions

    γp -> n π^+

    γp -> p π^0

Event Characteristics

- High Energy (9 GeV) Events
  - More energy overall
  - Greater fraction of energy in the forward direction
  - Greater track counts in forward detectors
- Background (1-2 GeV) Events
  - Less energy overall
  - More energy in radial direction
  - Track counts larger in side detectors

Conditional Trigger

- Fairly successful formula:
  - If Energy in Forward Cal < .5 GeV and Tracks in Forward TOF = 0

  Or

  - If Total Energy < .5 GeV and Forward Cal Energy < Barrel Cal Energy

  Cut

Conditional Trigger Results

- Eval Score 0.786

REACTION	TOTAL	CUT	NOT CUT	%CUT
n3pi_2gev	10000	3088	6912	30.88
n3pi_1gev	10000	4507	5493	45.07
pro2pi_2gev	10000	4718	5282	47.18
pro2pi_1gev	10000	6106	3894	61.06
e2gamma_1gev	10000	4229	5771	42.29
e2gamma_2gev	10000	5389	4611	53.89
delta_npi+	10000	8199	1801	81.99
delta_ppi0	10000	9773	227	97.73
n3pi_9gev	9851	25	9826	0.25
e2gamma_9gev	9962	4	9958	0.04
pro2pi_9gev	9942	30	9912	0.30
xdelta_9gev	10000	50	9950	0.50

Functional Form

- Z >= TFM*TTOF + EFM*EFCal + RM*((EFCal +1)/(EBCal + 1))
  - TTOF - Tracks Forward TOF
  - EFCal - Energy Forward Calorimeter
  - EBCal - Energy Barrel Calorimeter
- How do we decide what values to assign the coefficients and Z?
  - Use a Genetic Algorithm (GA)
- Driving the GA
  - if Background Event and is Cut +1
  - if Good Event and isn't Cut +5
  - if Good Event and is Cut –50
  - if Total number Good Events Cut > 50, reset

Results

- The methodology works for simulated events
  - Good Events:
    - Cuts less than 0.5%
  - Background Events:
    - Average Cut: 72 %
    - Range: 41% to 99.99%
  - Varying hadronic energy deposition doesn't change results
    - Tested with +- 20%

A Note on the Start Counter

- The start counter was never dropped from the trigger.
- James' conclusion: It may not be super useful
- No reason to give up that data if available
- "Latest" design is relatively easy to use
  - (but theta segmentation would have been cool …sigh!)

From the Electronics Review

- "Concept of local sums at front-end board level, followed by crate-level sums, and subsequent transfer to a central Gobal LVL-1 processing area, is sound."
- "The link work shown should be completed"
- "Concept and proof-of-principle for crate backplane operation at the required high rate needs to be developed for the CDR"
- "Global design for the LVL-1 needs to be developed for the CDR"

Gluex Energy Trigger – Moving Data

- Assume 250 MHz 8 bit flash ADC
  - Assume 16 (?!) Flash ADC channels/board
  - Assume 16 boards/crate -> 256 channels/crate
  - 576 channels in barrel calorimeter -> 3 crates
  - 2200 channels in forward cal -> 9 crates
- Energy addition in real time
  - 256 8 bit channels/crate -> 16 bit sum
    - If 256 12 bit channels/crate -> 20 bit sum
- Each crate must be capable of pumping 20 bits of data at 250 MHz or 625 MBytes/s

Trigger Computation on the FADC board

- 250 MHz 8 bit flash ADC
  - 16 Flash ADC channels/board
  - Each flash functions in “double pump” mode
    - 2 samples at 125 MHz
  - 16 x 16 = 256 bits into Trigger FPGA (on board)
  - Trigger FPGA clocks at 125 MHz
  - Two separate “adder trees”
  - 4 clocks (125 MHz) to complete the add
  - Two 12 bit results every 8 ns (3 Gbit/s)

Crate Summation

- 16 boards/crate
- Data sent to “crate summer”
  - Located in center slot
    - Reduces backplane load, complexity, timing skew
  - 8 x 2 x 12 = 192 bits into crate summer (from each side)
  - Total of 384 bits (at 125 MHz)
  - Difficult

Reduced Time Precision

- Take “average” of each pair of flash samples
- One 12 bit board sum every 8 ns (1.5 Gbit/s)
- Data sent to “crate summer”
  - Located in center
    - Reduces backplane load and complexity
  - 8 x 12 = 96 bits into crate summer (from each side)
  - Total of 192 bits at 125 MHz
  - Do-able

L1 Crate Prototype

- "A concept and proof-of-principle for crate backplane operation at the required high rate needs to be developed for the CDR."
- Topic 1 of CNU's upcoming NSF proposal

Backplane Option 1 – Parallel Data

- Use VME64x-9U style P5/P6 connectors
  - 2mm Hard Metric
  - Outer 2 rows grounded
  - 5 rows x (22 + 25) = 235 signals
- Can be added as separate backplane to VME64x (or Compact PCI) easily
- Can be developed and tested independently

Backplane Option 2 – Serial Data

- Convert Board Sum to serial data
- 12 bits @ 125 MHz -> 1.5 Gbps
- 2.5 Gbps (data rate = 2.0 Gbps)
- 3.125 Gbps (data rate = 2.5 Gbps)
- Will easily fit into 3U space
- Can be built and tested independently

Backplane Option 3 – Test Both

- Build 3U Test Crate
- Custom Backplane
  - Support parallel and serial data transport
- Build "L1 Data Source Modules"
  - Use Xilinx FPGA's
    - built in "Rocket-I/O"
  - Source data parallel (8 bits instead of 12) and serially
- Build "Prototype L1 Crate Summer"
- Test

Clock Distribution

- Need a 125 MHz clock everywhere
- Could use “submultiple” clock
- Local clocks need to be sync’d (i.e. agree on T0)
  - For timestamping to make sense
- All DAQ/Trigger elements are “clock aware”
- Ed Jastrzembski has taken this on

L1 Crate Summer

- Computes total energy in crate
- Tracks clock for timestamping
- Transfers data to “subsystem computer” via the “subsystem link”

Subsystem Link Features

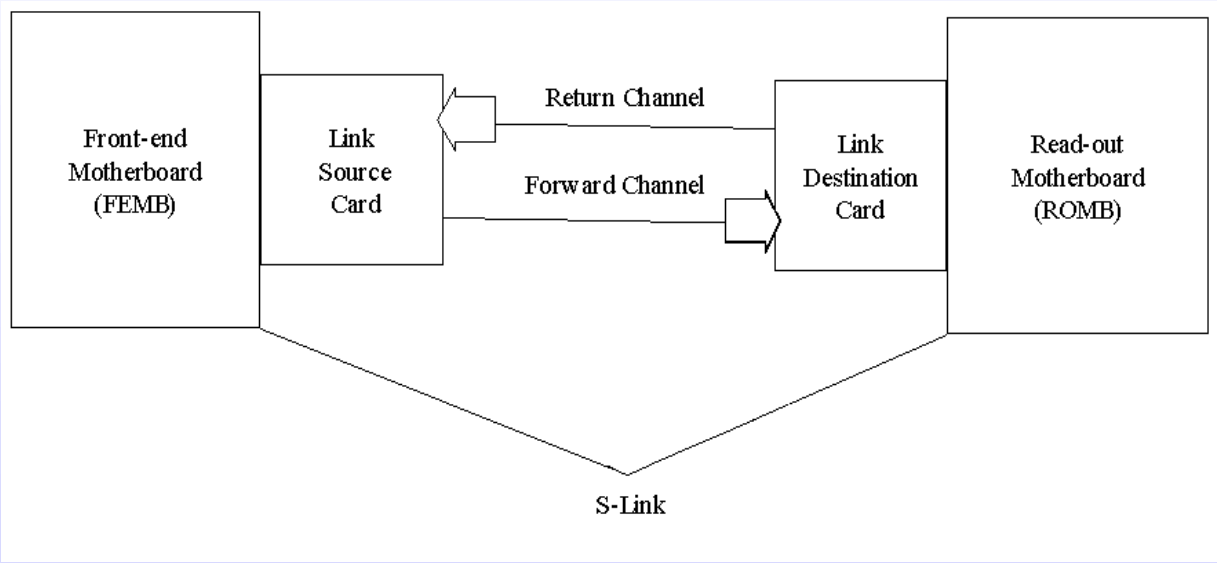
- High speed
  - With half-speed 8 bit option – 16 bits @ 125 MHz
    - 250 MByte/s = 2 Gbit/s data rate
  - With full speed 12 bit option – 20 bits @ 250 MHz
    - 625 MByte/sec = 5 Gbit/s
- Optical preferred
  - More flexibility in trigger location
  - No noise issues
- Easy-to-use interface
- "Daughter card" design might be good
  - Minimizes layout issues of high speed signals if a single, well tested, daughter card design is used.

Link Subtleties

- Would Like Error Correction
  - Classic "double detection-single correction"
    - Uses Hamming codes
    - Not suitable for fiber optic links – errors in bursts
  - Could use forward error correction with delay
  - Only adds a bit of latency – if you have bandwidth
- Timestamp embedded in data stream
- Skew adjustment at Subsystem Computer (using timestamp)

S-Link

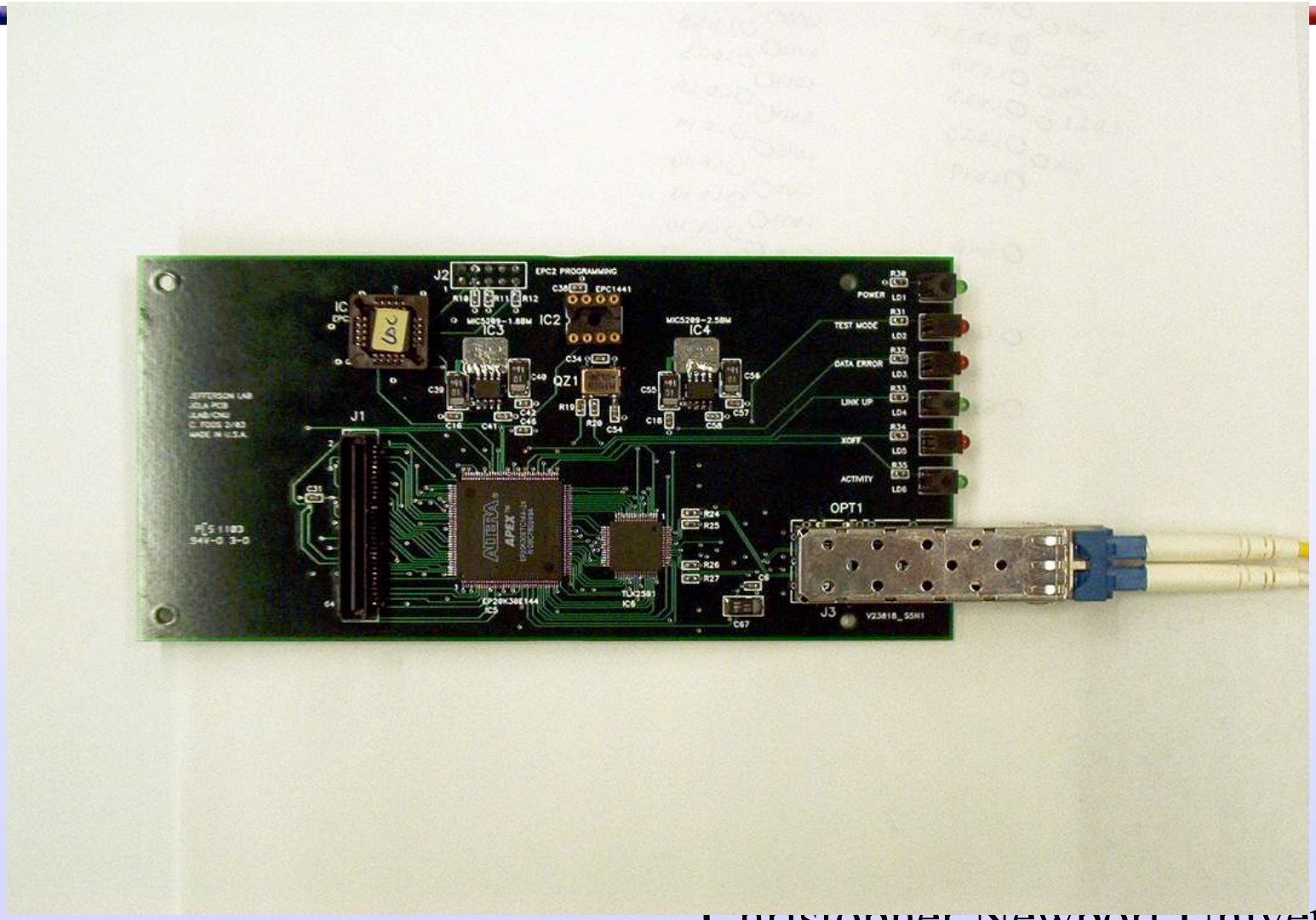
- An S-Link operates as a virtual ribbon cable, moving data from one point to another
- No medium specification (copper, fiber, etc.)
- 32 bits
- 40 MHz
- 160 Mbytes/s



HOLA at JLAB = JOLA

- Cern's HOLA Slink card – used in numerous places
  - Uses TI TLK2501 for higher speed serialization/deserialization
  - Data link clock is 125 MHz (@ 16 bits)
    - Data link speed is 250 MBytes/s
    - Actual throughput is limited by S-Link to 160 MBytes/s
- Obtain license from CERN
- Fabricate our own JOLA boards.
- Test JOLA S-Link cards using existing text fixtures:
  - SLIDAD (Link Source Card)
  - SLIDAS (Link Destination Card)
  - SLITEST (Base Module)

Setup Continued… (JOLA)



JOLA Status

- It works!
- Testing shows that both of the S-Link ends (LSC & LDC), are correctly sending/receiving the data.

S-Link64

- The S-Link cannot keep up. It has a throughput of 160 MBytes/sec, and we need from 250 - 650 MBytes/sec.
- The S-Link64 is an extended version of the S-Link.
  - Throughput: 800MBytes/sec
  - Clock Speed: 100MHz
  - Data size: 64 bits
  - Second connector handles extra 32 bits

The next step…JOLT *(Jlab Optical Link for data Transport)*

- S-Link64 will work for us, but a copper cable with a 10 m cable length will not.
- Xilinx's new V-II Pro offers nice features for next gen.
  - The V-II Pro chip can replace both the Altera FPGA as well as the TI TLK2501.
  - Incorporates PowerPC 405 Processor Block
  - Has 4 or more RocketIO Multi-Gigabit transceivers
    - Each RocketIO has 3.125 Gbps raw rate -> 2.5 Gbps data rate
    - 10Gbps (1.25 Gbyte/s) if 4 channels are used.
  - The full S-Link64 spec requires 3 lanes
  - Error correcting will likely require 4 lanes
  - We may be able to use 2 lanes

JOLT – 1 and JOLT -2

- JOLT will give a crate-to-crate transfer rate of 4 x 2.5 Gbit/s or well in excess of S-Link64 spec of 800 Mbyte/s
- First design is Slink (Jolt-1)
  - One lane version
  - Easily testable with current support boards
- Second design is Slink-64 (Jolt-2)
- CERN is interested in our development.
- Topic 2 of upcoming NSF proposal

Level 3 (Software) Trigger

- Input rate -> 100 - 200 KHz
- Output rate -> 20 KHz
- Need 5-1 to 10-1 rejection
- “Compute” photon energy – reject low energy
- “Full” reconstruction
  - Accuracy can be “less than optimum”

Level 3 (Software) Trigger

- Time estimates based on CLAS hit based tracking
  - 3% momentum resolution
  - 0.1 SpecInts per event
  - (1% takes 9x as long)
- Need 20000 Specints in Level 3 farm for 200 KHz
- Design report -> 200 processors @ 200 Specint/proc
- Factor of 2 for overhead
- P4 @ 3.06 GHz is 1100 Specints.
- Likely to have 1600 - 2000 Specint processors
  - Tradeoff of # processors vs reconstruction precision
- Topic 3 of CNU's upcoming NSF proposal

Conclusion

- Have plan for prototyping L1 crate energy sum
- Have a roadmap to get to very high speed links supporting fully pipelined Gluex triggers
- Borrows liberally from existing designs. Is technically feasible today.
- Have plan for ensuring functioning Level 3 trigger at startup.
- NSF proposal in preparation