

Paul Smith Indiana University

Level 1 Trigger and DAQ

- Front ends fully pipelined
- Trigger "spies" on data and is also pipelined
- Trigger causes "event extraction" from pipeline



Christopher Newport University

U.S. Department of Energy's



F1TDC Specifications



Packaging Inputs Control

Clock

Dynamic Range Standard Deviation INL DNL Acquisition

FIFO Interface

Power

6U VME64x Differential ECL (110 Ohm) 64 Channels @ 120 pS LSB 32 Channels @ 60 pS LSB START, SYNCRES, TRIGGER Front Panel – Differential ECL (110 Ohm) Backplane – Differential LVPECL (110 Ohm) Differential LVPECL (110 Ohm) – 40 MHz Internal, Front Panel, Backplane 7.8 uS (for 120 pS LSB) 3.9 uS (for 60 pS LSB) Less than 0.9 LSB

0 LSB

10-50% LSB Trigger Matching w/ Zero suppression Programmable Trigger Window and Latency 1 M TDC Data Words 32-bit VME Block Transfers (>20 Mbyte/s) 64-bit VME Block Transfers (>40 Mbyte/s) +12V @ 0.5A -12V @ 0.4A +3.3V @ 7.3A +5V @ 1.8A

3 types of FADCs?

8 bits, 250 MSPS	10-12 bits, 125 MSPS	8-12 bits, 62.5 MSPS
4000 channels	3240 channels	11,400 channels
Calorimeters -energy sum	Central Tracking	Forward Drift Cathodes
Other PMT/SiPMT	dE/dX	
low density		high density low cost

Single channel FADC prototype



Test bed for:

- SPT converter chip
- Xilinx chip and software
- Mentor PCB & FPGA software
- Intellectual Property (PCI core)
- Robotic assembly

Indiana University



FCAL Cockcroft-Walton PMT base





100 Prototypes constructed at IU



GlueX Electronics Review - July 23 2003



Andy Lankford (UC Irvine), Glenn Young (ORNL), and John Domingo(JLab)

Selected Review Conclusions:

... characteristics are sound and appropriate choices for GlueX

- Although the GlueX electronics design parameters (e.g. data rates) exceed current JLab experiments, they do not exceed the performance of other contemporary experiments.
- More manpower will be needed in order to fully realize the GlueX electronics system.
 Considerable special (technical) expertise will also be required.

The requirements and specifications of the analog front-end electronics are not yet adequately defined. This is coupled to the tentative status of some detector designs. The lack of full definition of detector designs may soon limit progress on electronics design...

The decision to standardize all detector readout on a single TDC module design and a single Flash ADC module design is good, and will help simplify the overall electronics system design in a constructive way and conserve valuable engineering resources. The Committee feels that it is desirable to locate these modules in a radiation-free area if possible, in order to improve access.

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Status

Detector:	FCAL	BCAL	CDC	FDC	TOF	СКОУ	TAG	STC	UPV
On-detector Electronics:	CW PMT base	SiPM Disc	Preamp	Preamp Disc	Disc	Preamp	Disc	Disc	SiPM
Digitizer:	FADC	FADC	FADC	FADC	FADC	FADC	FADC	FADC	FADC
		TDC		TDC	TDC		TDC	TDC	
LI Trigger:	Energy	Track Count			Track			Track	
	Sum Ene Su	Energy Sum			Count			Count	

"good" shape			
R&D in progress			
need further definition			

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