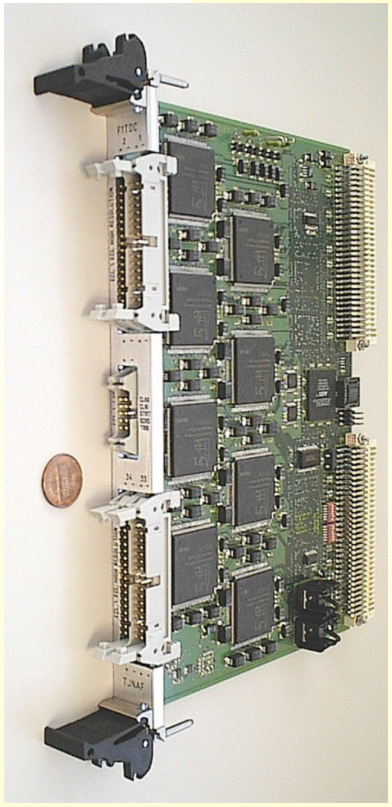
U. S. Department of Energy's
Jefferson Lab
Thomas Jefferson National Accelerator Facility

F1TDC Specifications



Packaging	6U VME64x
Inputs	Differential ECL (110 Ohm)
	64 Channels @ 120 pS LSB
	32 Channels @ 60 pS LSB
Control	START, SYNCRES, TRIGGER
	Front Panel – Differential ECL (110 Ohm)
	Backplane – Differential LVPECL (110 Ohm)
Clock	Differential LVPECL (110 Ohm) – 40 MHz
	Internal, Front Panel, Backplane
Dynamic Range	7.8 uS (for 120 pS LSB)
	3.9 uS (for 60 pS LSB)
Standard Deviation	Less than 0.9 LSB
INL	0 LSB
DNL	10-50% LSB
Acquisition	Trigger Matching w/ Zero suppression
	Programmable Trigger Window and Latency
FIFO	1 M TDC Data Words
Interface	32-bit VME Block Transfers (>20 Mbyte/s)
	64-bit VME Block Transfers (>40 Mbyte/s)
Power	+12V @ 0.5A
	-12V @ 0.4A
	+3.3V @ 7.3A
	+5V @ 1.8A