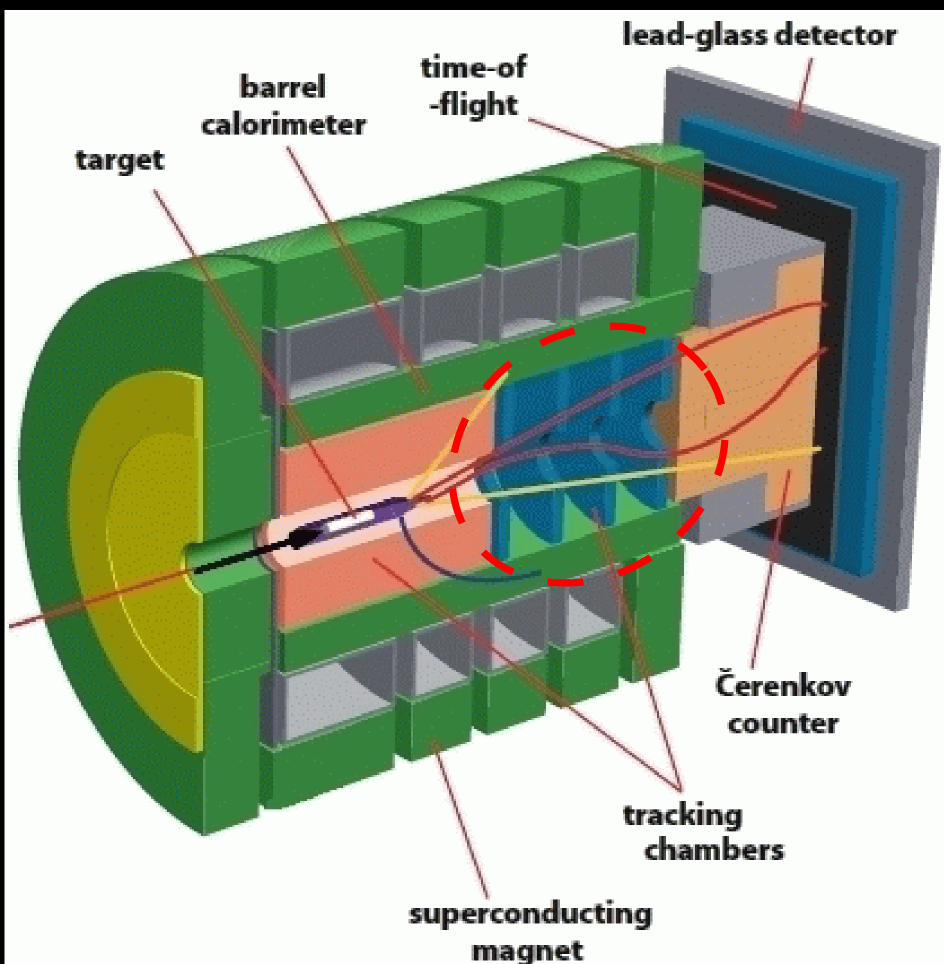
Forward Drift Chamber Detector Review



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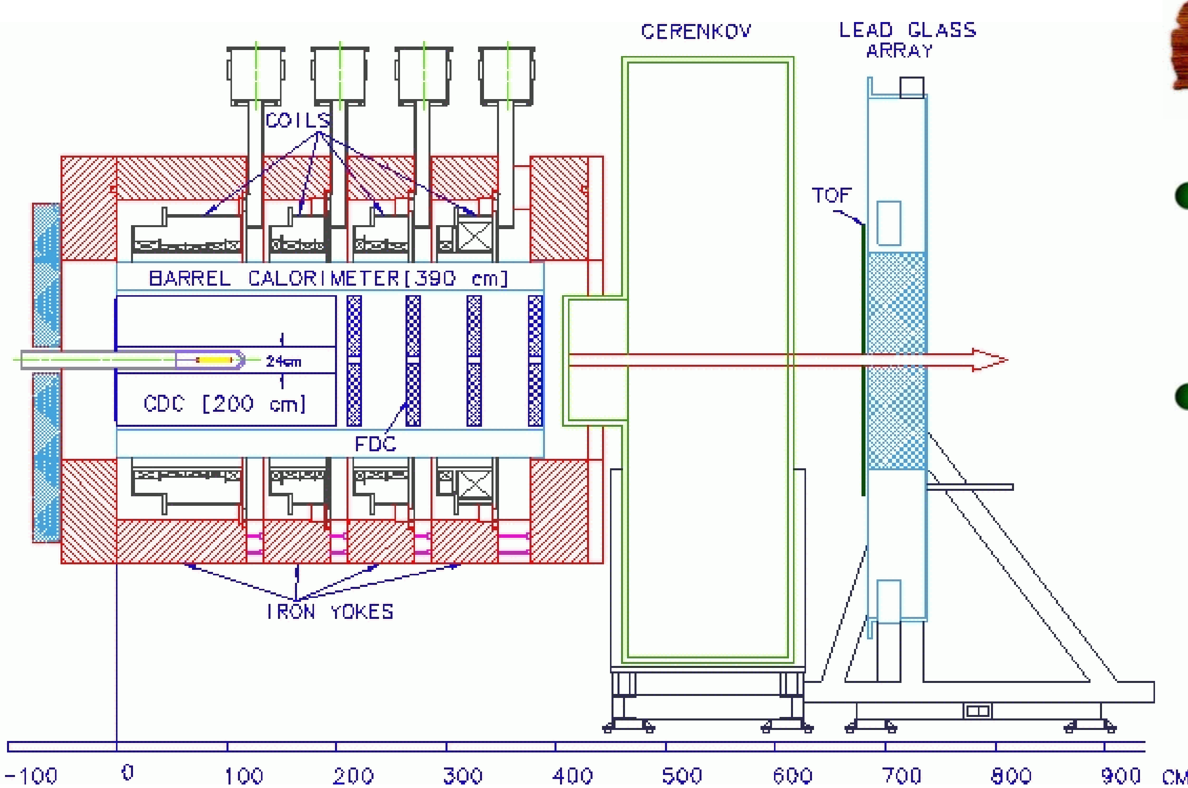
Outline :

- Purpose & Design Goals
- Monte Carlo Studies
- Prototyping Efforts
- Design Issues

Forward Drift Chambers

- **Measure momenta of charged particle tracks emerging from the target up to 30° relative to the photon beam line.**

(FDC only 0−10°; CDC+FDC 10−30°)



System Design

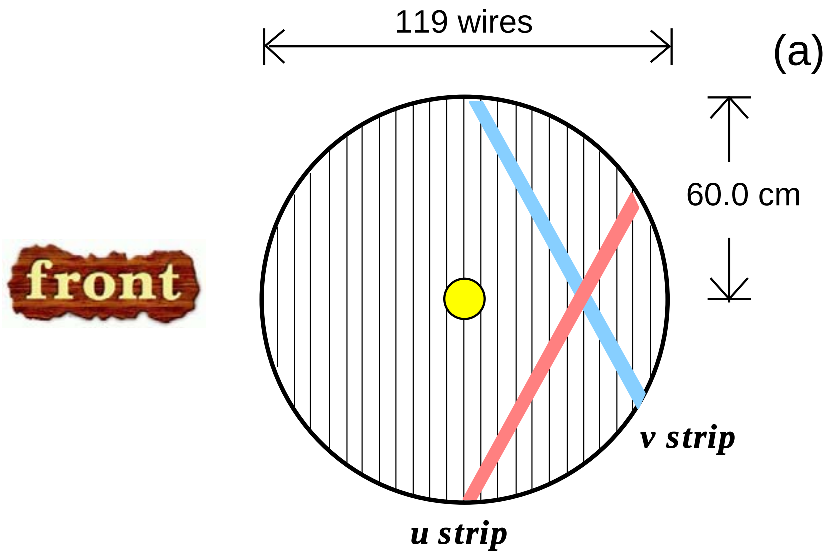
- **Four separate packages**
  - ***equidistant along z***
- **Package design:**
  - ***6 layers each***
  - ***Each layer:***

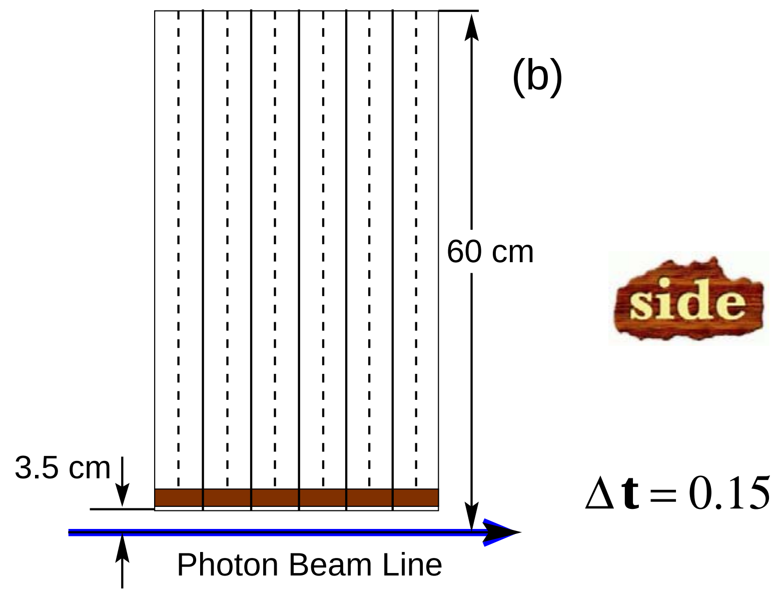
    cathode/wire/cathode

IDENTICAL PACKAGES

Goal: **Space points in each coordinate measured with ~150 μm resolution.**

Forward Drift Chambers





$\Delta \mathbf{t} = 0.15\,\mathbf{gm/cm^2}$

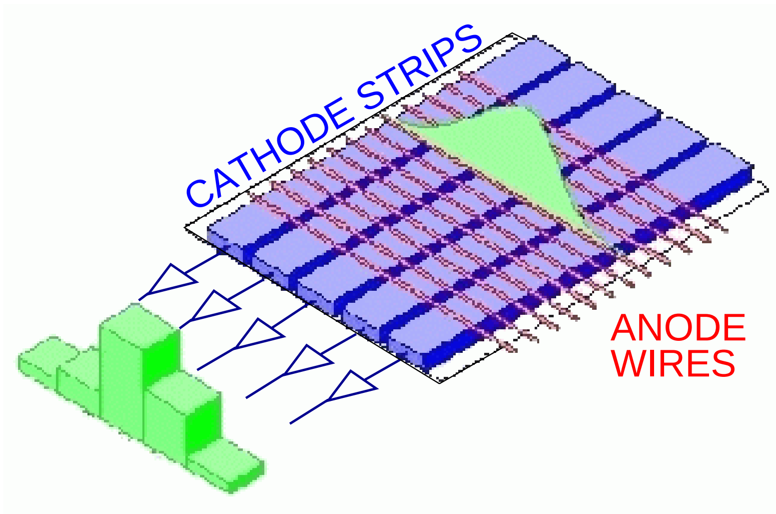
- **Wire planes sandwiched between U & V cathode strip planes.**
- **Neighboring layers within package rotated by 60°.**
- **Total number of channels/package = 3570:**

  119 anode wires/plane x 6 planes = 714 channels

  238 cathode strips/ plane x 12 planes/package = 2856 channels

- **Total number of channels = 14280.**

Cathode Strip Chambers



- **Due to spiraling trajectories and high multiplicity of charged tracks through FDC, system MUST provide:**
  - ***sufficient redundancy to enable reliable pattern recognition.***

    (N_{trk}~ 3−6 tracks/evt + bck)
  - ***good spatial resolution and direction information.***

RESOLVE LOCALLY ** FIT GLOBALLY

- **Determine precision charged track coordinate by interpolating charge on 3−5 adjacent cathode strips.**

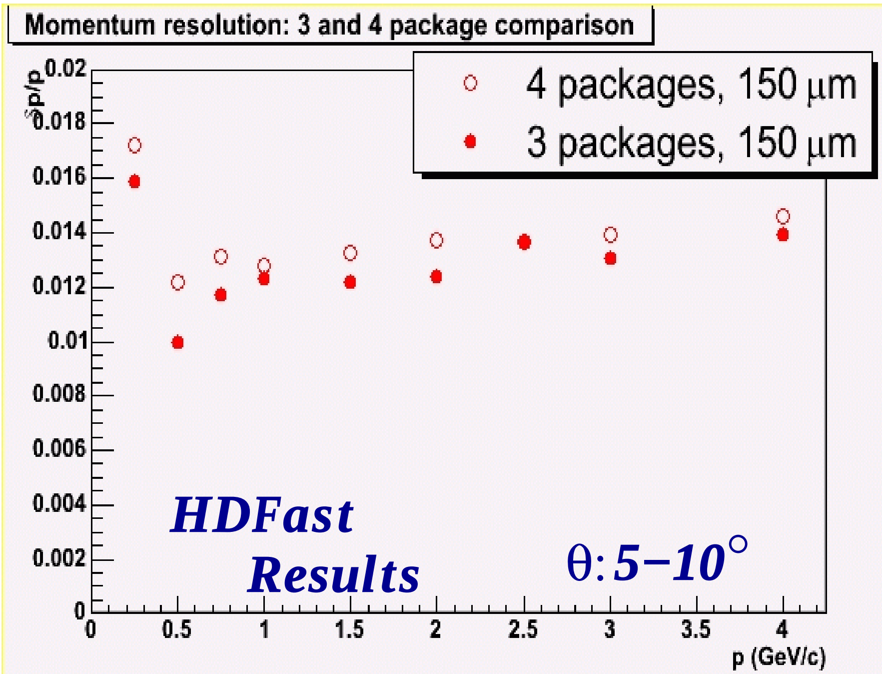
  Measure Q_i distribution with S:N > 100:1.

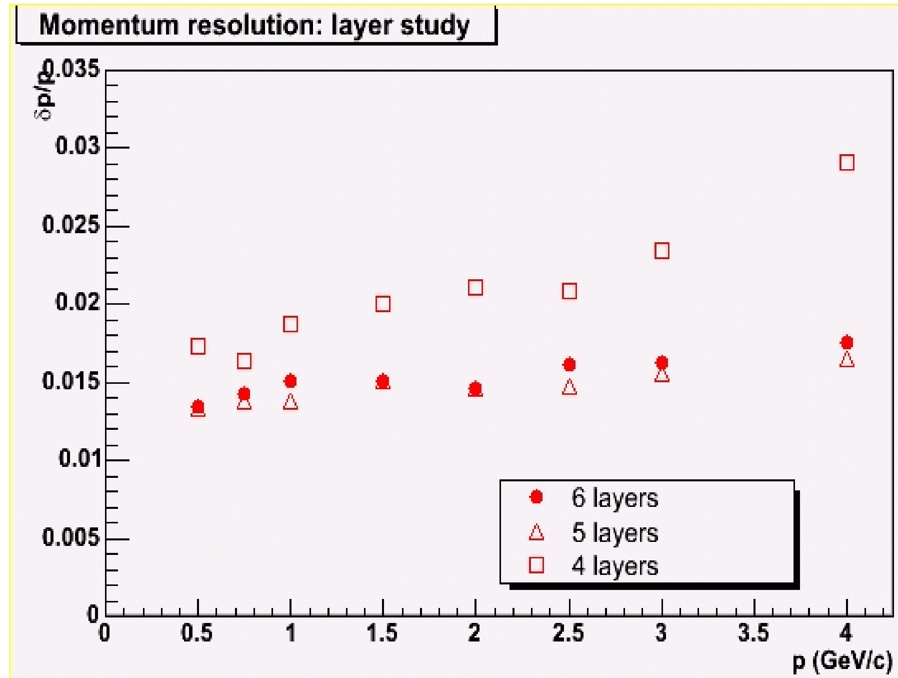
- **Accurate intercalibration of adjacent channels essential.**

  Position accuracy unaffected by gas gain or drift time variations.

Monte Carlo Studies

PRELIMINARY





Assumptions: 150 μm resolution; equal package spacing along z.

Resolution Studies :

- ***Roughly speaking:***

$$\frac{\delta P}{P} = \mathcal{C}_1 + \mathcal{C}_2 * P$$

$\mathcal{C}_1$: *multiple scattering*; $\mathcal{C}_2$: *position resolution*

- ***Single track resolution similar for 3 and 4 package designs.***

But, redundancy essential for pattern recognition!!

FDC Electronics

- **On-Chamber Electronics :**
  - **Low−noise amplifier + pulse shaper.**
    - → *ATLAS−based ASIC design will be used for our purposes.*
  - **Gain ~0.9 mV/fC; gain variation ~2%; calibration precision ~1%**

- **Off-Chamber Electronics :**
  - **Anode: 125 ps LSB resolution F1 TDCs + discriminators.**
  - **Cathode: 125 MHz Flash ADCs (⇒ ~2 ns timing resolution).**

Notes:

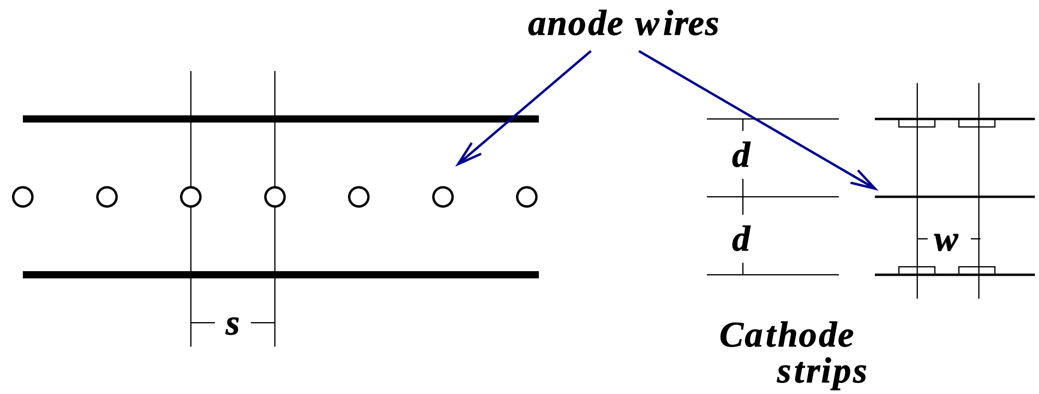
i). Preamp design underway. Collaboration developing between Univ. Alberta and JLab Fast Electronics group.

ii). Clock rate of FADCs not yet fully specified.

− Significant cost reductions possible for slower clock rates.

Initial Prototyping Efforts

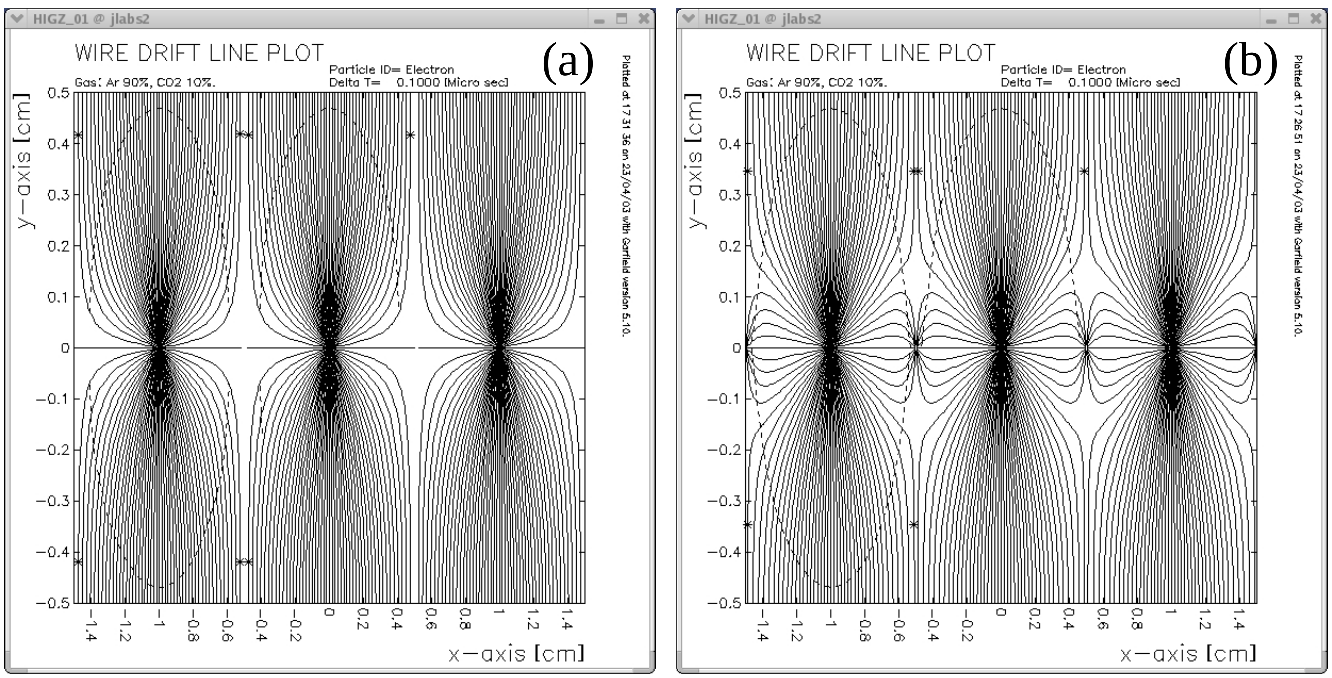
- **Standard CSC design:**



Conditions:

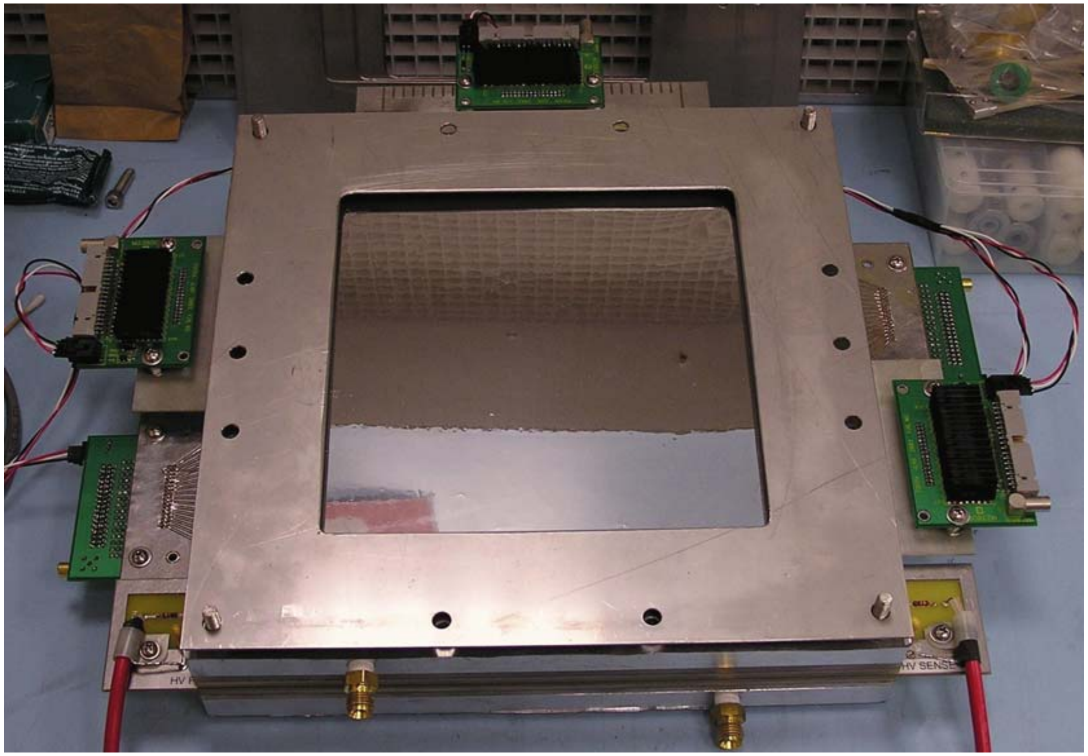
i). No anode wire readout

ii). Field not appropriate for drift chamber.



OPTIMAL ELECTRODE CONFIGURATION??

FDC Prototype #1



Test bed for optimizing the wire plane and cathode plane electrode configurations.

- **1 anode plane consisting of 16 sense wires (10 mm separation) Second configuration with alternating anode and field wires.**

  → **Understand trade−offs between position resolution at cathode plane and timing resolution in the wire plane.**

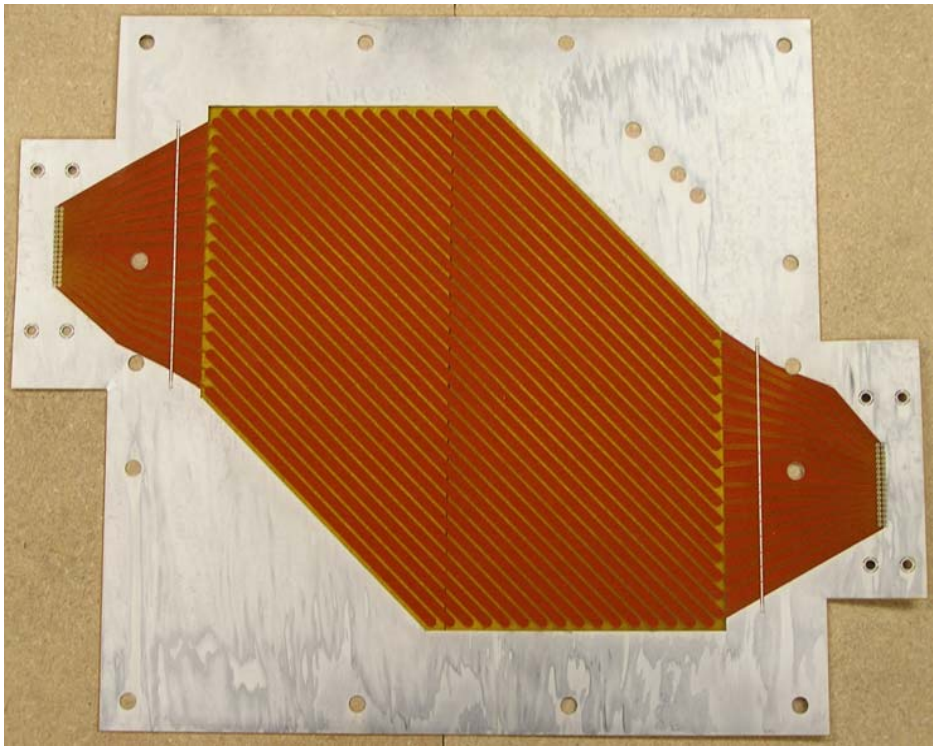
- **2 cathode planes oriented at 45° with respect to wires and 90° with respect to each other.**

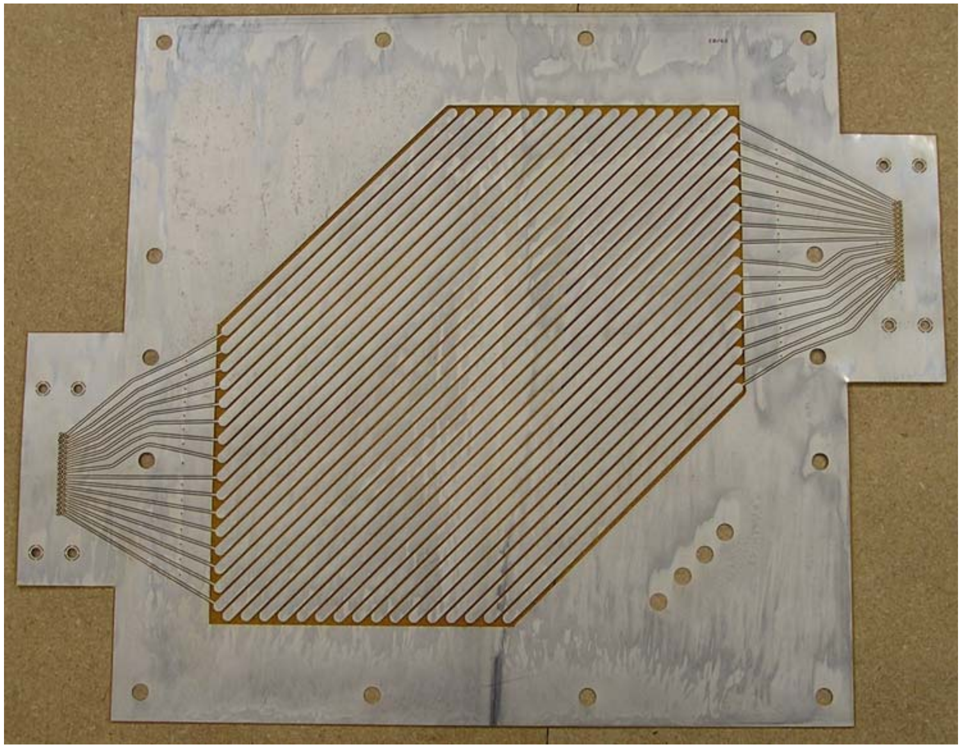
- **Signal routing circuit boards with SIP preamps (CLAS DC design).**

FDC Prototype #1

Cathode Planes

- **Copper−plated kapton, 32 strips, 5 mm pitch, dielectric thickness = 50 μm.**



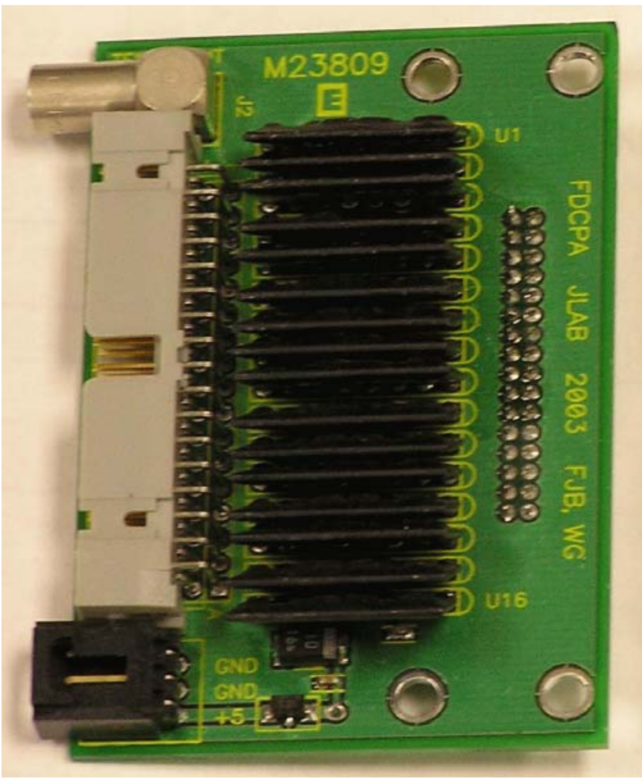


- **Several cathode planes designed: strip separations = 0.25, 0.50, 1.0 mm.**

(+ planes perpendicular to wire direction)

FDC Pre−Amp Boards

HALL B SIP PREAMPS



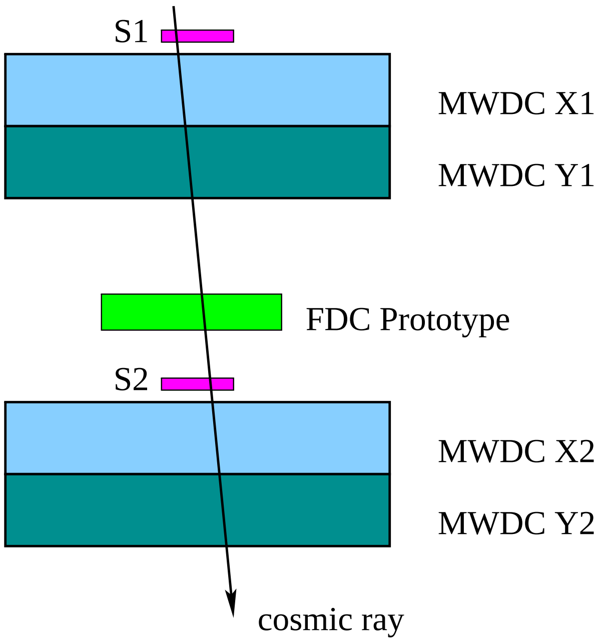
- **Preamplifier properties:**
  - *– Gain 2.25 mV/μA*
  - *– fast rise and fall time (3−4 ns)*
  - *– wide frequency bandwidth*
  - *– wide dynamic range*
  - *– low noise*
  - *– low power dissipation (65 mW)*

- **SIP performance will be used as a benchmark for performance comparisons.**

Presently cathode and anode amplifier boards are identical except for cathode polarity inversion.

Cosmic Ray Telescope

Purpose: Define tracks with ~200 μm resolution at FDC position.



- **Trigger: coincidence between top and bottom scintillator paddles.**

  Coincidence logic in NIM electronics.

- **Cosmic ray test chamber anode signals amplified and discriminated by chamber−mounted LeCroy 2735DC boards with adjustable thresholds.**

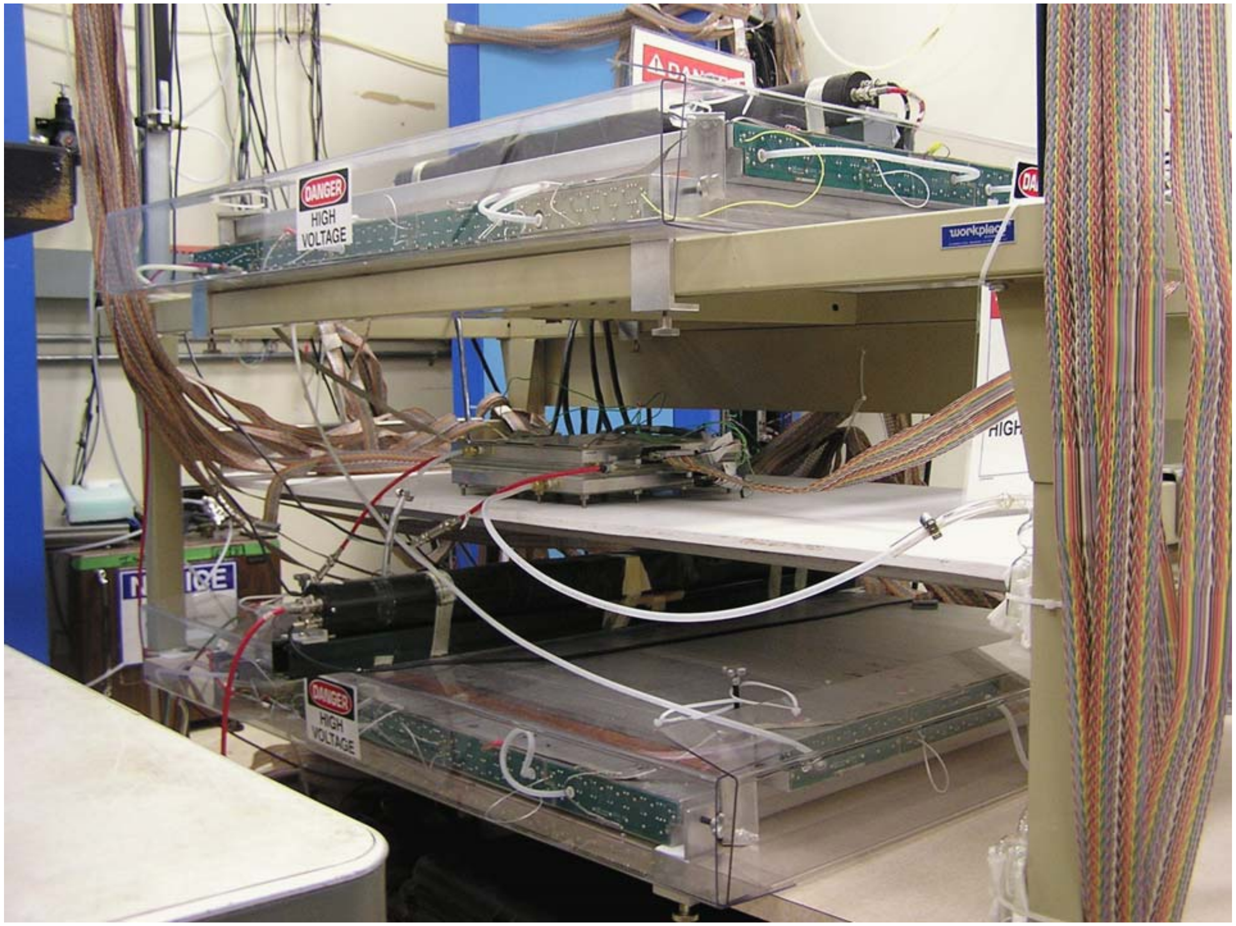
  Timing signals read out with LeCroy 1877S multi−hit FASTBUS TDCs.

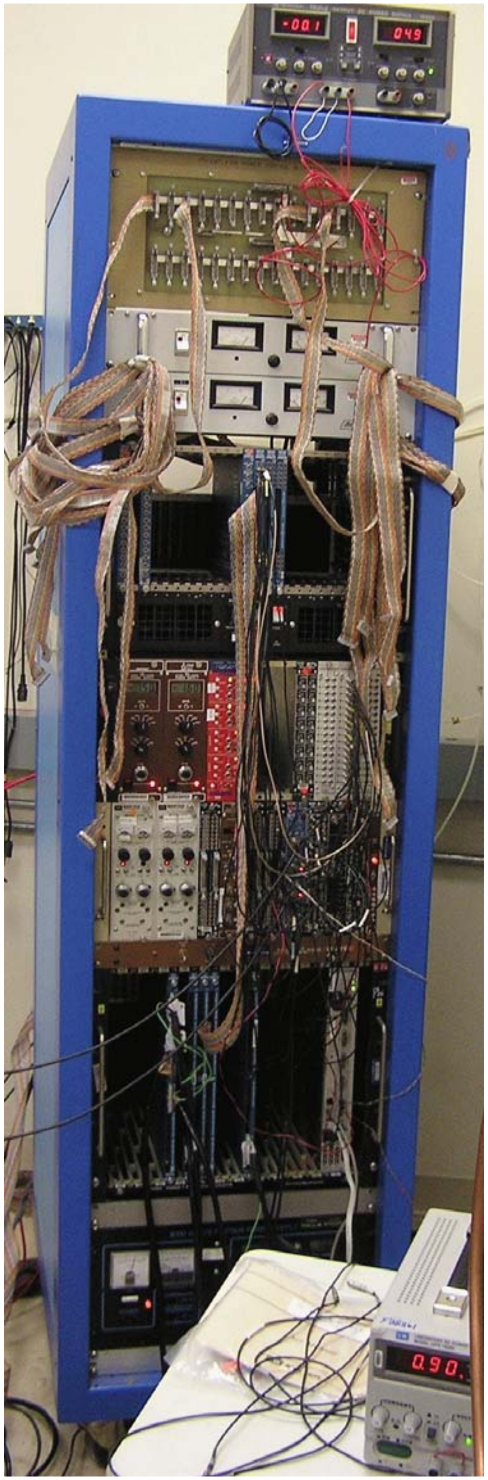
- **FDC prototype signals amplified by Hall B “SIP" preamps.**

  Anode signals discriminated by LeCroy 3412E and digitized by 1877S TDC.

  Cathode signals read out with LeCroy 1881M FASTBUS ADC.

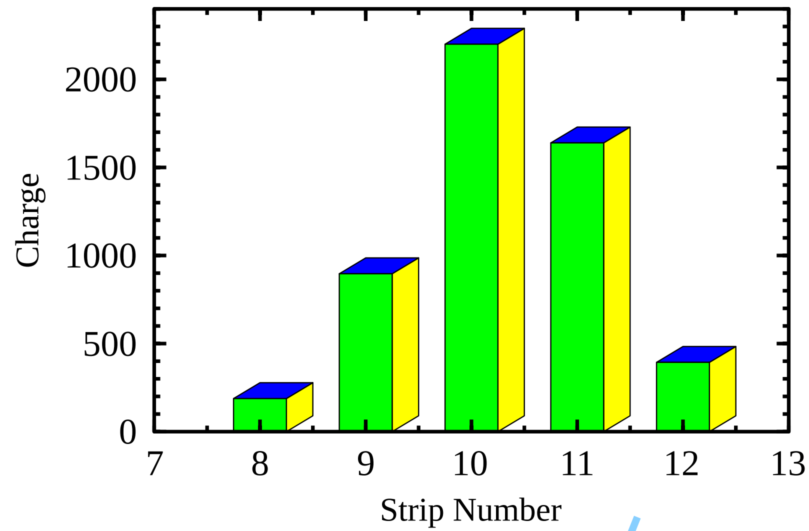
Test Setup for Prototype Studies

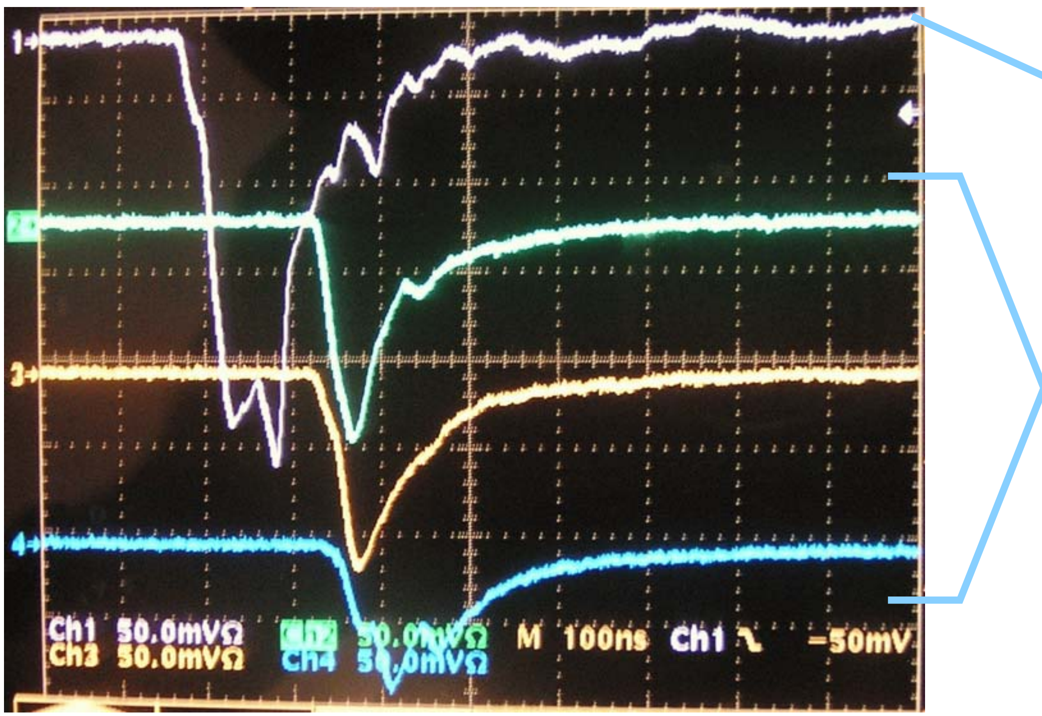


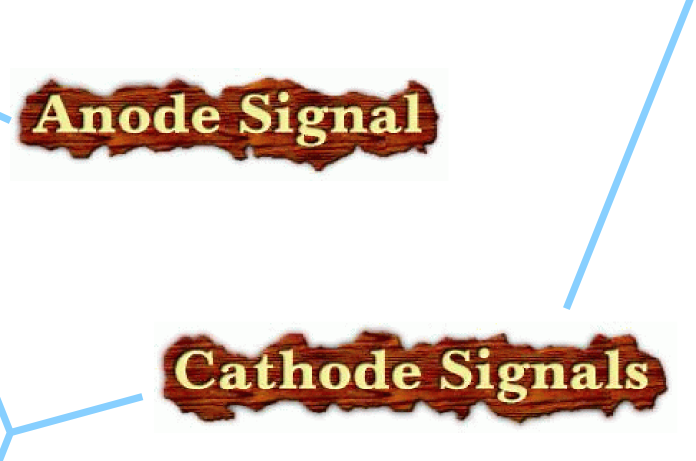


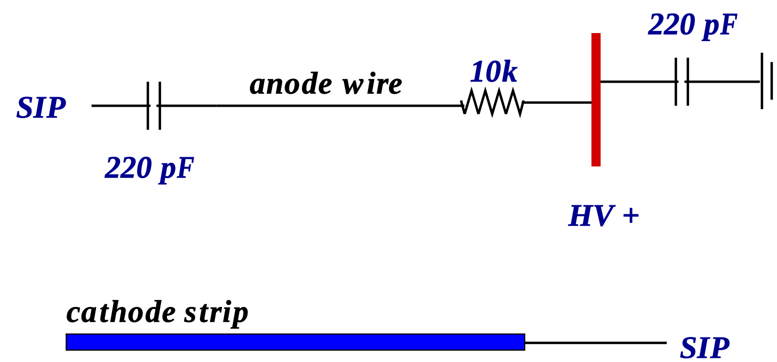
FDC Prototype Signals

- **Anode wires at +1.8 kV, field wires and cathodes at ground.**

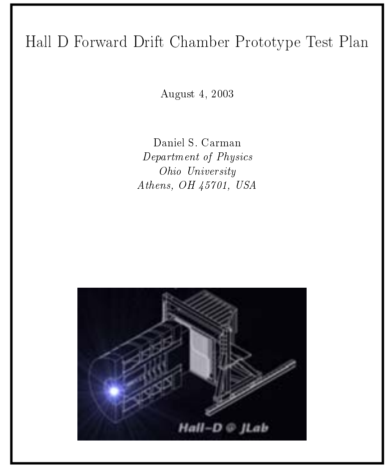








FDC Test Plan


Hall D Forward Drift Chamber Prototype Test Plan

August 4, 2003

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Hall-D @ JLab

- **A detailed test plan outlining the FDC prototyping effort has been provided to the collaboration.**

Prototype Assembly

- *chamber cleaning*
- *wire plane stringing*
- *electronics mounting*
- *stack assembly*

Bench Testing

- *short checking*
- *gas flow*
- *HV plateau*
- *gas gain measurements*
- *noise measurements*

Resolution Studies

- *cosmic−ray telescope*
- *single track resolution*
- *two−track resolution*
- *electrode configurations*
- *cross talk measurements*
- *efficiency*

Miscellaneous

- *magnetic field studies*
- *wire deadening*
- *RF noise pickup*
- *alignment & positioning*
- *internal chamber supports*

Future Prototyping

- In terms of detector prototyping, we foresee that at least two working chamber prototypes will be required to complete the FDC R&D.

Prototype #2: Main design issues include:

- Mechanical design issues.

  (field uniformity)

- On−chamber electronics design/layout.

Design work to commence in the late winter/early spring.

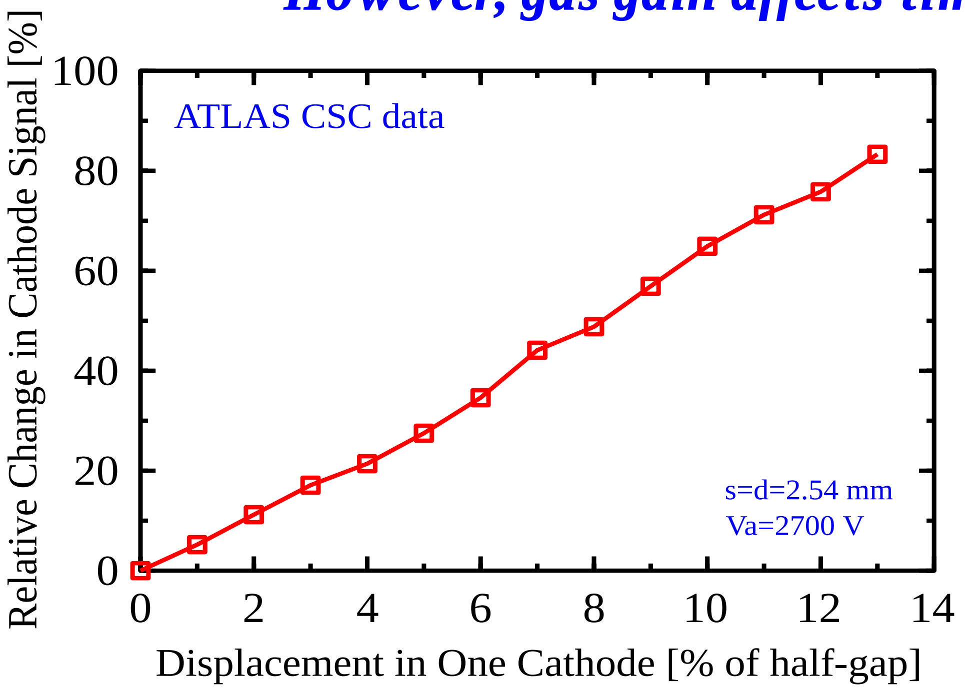
Other R&D: − Full scale mock−ups for testing chamber mounting & alignment schemes + cable routing + installation.

INCREASE ACCESSIBILITY TO MINIMIZE DOWN TIME.

− Gas system design (TJNAF detector group).

Cathode Resolution Effects

- **Fractional charge on cathode is not important for cathode precision.**
  - ***Relative charge measurement.***
  - ***Must be reasonably uniform for operational stability.***
- **Must control gas gain for time−to−distance calibration.**
  - ***Cathode resolution relatively independent of gas gain.***
  - ***However, gas gain affects time walk correction for drift time.***



- **To keep stable to +/− 20%, gap tolerance must be defined to roughly 100 μm.**

Chamber Failure Modes

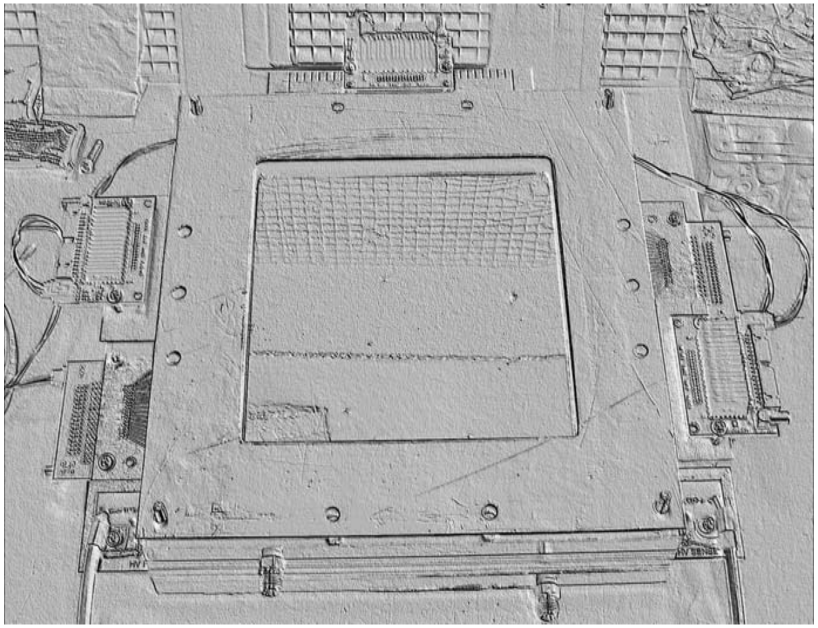
- **An important design aspect is to understand potential chamber failure modes.**
  - **Understand impact on system operation.**
  - **Affect design to minimize impact.**
  - **Minimize access time to system within solenoid.**
  - **Design must allow for access to critical detector components.**

Failure Modes

- *Broken wires*
- *LV transformer failure*
- *Circuit board short*
- *Preamp corrosion*
- *High current draw*
- *Cable disconnect*
- *Increased noise*
- *Swapped cables*
- *HV disconnect*
- *LV disconnect*
- *Pinched gas line*
- *Gas leak*
- *Window tear/rupture*
- *Internal chamber short*

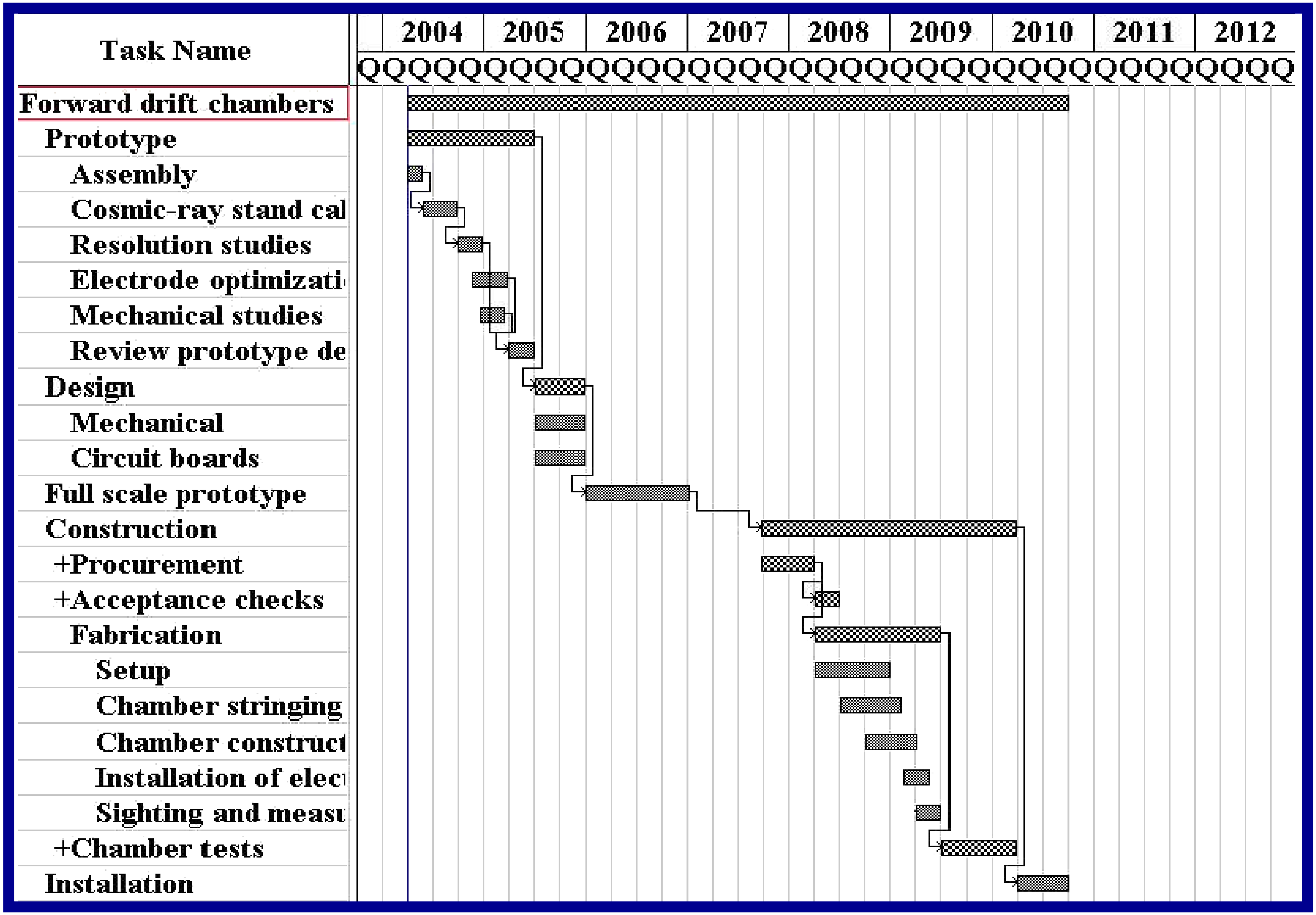
Other Issues & Conclusions

- Current prototype chamber under study to optimize basic electrode design.
- Converge on appropriate redundancy.
- Need to study and test different gas mixtures for performance.
- Move ahead with R&D program for on−chamber electronics.
- Work to design full−scale prototype.
- Finalize FADC design for FDC system.
- In−beam cathode chamber tests.
- Study how to deaden wires about the beam hole.



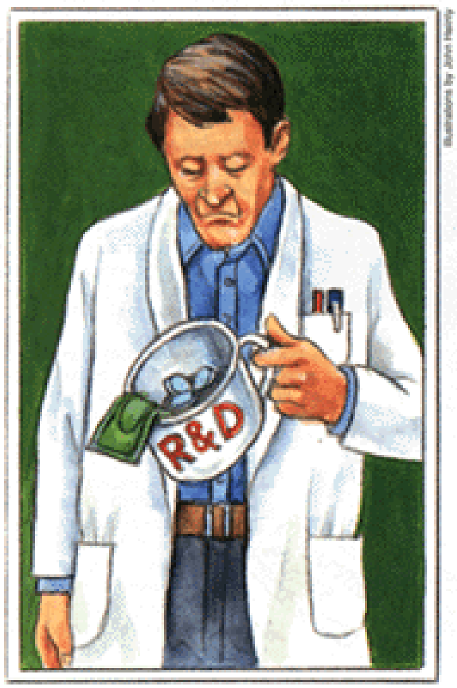
Backup Slides for Review

Forward Drift Chamber Timeline



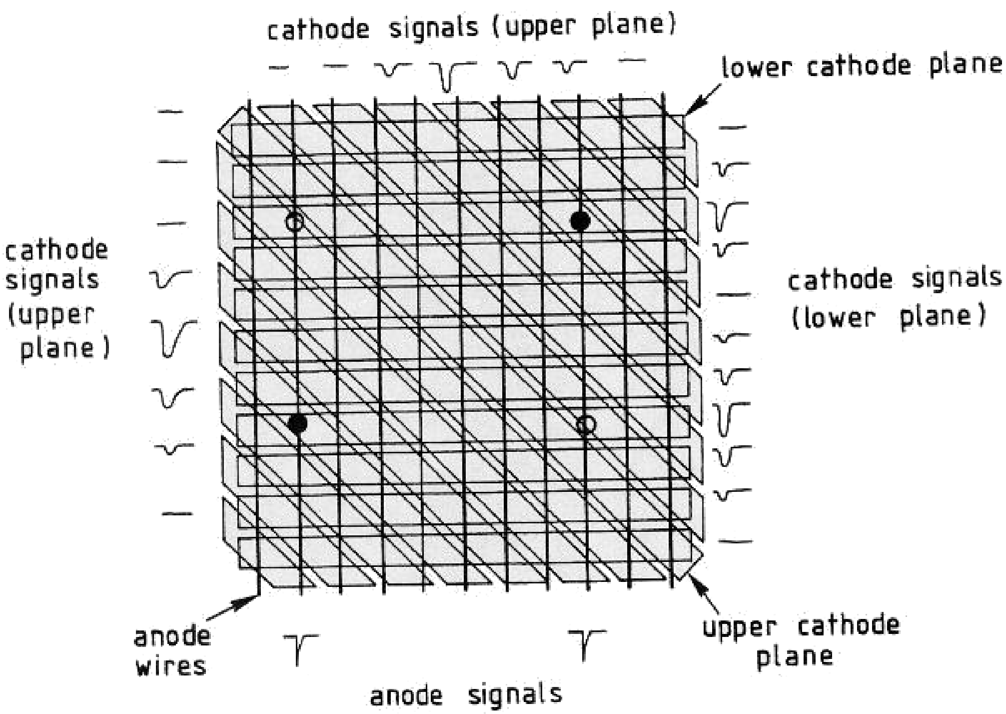
FDC R&D Issues

- **Optimization of electrode configuration.**
  Circuit board design.
  Mechanical support design.
  Optimization of gas choice.
  Performance in magnetic field.
  Performance in RF environment.
  Noise immunity.
  Manufacturing techniques.
  Strip−to−strip intercalibration.
  Pulse shaping and amplification.
  Radiation tolerance assurance.
  Gain monitoring.
  Mounting and alignment.
  Serviceability.
  Cable routing.
  Aging.



Pattern Recognition

- **Monte Carlo simulations indicate the following:**
  - ***charged particle rate across FDC chambers ~1 MHz.***
  - ***expect roughly 3−6 charged tracks per event.***
  - ***expect roughly 1−2 background tracks per event.***
  - ***expect a few % occupancy due to photon conversions, etc.***



Redundancy is crucial to allow for accurate pattern recognition.

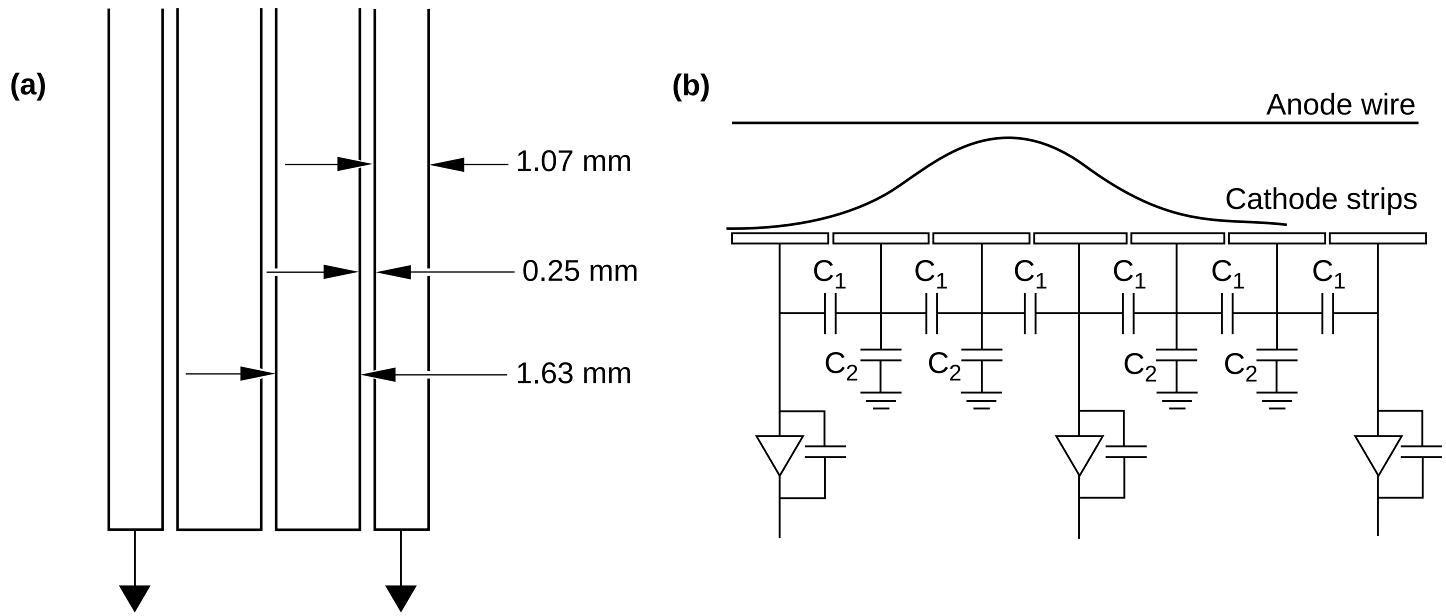
Experience from CLAS provides clear direction for successful L/R resolution and pattern recognition:

RESOLVE LOCALLY ** FIT GLOBALLY

Alternate Cathode Design

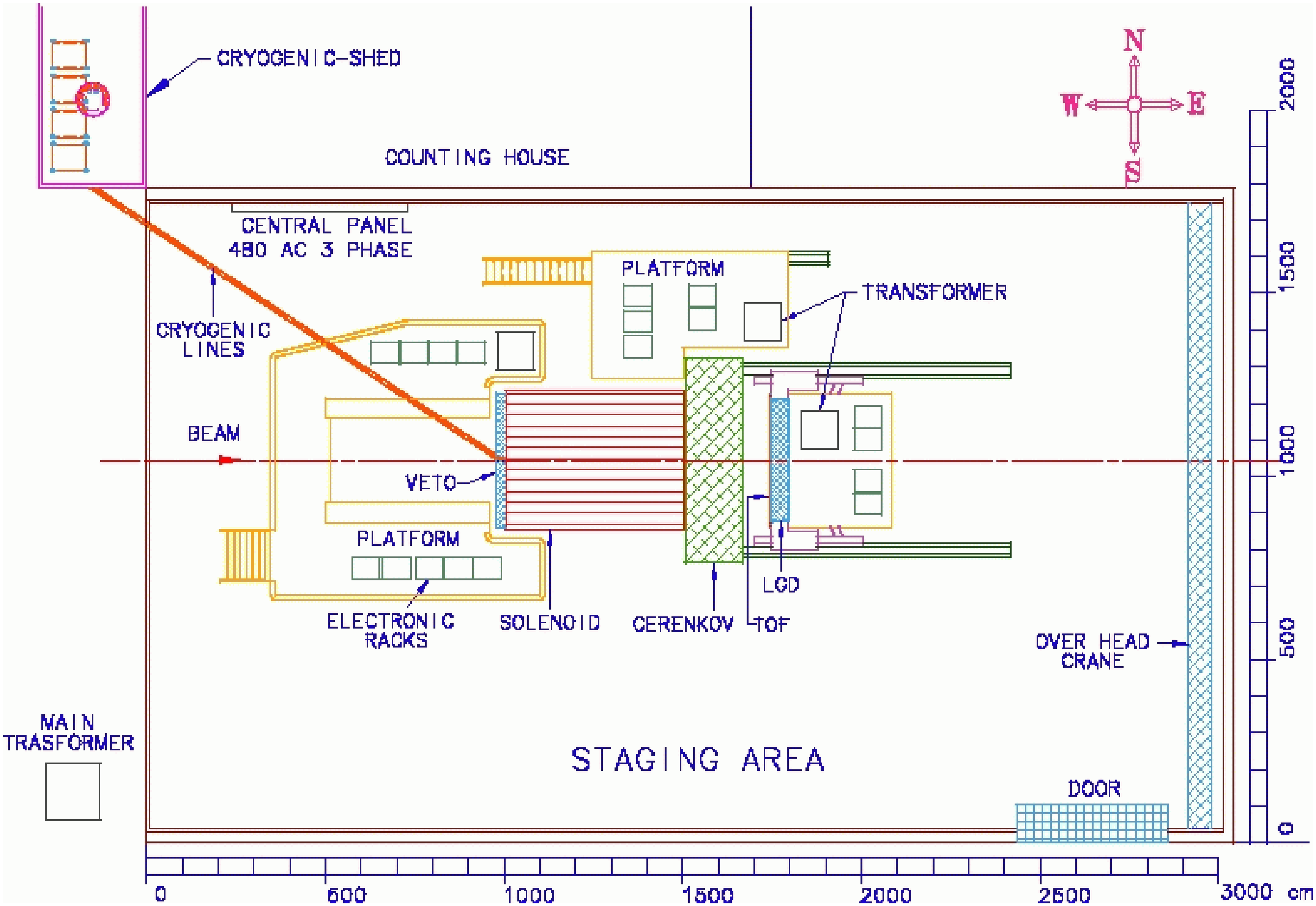
- **Other groups (e.g. ATLAS) have constructed chambers with fewer cathode readout strips (w/d > 1).**

Maintain: acceptable resolution, minimal differential non−linearity.



Intermediate strips capacitively coupled together.

Hall D Layout



FDC Specifications

Parameter	Value
Wire spacing s	10 mm (anode-anode), 5 mm (anode-field)
Anode-cathode distance, d	5.0 mm
Cathode readout pitch, w	5.0 mm
Gap between cathode strips, w_g	1.0 mm
Width of cathode strips	4.0 mm
Capacitance between strips	0.6 pF/cm
Resistance between strips	$\sim$20 MΩ
Anode wire radius, r_a	0.010 mm
Wire capacitance per unit length, C_0	$\sim$9 pF/m
Gas gain	4×10^4
Operating voltage at nominal gain	1800 V
Electric field at cathode, E_c	$<$1 kV/cm
Electric field on anode wire surface	280 kV/cm
Field-shaping wire radius	0.040 mm
Electric field on field-shaping wire surface	15 kV/cm
Positive ion mobility, μ^+	1.3 cm^2/V/s
Total ion pairs	180
Minimum wire tension	50 gm
Total charge collected	$\sim$50 fC
Charge collected in 30 ns (%)	$\sim$20%