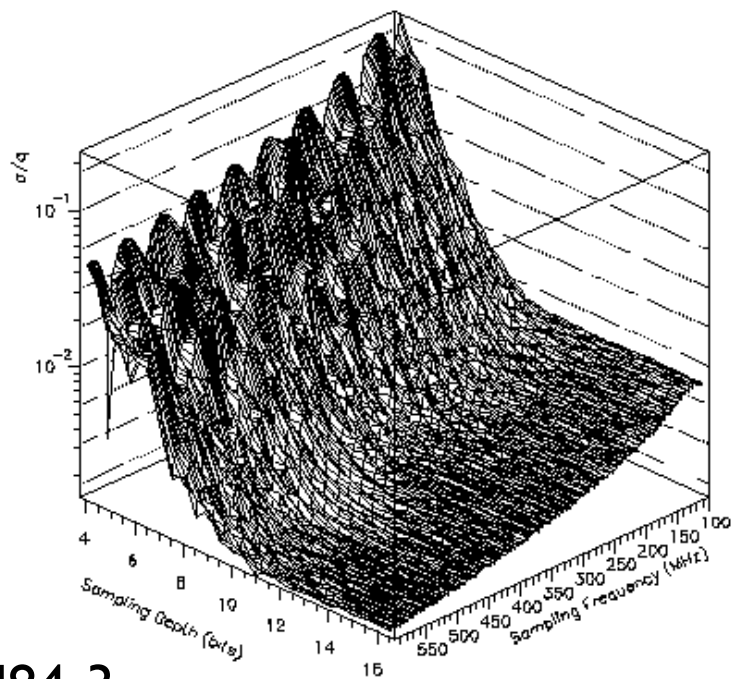
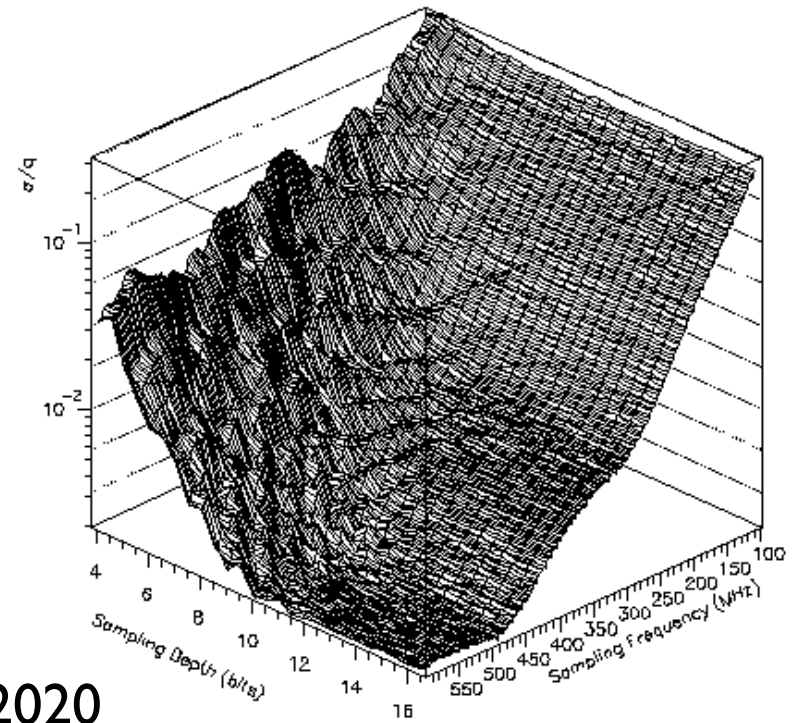


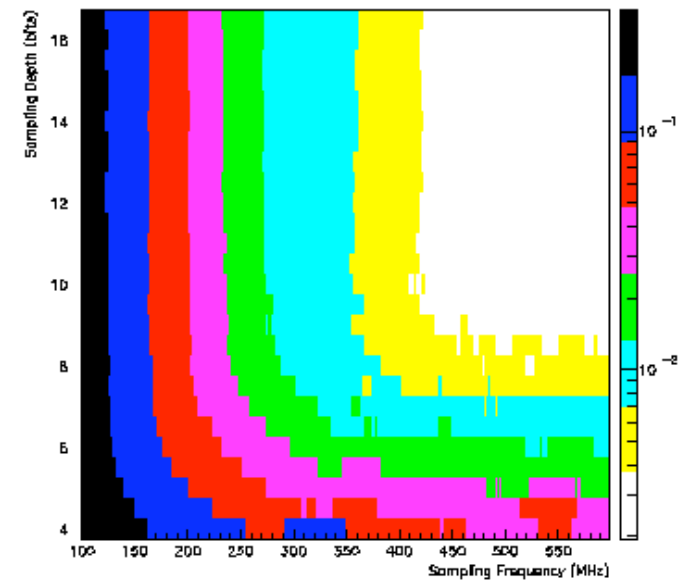
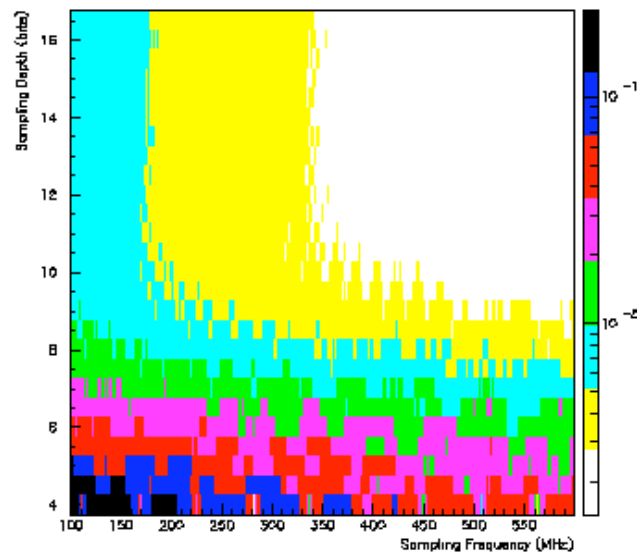
Sum from 120 to 180 nS = 1429



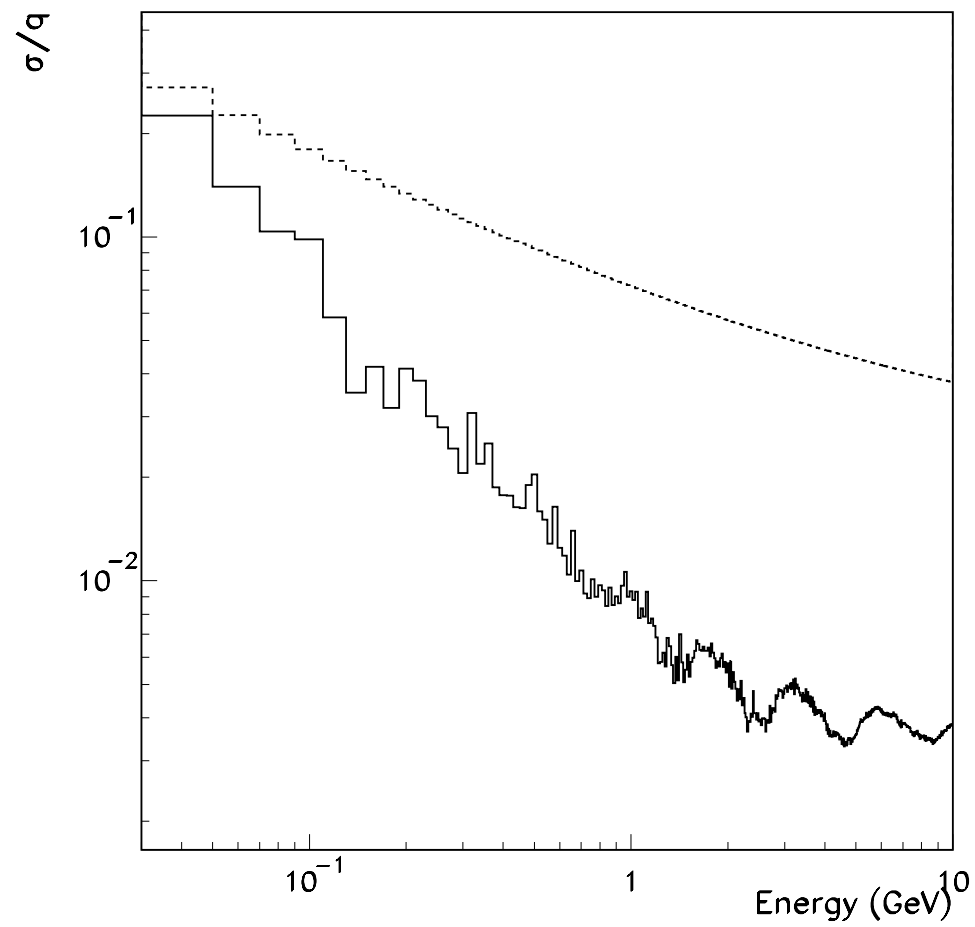
FEU84-3



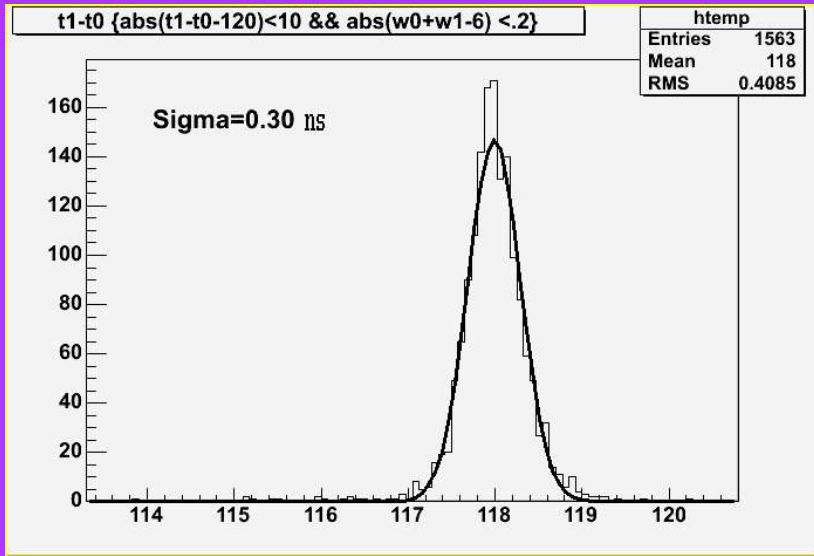
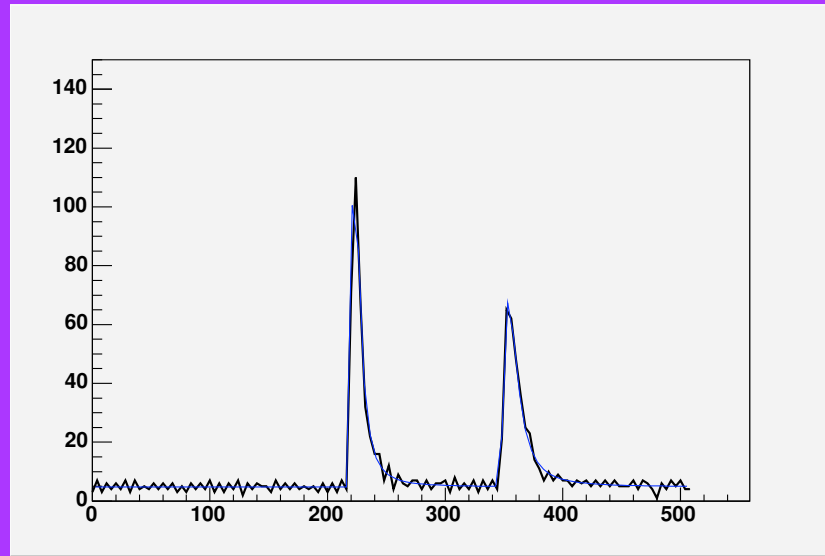
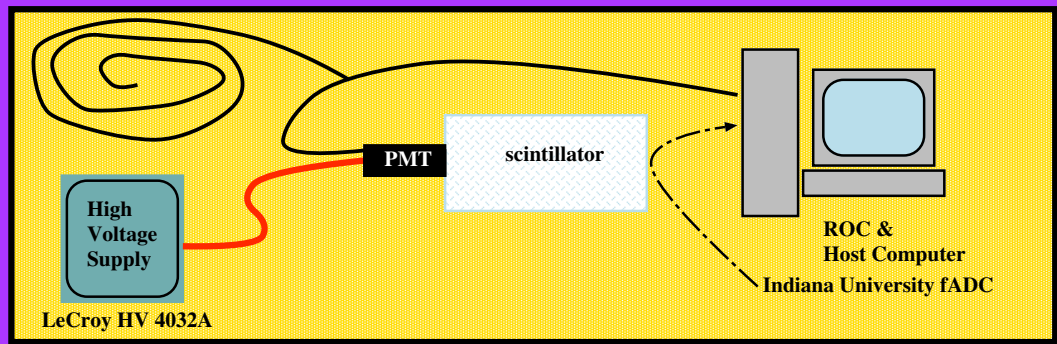
XP2020



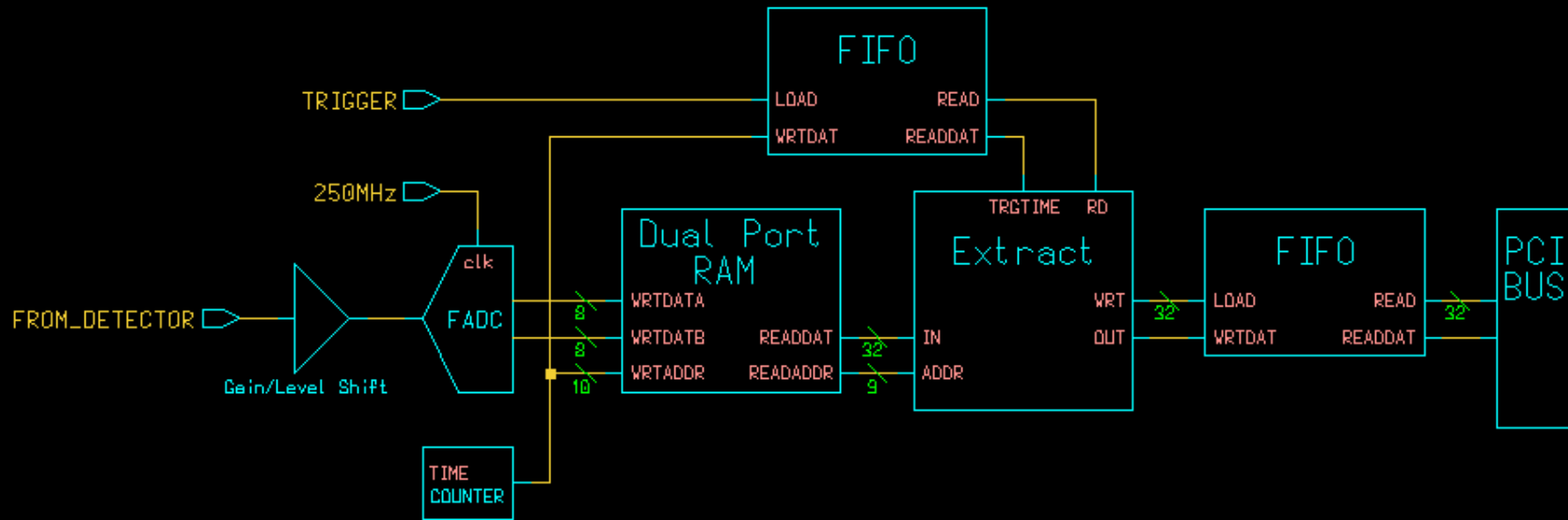
FEU84-3 250 MHz 8 bits



Timing - echo test



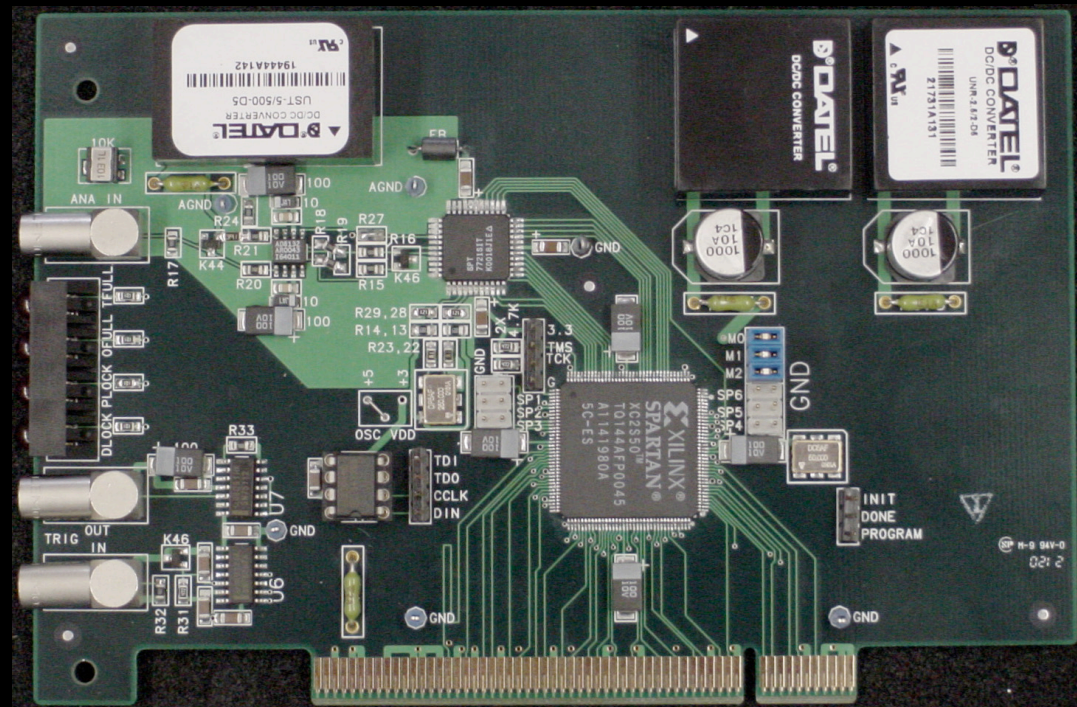
Single channel FADC prototype



Test bed for:

- SPT converter chip
- Xilinx chip and software
- Mentor PCB & FPGA software
- Intellectual Property (PCI core)
- Robotic assembly

Indiana University



Parameters Core Overview Contact

Dual Port Block Memory

Component Name:

Memory Size

Width A: Valid Range: 1..256 Depth A: Valid Range: 2..32768
 Width B: Depth B:

Port A Options

Configuration: Read And Write Write Only Read Only
 Write Mode: Read After Write Read Before Write No Read on Write

Port B Options

Configuration: Read And Write Write Only Read Only
 Write Mode: Read After Write Read Before Write No Read on Write

Initial Contents

Global Init Value: (Hex Value)
 Load Init File
 Load File... (.coe File)

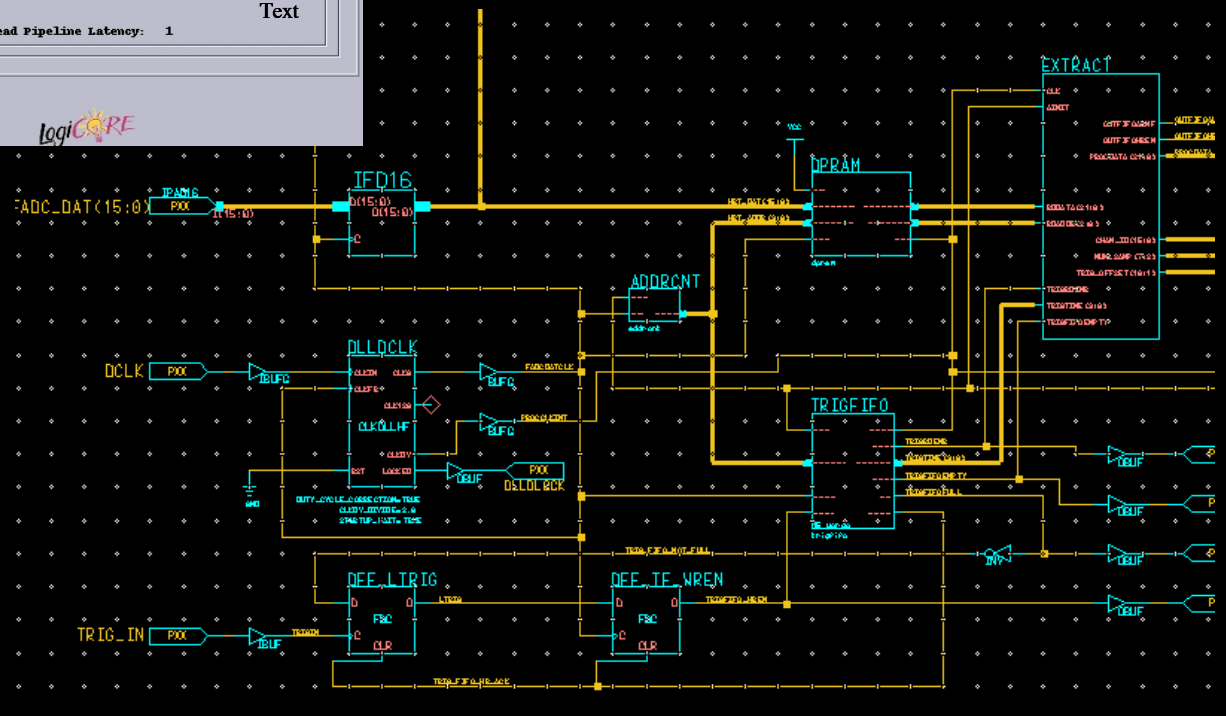
Information Panel

Address Width A:	4	Address Width B:	4
Blocks Used:	1		
Port A Read Pipeline Latency:	1	Port B Read Pipeline Latency:	1

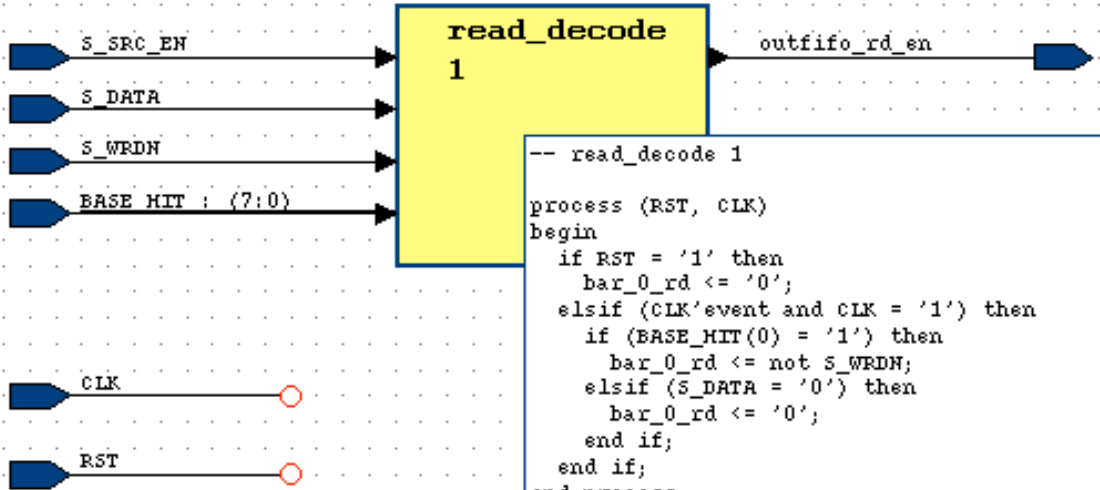
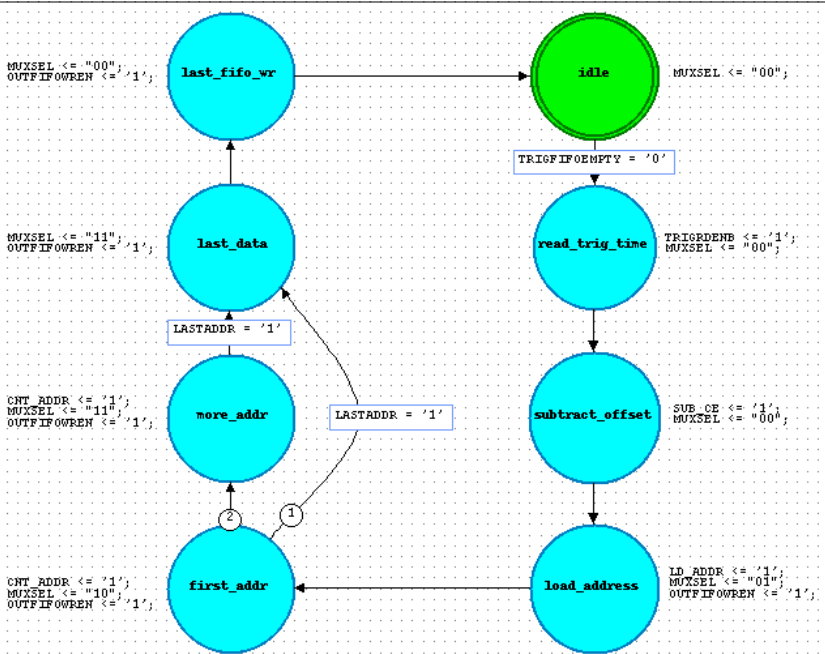
Text

Display Core Viewer after Generation

Xilinx schematic



Mixed VHDL & Graphics

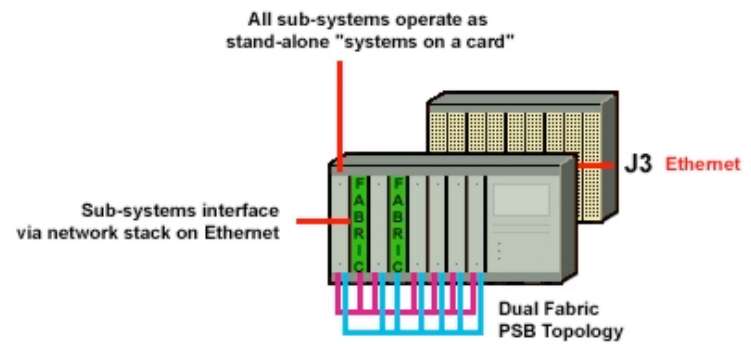
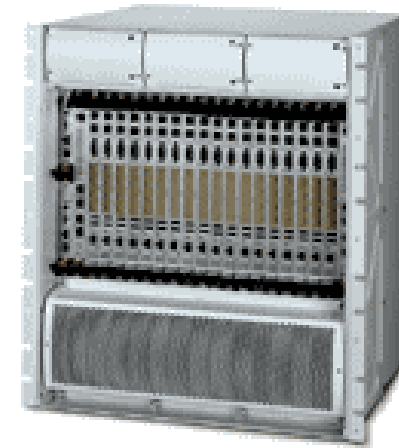
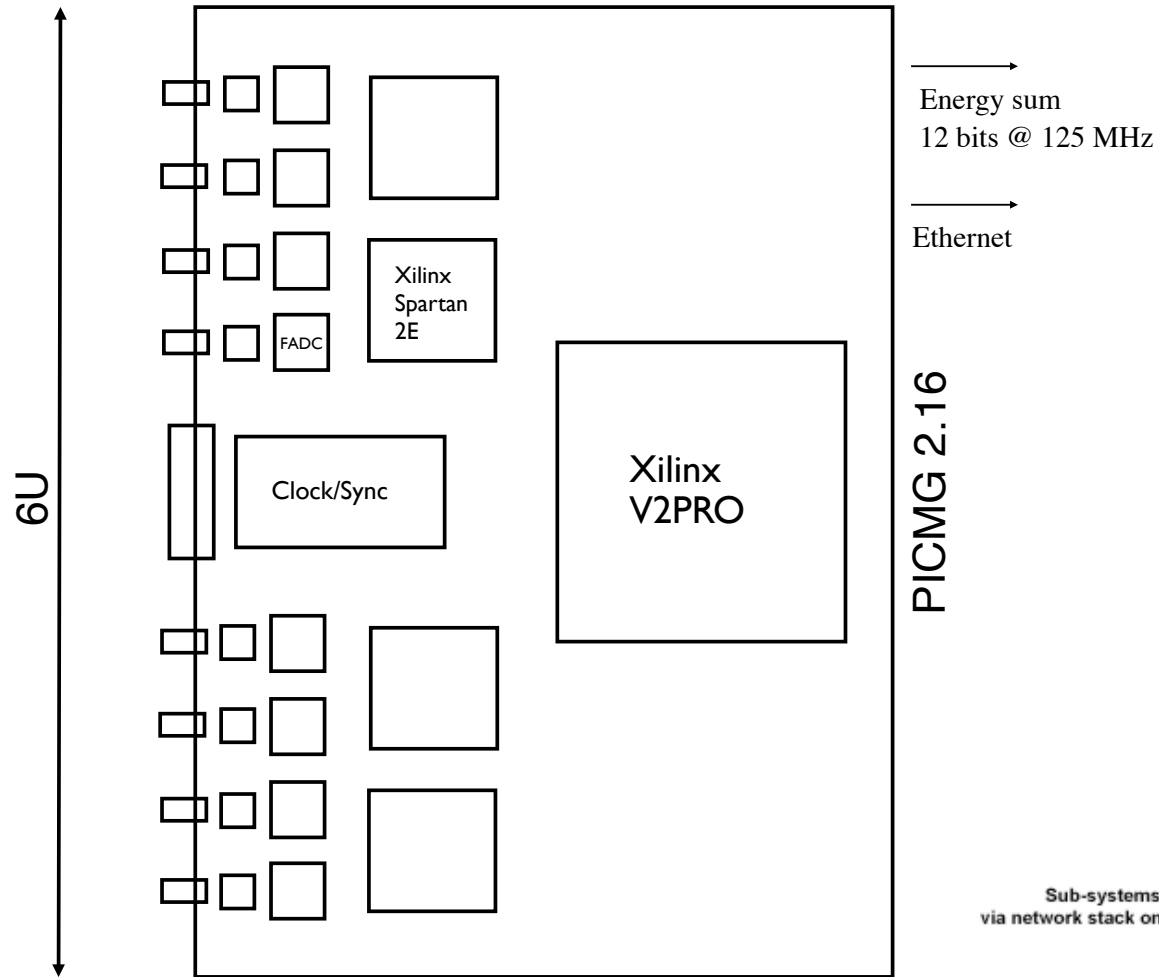


```

-- read_decode 1
process (RST, CLK)
begin
    if RST = '1' then
        bar_0_rd <= '0';
    elsif (CLK'event and CLK = '1') then
        if (BASE_HIT(0) = '1') then
            bar_0_rd <= not S_WRDN;
        elsif (S_DATA = '0') then
            bar_0_rd <= '0';
        end if;
    end if;
end process;

outfifo_rd_en <= BASE_HIT(0) and not S_WRDN;
    
```

Next (final?) version



-- Underlying Concepts --

From the review:

- The general concept of local sums at the front-end board level, followed by crate-level sums and subsequent transfer to a central “Global LV1-1” processing area, is sound. A concept and proof-of-principle for crate backplane operation at the required high rate needs to be developed for the CDR. If high-speed serial operation proves challenging, the collaboration should explore possible parallel concepts to lower the bus-speed requirements.

Possible Crate Layout

Ethernet switch	
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
Clock/Sync	
Energy Sum	16 bits @ 125 MHz
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
○ ○ ○ ○	FADC ○ ○ ○ ○
Single board computer	

