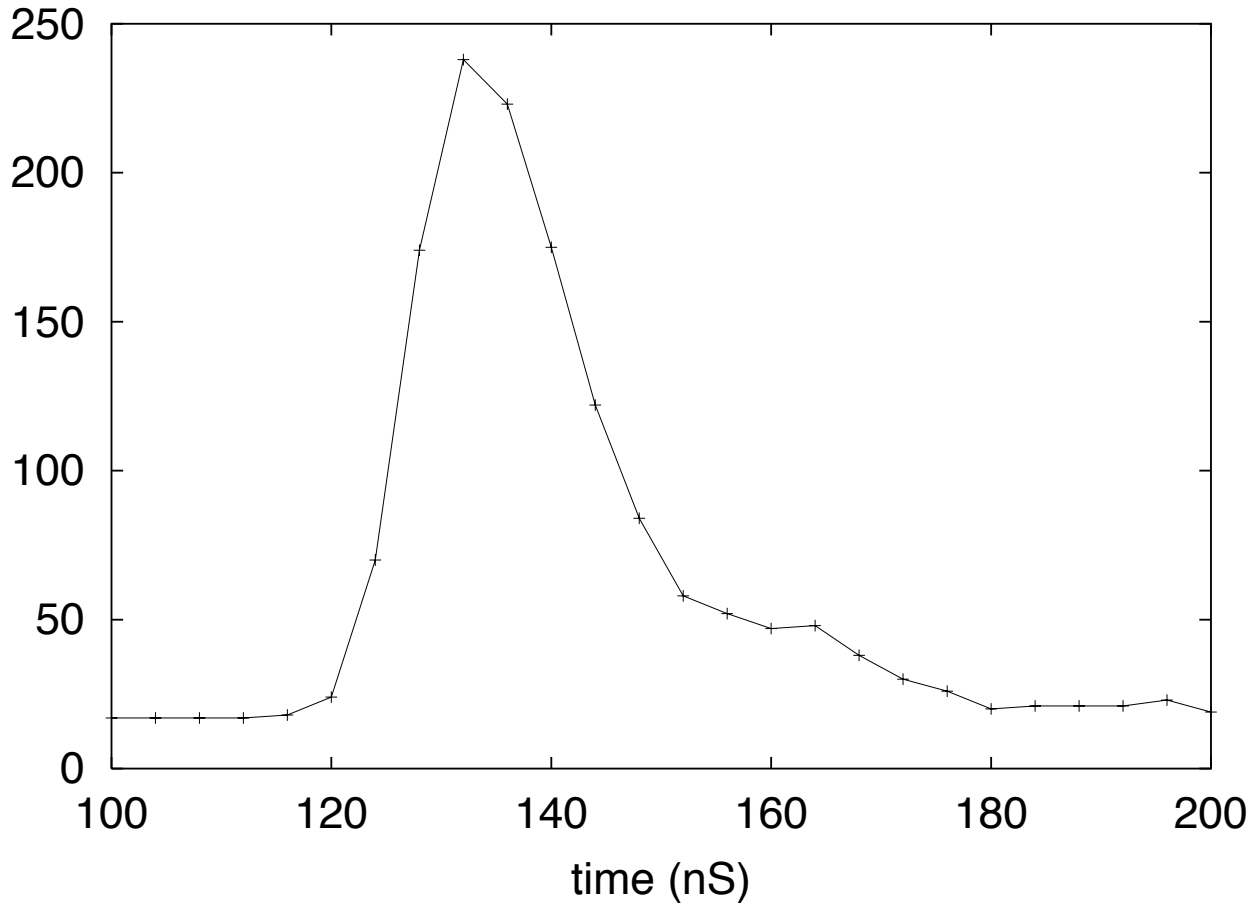
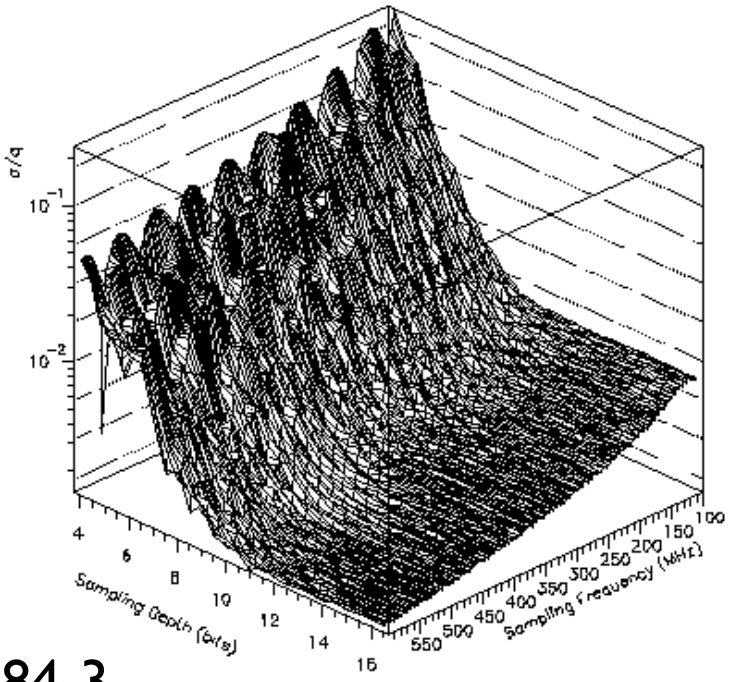
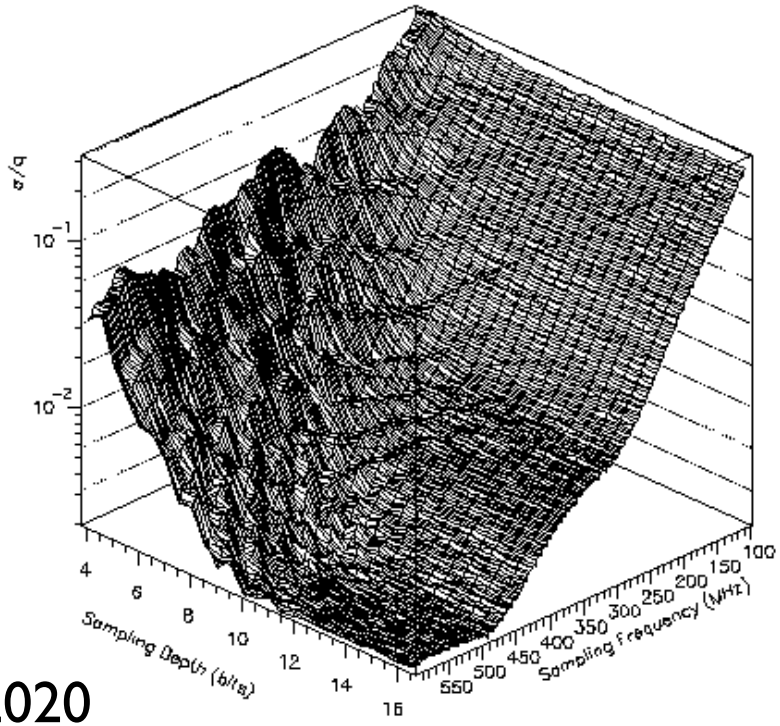


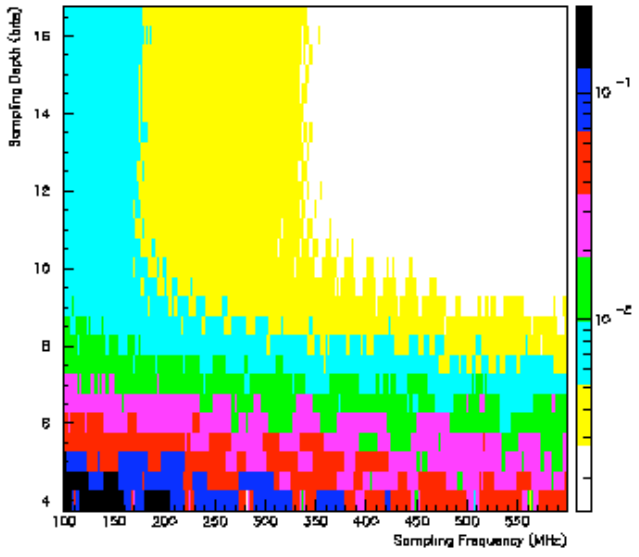
Sum from 120 to 180 nS = 1429

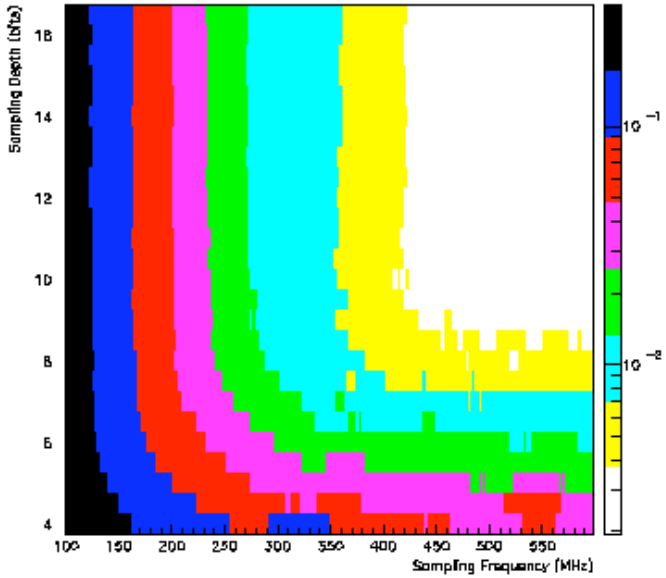


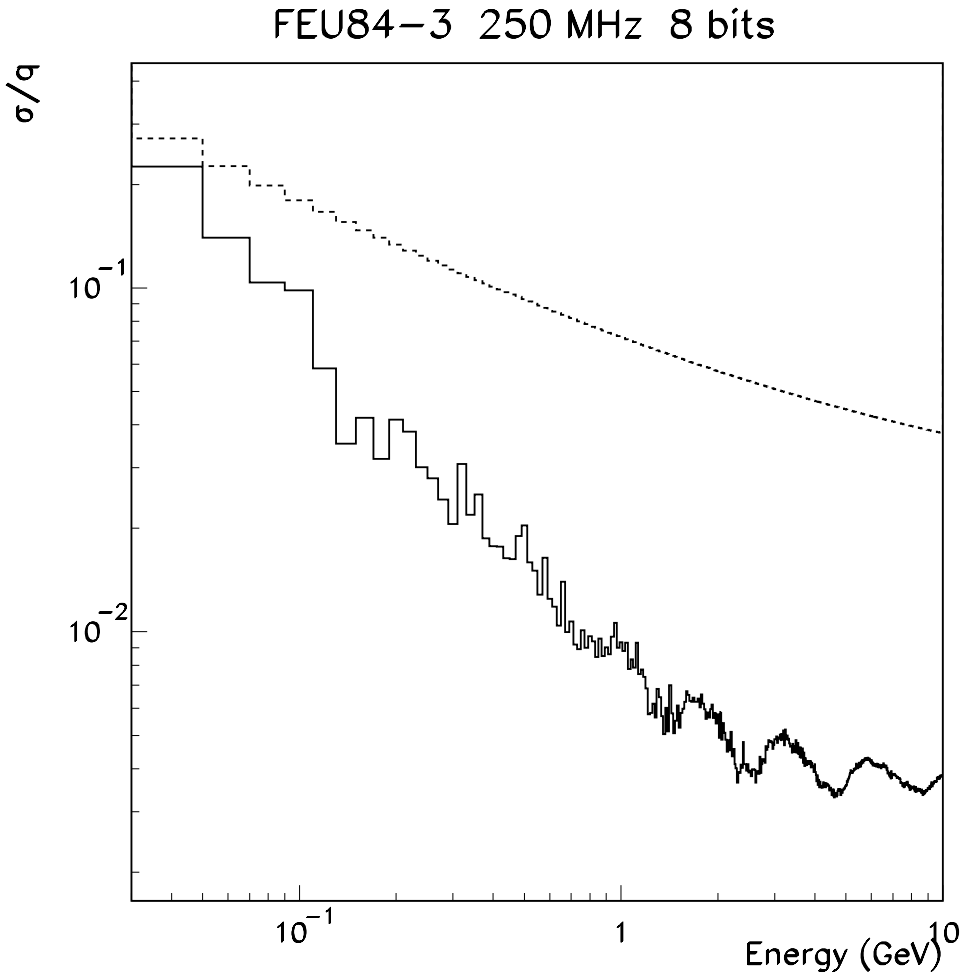
FEU84-3



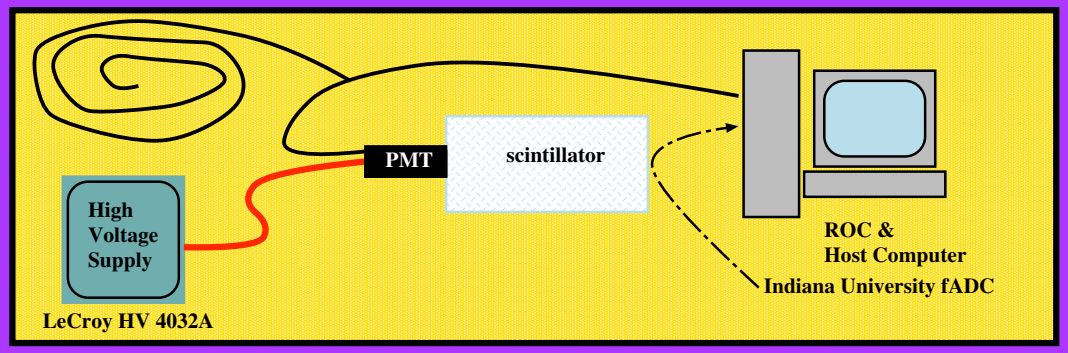
XP2020

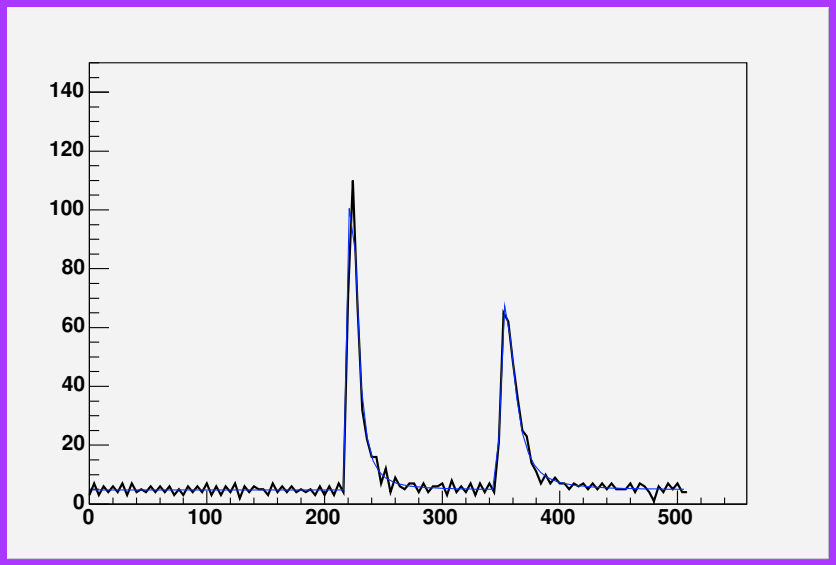


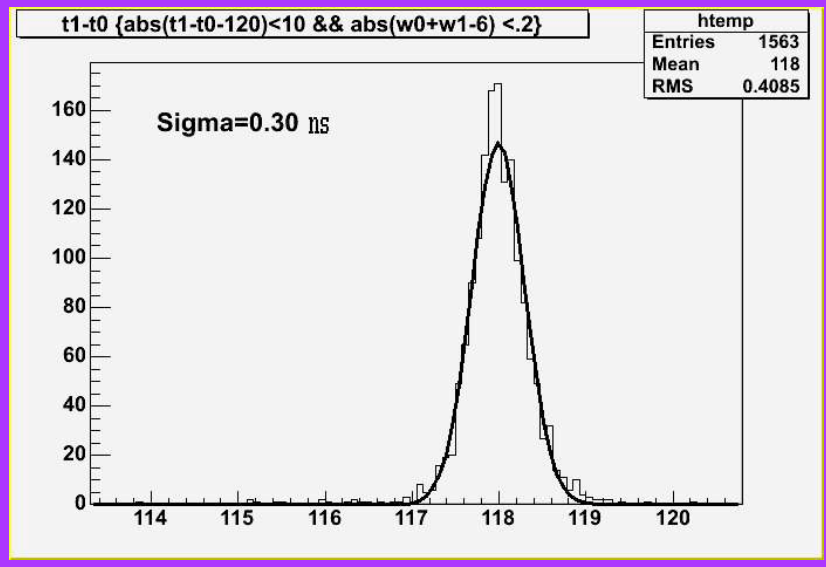



FEU84−3 250 MHz 8 bits
σ/q
10^{-1}
10^{-2}
10^{-1}
1
10
Energy (GeV)

Timing - echo test

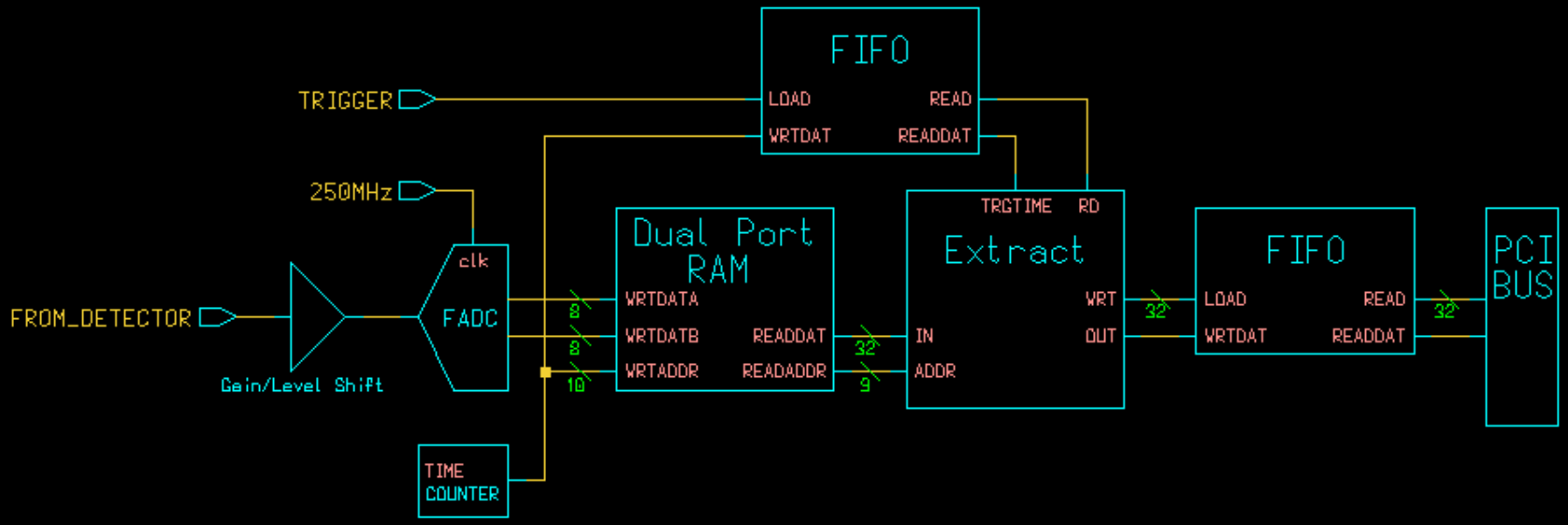






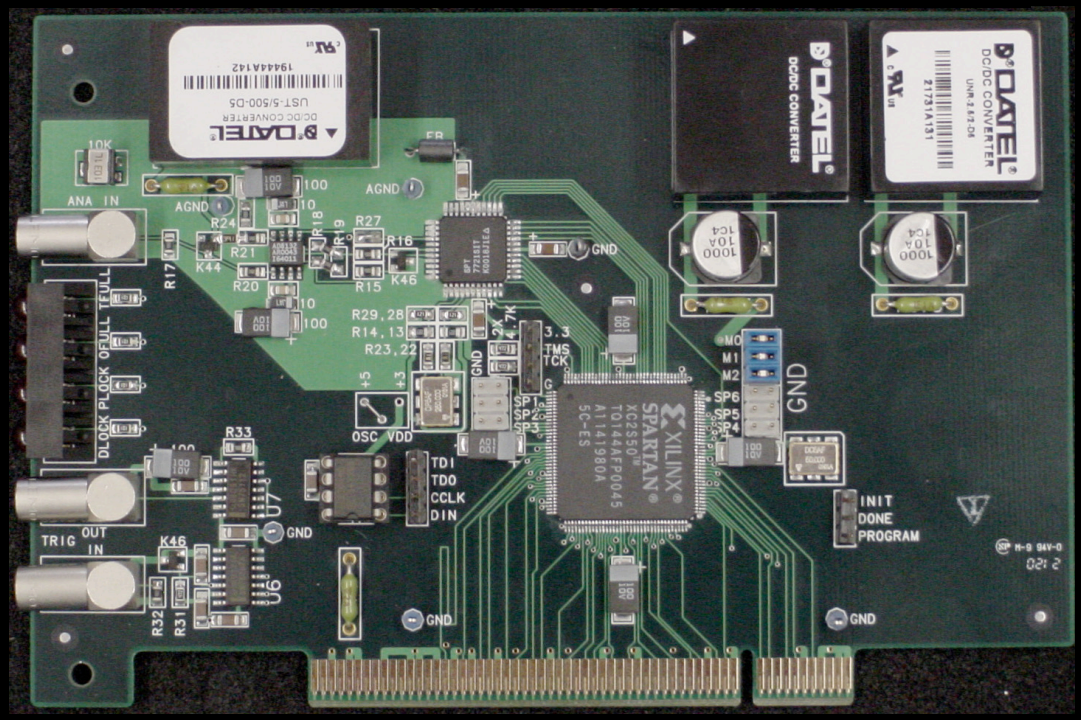
Timothy Paul Smith
Dartmouth College

Single channel FADC prototype

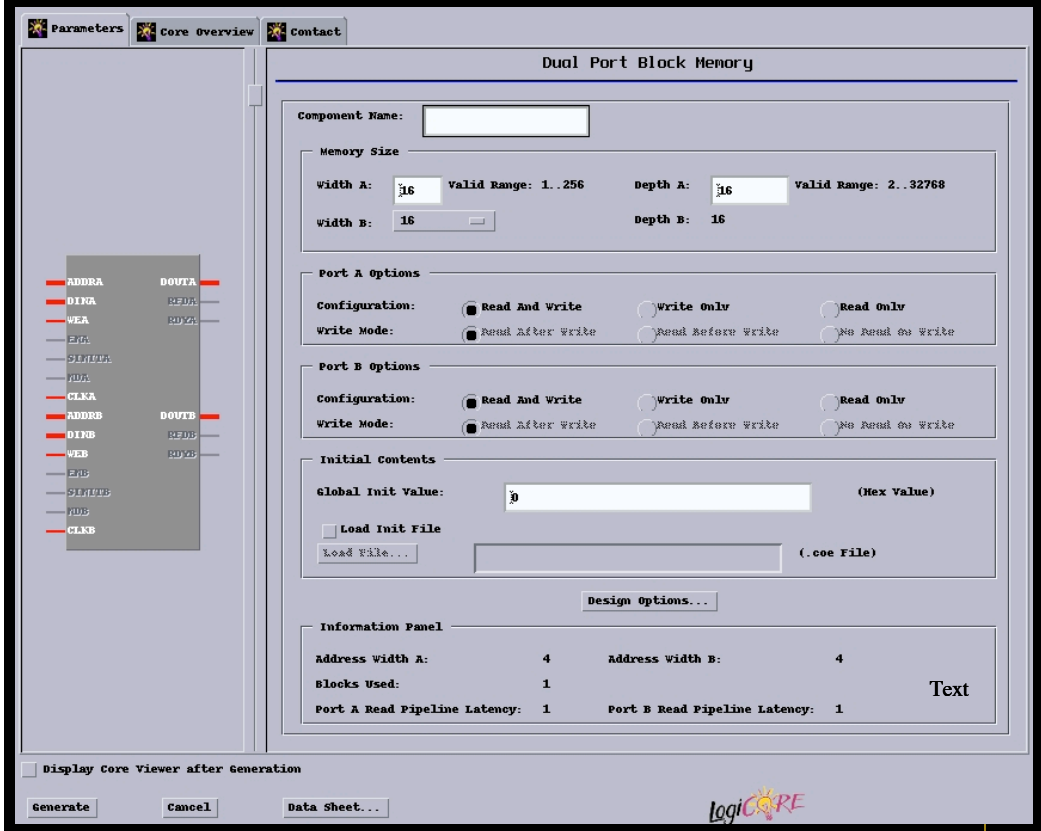


Test bed for:

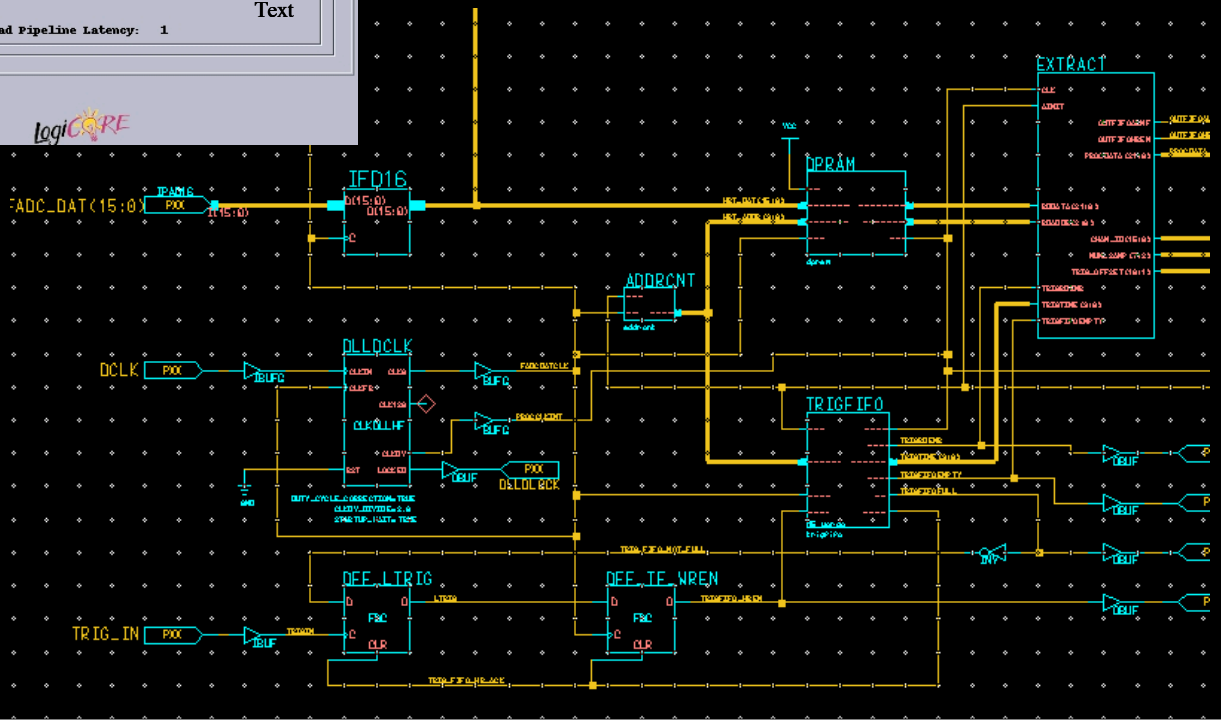
- SPT converter chip
- Xilinx chip and software
- Mentor PCB & FPGA software
- Intellectual Property (PCI core)
- Robotic assembly

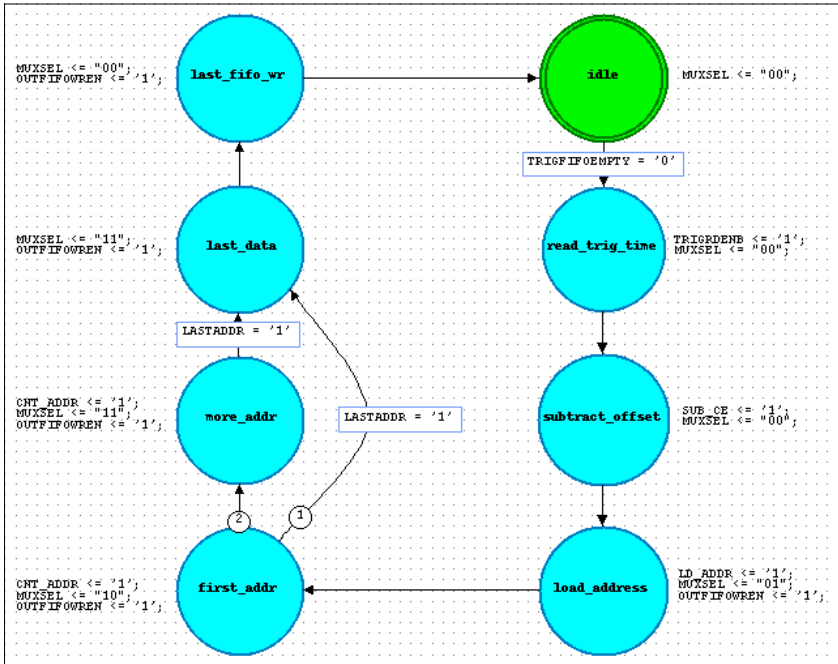


Indiana University

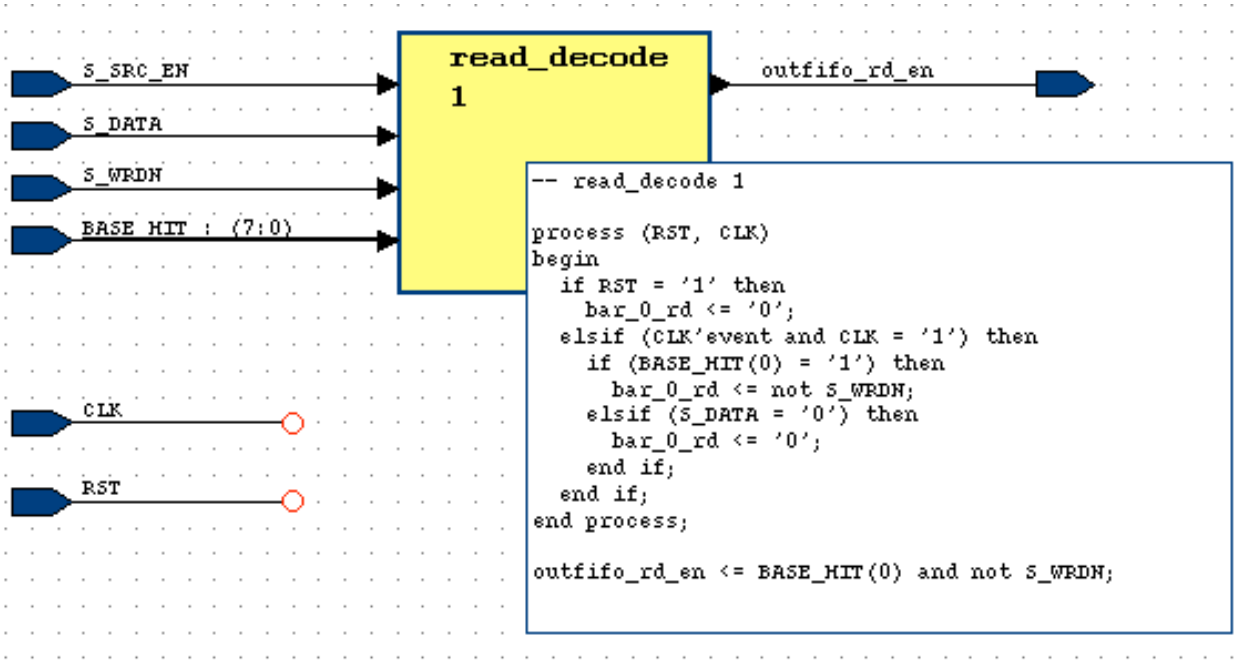


Xilinx schematic

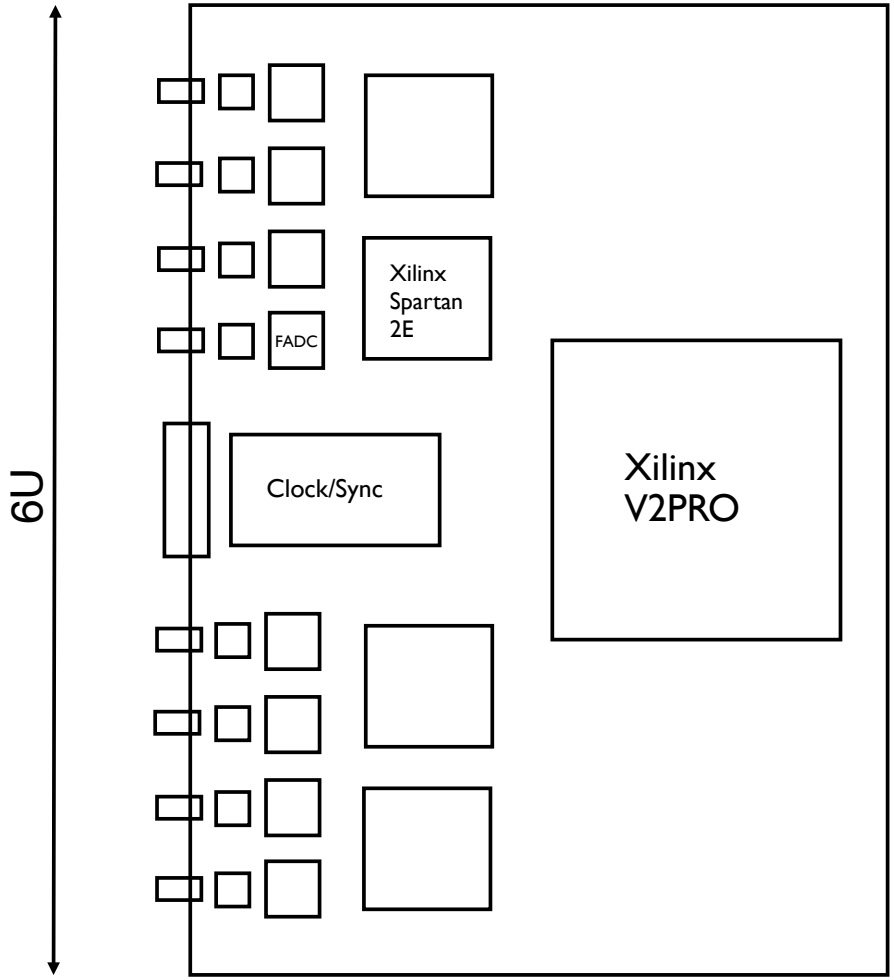




Mixed VHDL & Graphics

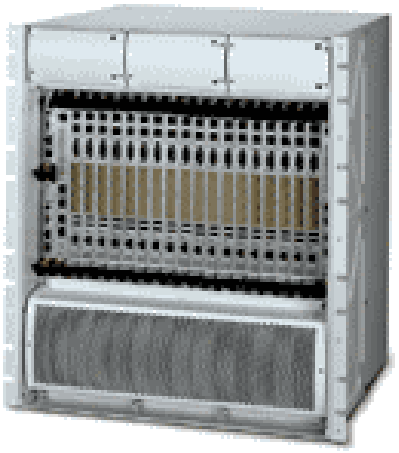


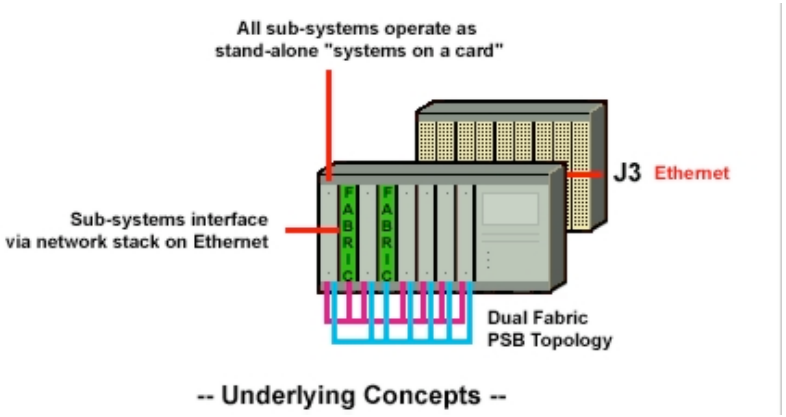
Next (final?) version



Energy sum
12 bits @ 125 MHz

Ethernet

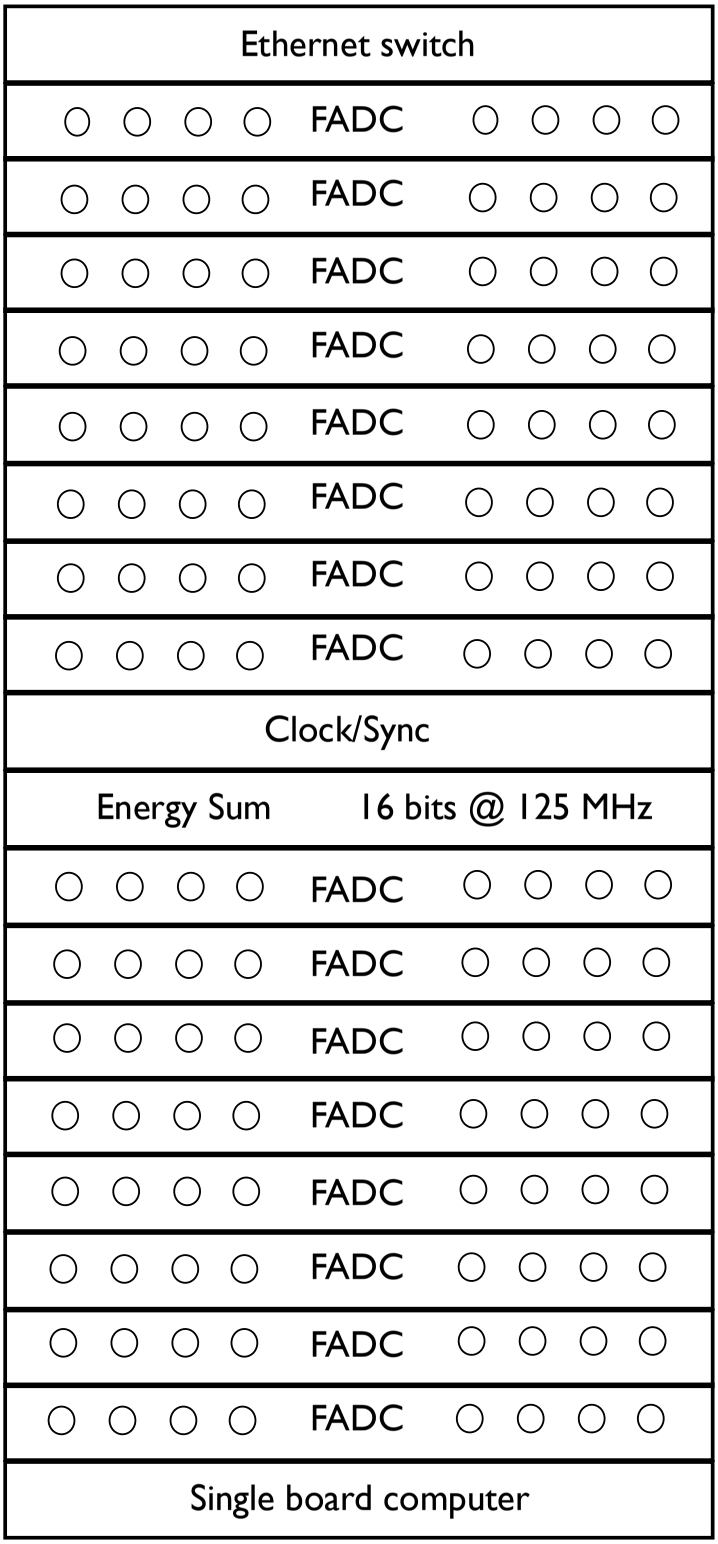




-- Underlying Concepts --

From the review:

- The general concept of local sums at the front-end board level, followed by crate-level sums and subsequent transfer to a central “Global LVl-1” processing area, is sound. A concept and proof-of-principle for crate backplane operation at the required high rate needs to be developed for the CDR. If high-speed serial operation proves challenging, the collaboration should explore possible parallel concepts to lower the bus-speed requirements.



Possible Crate Layout