Clock and Trigger Distribution

(Hall D Electronics Workshop – 12/07/04, EJ)

Synchronous Pipelined Data Acquisition System

- Sections operating up to 250 MHz
- All channel pipelines of the system should be clocked at the same time
- All pipelines of the system should be enabled for clocking on the same clock interval
- Accomplishing these allows the detector data samples to be correlated across the entire system.

Clock Distribution and Synchronization

Consider 2 signals: clock and reset

- Each front-end board has a counter that is incremented by clock.
- Count is held at zero while reset is asserted; counting is enabled when reset is unasserted.
- Counter value is used as the address in memory where the data sample is stored and serves to locally time stamp the data.
- Counter on every board in the system enabled to begin counting on the same clock edge so that all data fragments are properly aligned.
- Once this initial alignment is achieved, we must be able to monitor the system to assure that alignment is maintained.
- One way to monitor the alignment is to record the counter value when each trigger signal arrives. The local trigger times from the different pipeline elements can be compared as the data is being assembled to be sure no shifts have taken place.

- Centrally located master clock module generates a low frequency (e.g. 62.5 MHz) clock signal.
- The asynchronous reset signal is synchronized to the master clock in this module.
- Both the low-frequency clock and the synchronous reset are fanned out and are sent to each crate in the system.
- Each crate contains a local clock distribution board.
- A programmable delay element is inserted at the clock and reset inputs of the crate distribution card. This allows for a fine adjustment of timing at the crate level.
- For crates containing high speed pipelines (Flash ADCs), a local 250 MHz clock signal is generated from the low-frequency input clock using a Phase-Locked Loop (PLL) circuit.
- The PLL guarantees phase alignment of the 250 MHz clock with the input clock.
- The 250 MHz local clock and the reset are fanned out and are sent to each module in the crate.
- For crates containing lower speed pipelines (F1 TDCs), a local PLL circuit would divide the master clock frequency by 2 (31.25 MHz).

- Fan out of the clock and reset signals on the master clock module, the crate distribution board, and the front-end boards is done using low-skew (50-100 ps) fan out buffers and employing careful layout techniques (e.g. equal length traces).

- Distribution of the signals to modules within a crate may be done using short (<1 ft), matched, high-quality coaxial cables.

- Since the master clock module and front-end crates may be 100 feet apart, the use of fiber-optic links is desirable in this level of distribution.

- Care must be taken not to introduce significant jitter into the signals here.

Trigger Distribution

- A trigger signal must be distributed to the front-end electronics.
- The trigger signal is assumed to have a fixed latency relative to the physics event.
- When a trigger signal arrives at a front-end module, the relevant section of data in the pipeline (earlier time) is transferred to a buffer for readout.
- Whenever any local readout buffer is approaching a full state, trigger signals must be halted until sufficient storage is available.
- The front-end module communicates this ‘almost full’ state to the trigger system by the assertion of a busy signal.
- The collection of busy signals from all modules is here considered part of the trigger distribution system.
- Additional trigger information (e.g. trigger type) needs to be conveyed to the read-out-controllers.

- We are currently investigating the integration of the clock and trigger distribution systems into a common high-speed serial network.

- Such a system could be based on the G-link chip set (Agilent HDMP-1032A/1034A) and appropriately chosen fiber optic transceivers.

- G-link is a virtual ribbon cable interface for the transmission of data.

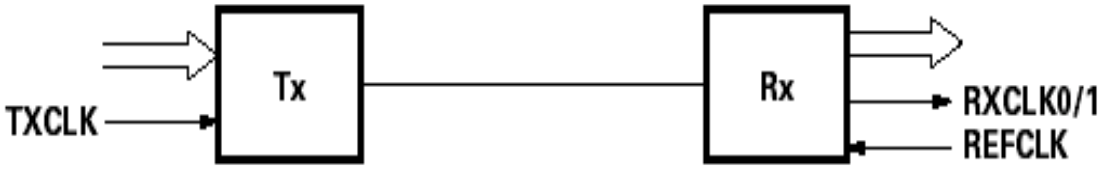
- 16-bit parallel data (a frame) loaded into the transmit chip (Tx) is delivered to the receiver chip (Rx) over a serial channel (fiber) and is reconstructed into its original parallel form.

- The serial link is synchronous. Frames may be clocked into the Tx chip at a rate of 13 MHz to 70 MHz .

- The link (Tx,Rx) has a short and fixed latency (4 clock cycles). The frame clock is recovered from the serial data stream by the Rx chip.

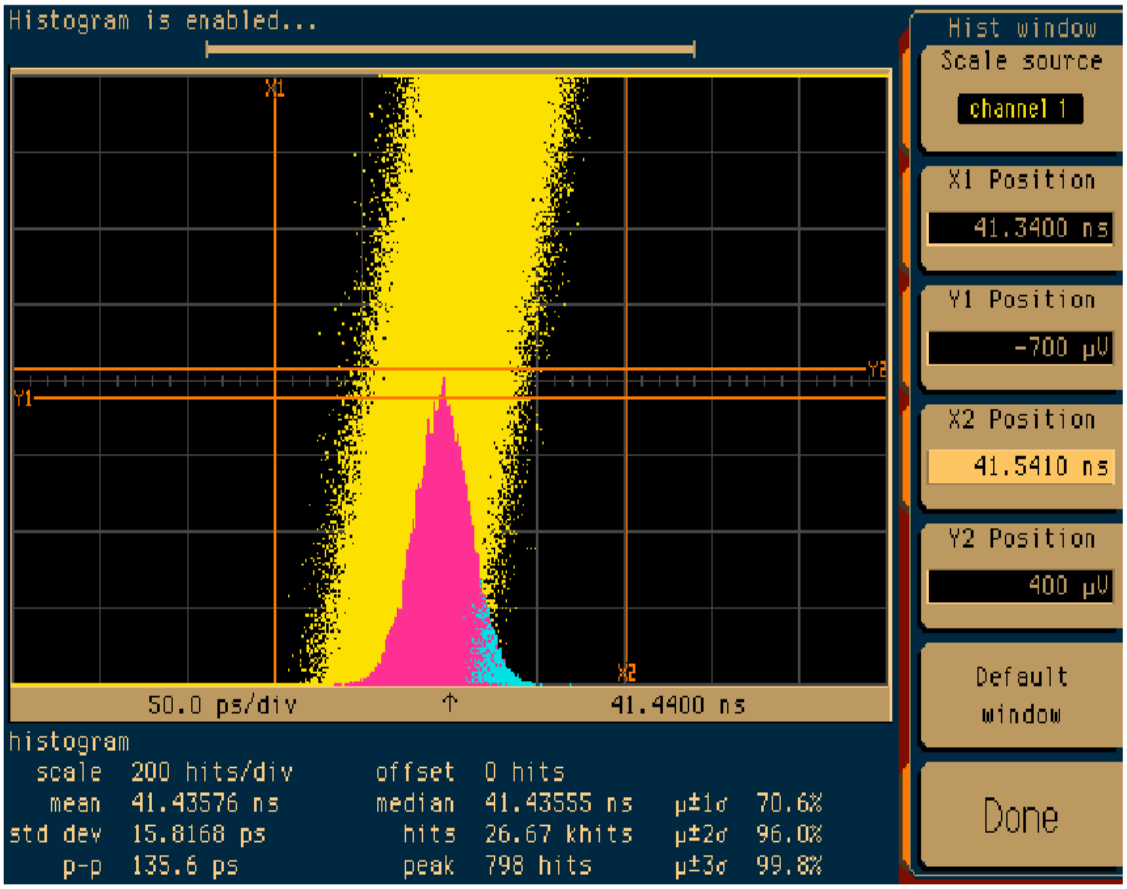
- Measurements by Agilent demonstrate that the recovered clock has very low jitter – less than 15 ps when the channel is a short copper interconnect.

G-link



A) 16 BIT SIMPLEX TRANSMISSION

Random Jitter (RJ) of the HDMP-1034 Recovered Clock at RXCLK#1



HEWLETT PACKARD

- In our application individual G-links connect the master clock module to each crate distribution board.

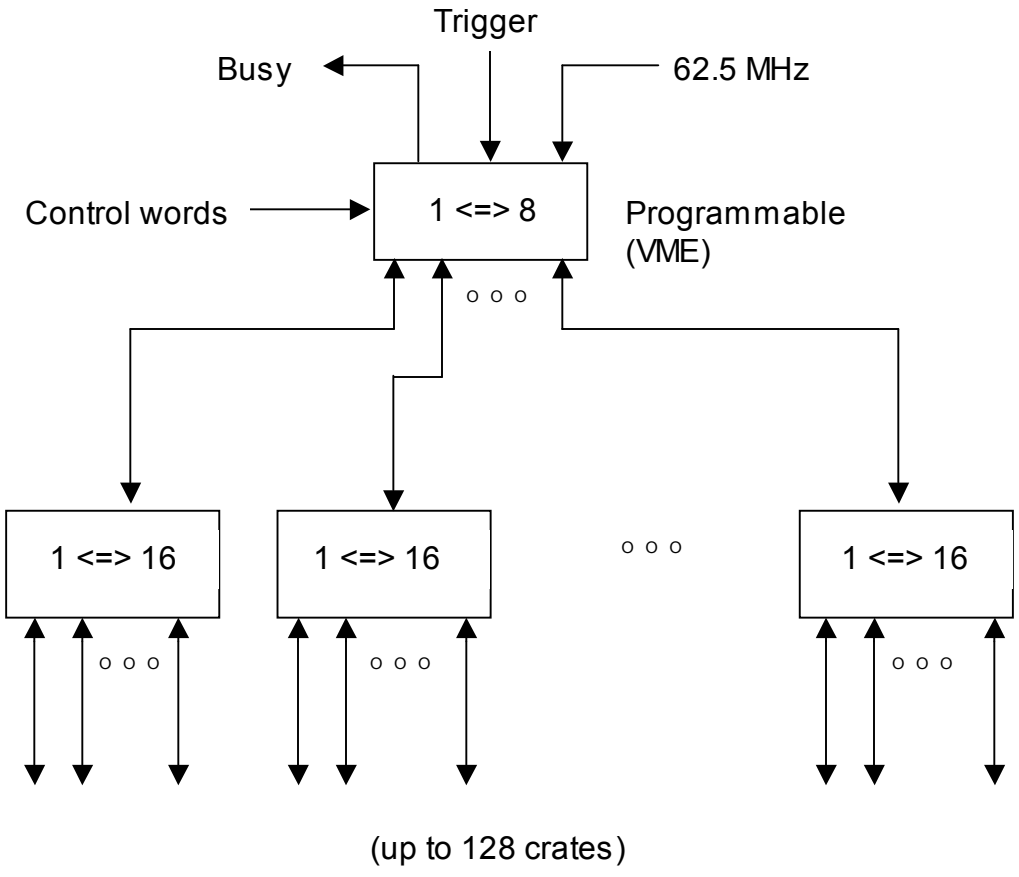
- The master clock serves as the frame clock for each Tx chip, and the Rx chip in each crate recovers this clock.

- Reset and trigger patterns are specified as unique data words transmitted, and are synchronized to the clock at each Rx.

- Many other “control events” could also be broadcast as unique data patterns to the crates.

- Reverse links would carry the busy signals as well as other status information back to the trigger system.

G-link Clock & Trigger Distribution



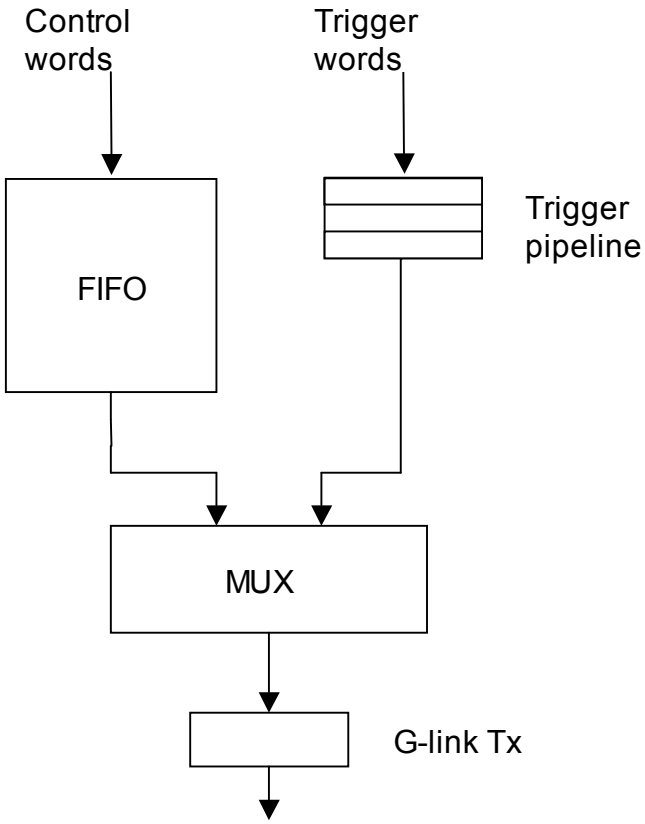
(up to 128 crates)

Some implementation details

- Trigger words may be issued at 16 ns intervals (master clock = 62.5 MHz).

- Trigger words are time critical – must be transmitted promptly to maintain fixed latency.

- Control words (reset, etc.) are not time critical – they can be queued in a FIFO and sent in any G-link frame not used by a trigger word.



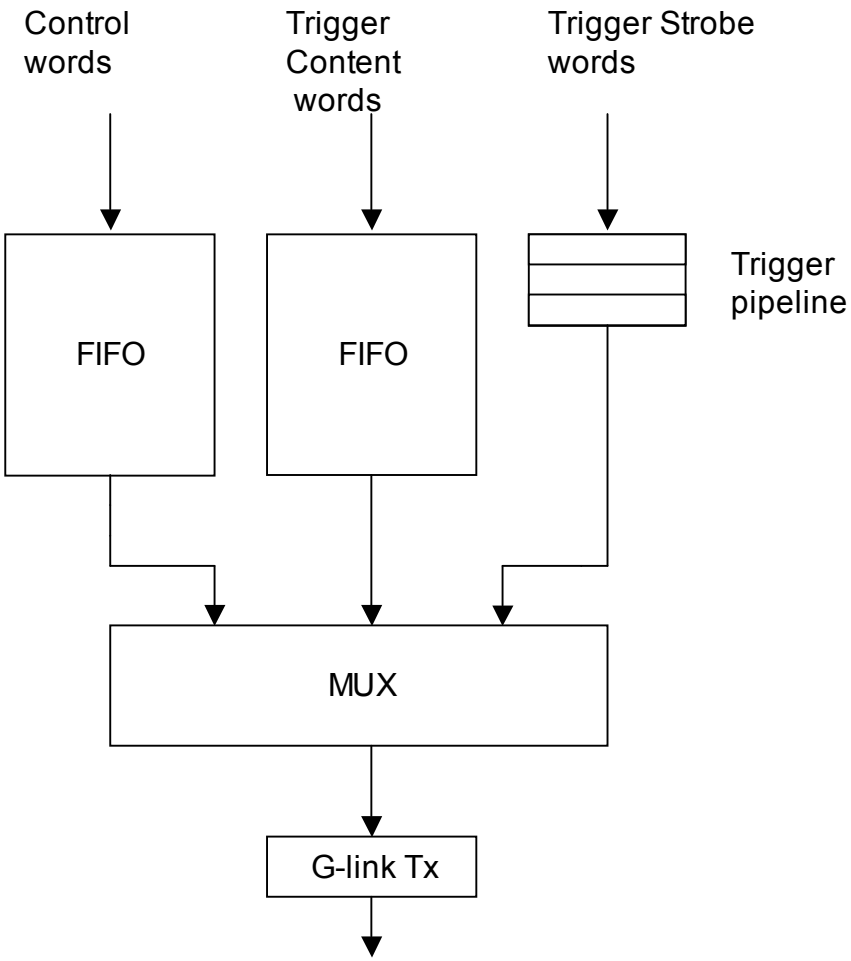
- Information flowing backwards from the front end crates (busy, status, etc.) is not time critical, and is multiplexed onto a single G-link (16 => 1)

- In the simplest implementation, 15 bits (16 – 1 tag bit) are available for trigger information to the ROCs.

- If this is not enough, we can split trigger information across several words.

- Trigger data:
  (1) Trigger strobe word - time critical
  (2) Trigger content word(s) - not time critical

- Like control words, the trigger content words can be queued in a FIFO and sent in any G-link frame not used by a trigger strobe word.


Control words
Trigger Content words
Trigger Strobe words
FIFO
FIFO
Trigger pipeline
MUX
G-link Tx

Possible problems distributing clock by G-link

- Jitter :
  - G-link Tx-Rx chipset – negligible (15 ps)
  - optical transceivers (??)
    ex. Finisar FTRJ8519F1 (<65 ps typical)
    (2.125 Gb/s, 850 nm)

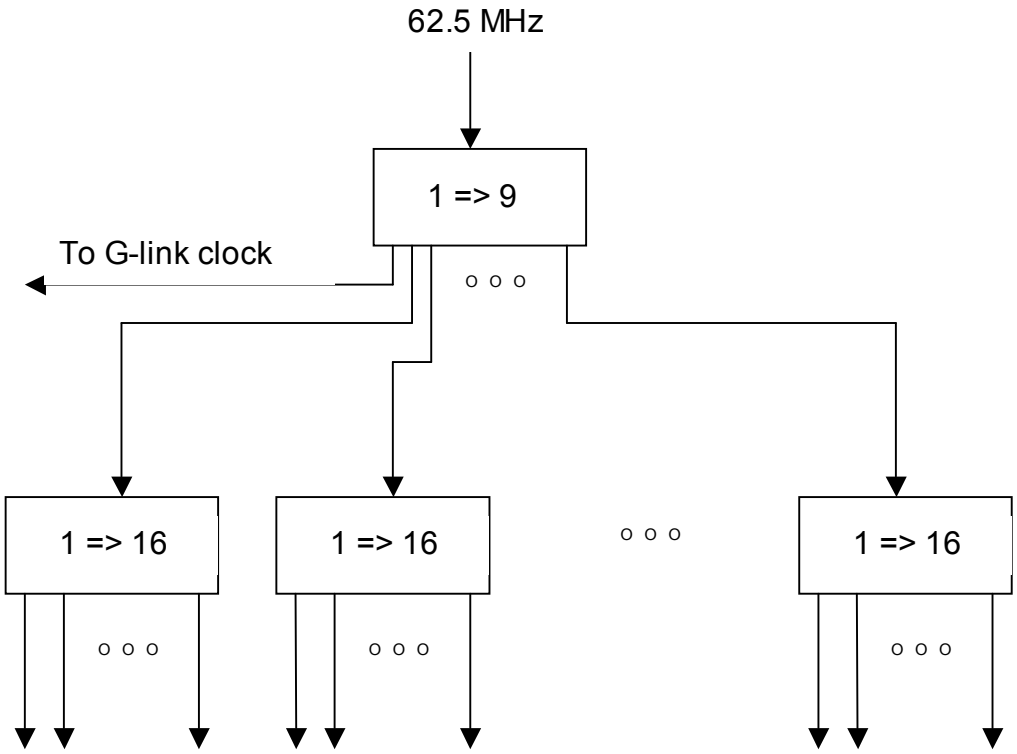
- Jitter in clock distribution is bad for F1 TDCs. Internal reset of time (synchronous mode) occurs on a clock edge. Clock jitter will degrade crate-to-crate timing resolution.

- Timing extracted from FADC data is much less sensitive to jitter (4 ns bins ~ 1 ns resolution).

Alternate Clock Distribution Scheme

- Fan out and distribute clock (62.5 MHz) using differential PECL or ECL levels on high quality twinax cable (e.g. Alpha 9818C)
- AC coupling at intermediate and final destinations.
- Tie shielding of cables to ground only at source end.
- Ground loops are eliminated.
- Signals were observed to be very clean after ~200’ of Alpha 9818C cable.
- Minimal jitter introduced by cable – we used it to test F1 TDC resolution.
- Use top level output to clock G-link trigger/control distribution network (optical).
- Trigger & control words arrive at crates synchronized to sampling clock.

Clock Distribution by Copper Cable



(up to 128 crates)