JLab High Resolution TDC

Hall D Electronics Workshop (12/04)

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Data Acquisition

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- Project started as an effort to test and understand the performance of the F1 TDC chip for use in Hall D

- The need to find an alternative to Fastbus based high resolution TDCs motivated the expansion in scope of the project

- The first prototype has been working since Sept ’02 – with a few small fixes and additions it will become a useful module in current experiments

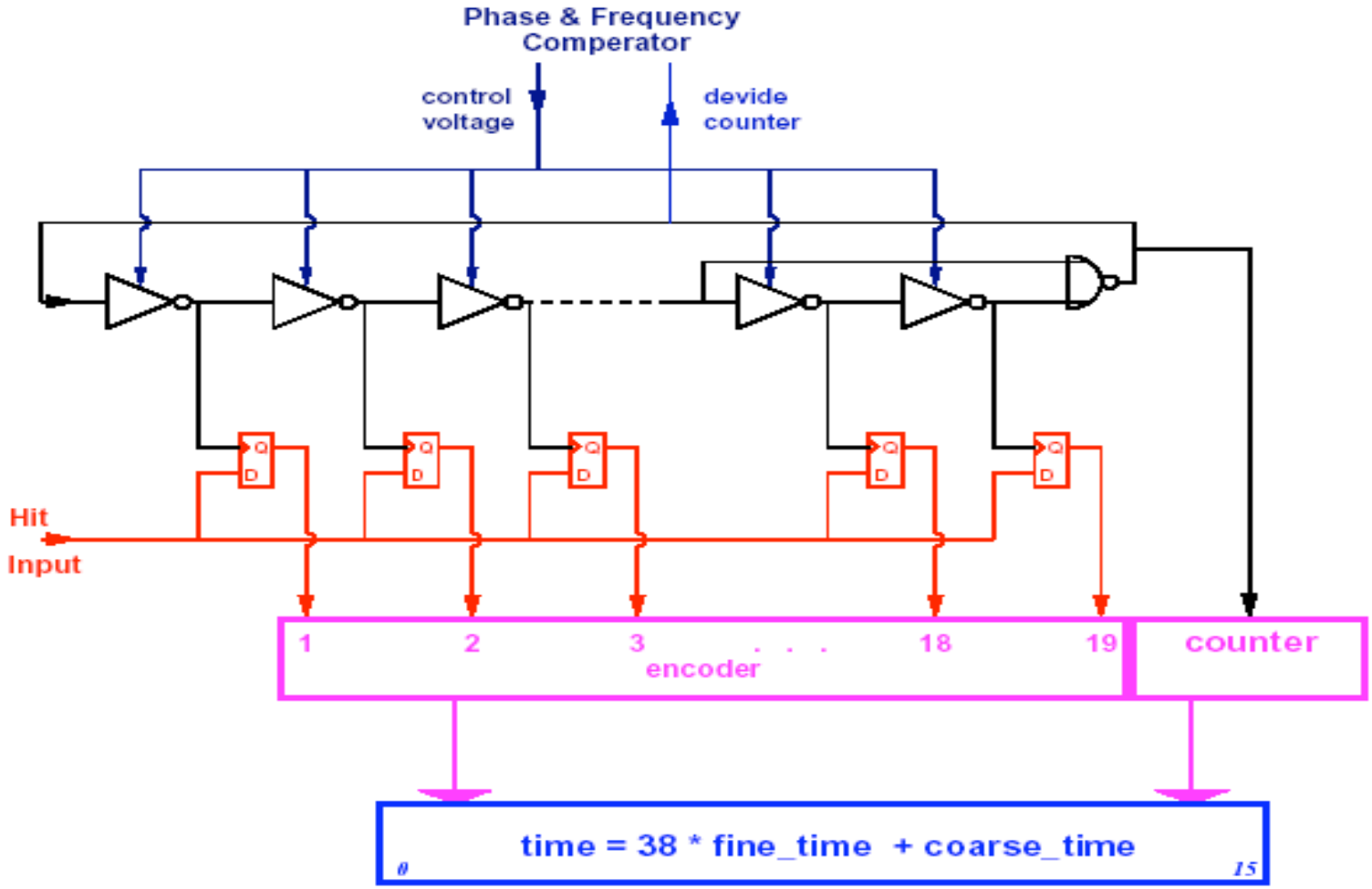
F1 TDC Chip

- Designed at the University of Freiberg for the COMPASS experiment at the CERN SPS
- COMPASS (COmmon Muon Proton Apparatus for Structure and Spectroscopy)
- Used for many different COMPASS detector systems (straws, dc, muon, mwpc, scifi, hodoscope…)
- In most cases the F1 chip is mounted on the COMPASS detector system, so reasonably low power consumption was an important design consideration
- Marketed by acam-messelectronic gmbh (Germany)
- Uses purely digital delay techniques to measure time
- Stability ensured by self adjustment of core voltage through a PLL circuit and external voltage regulator

F1 Chip Features

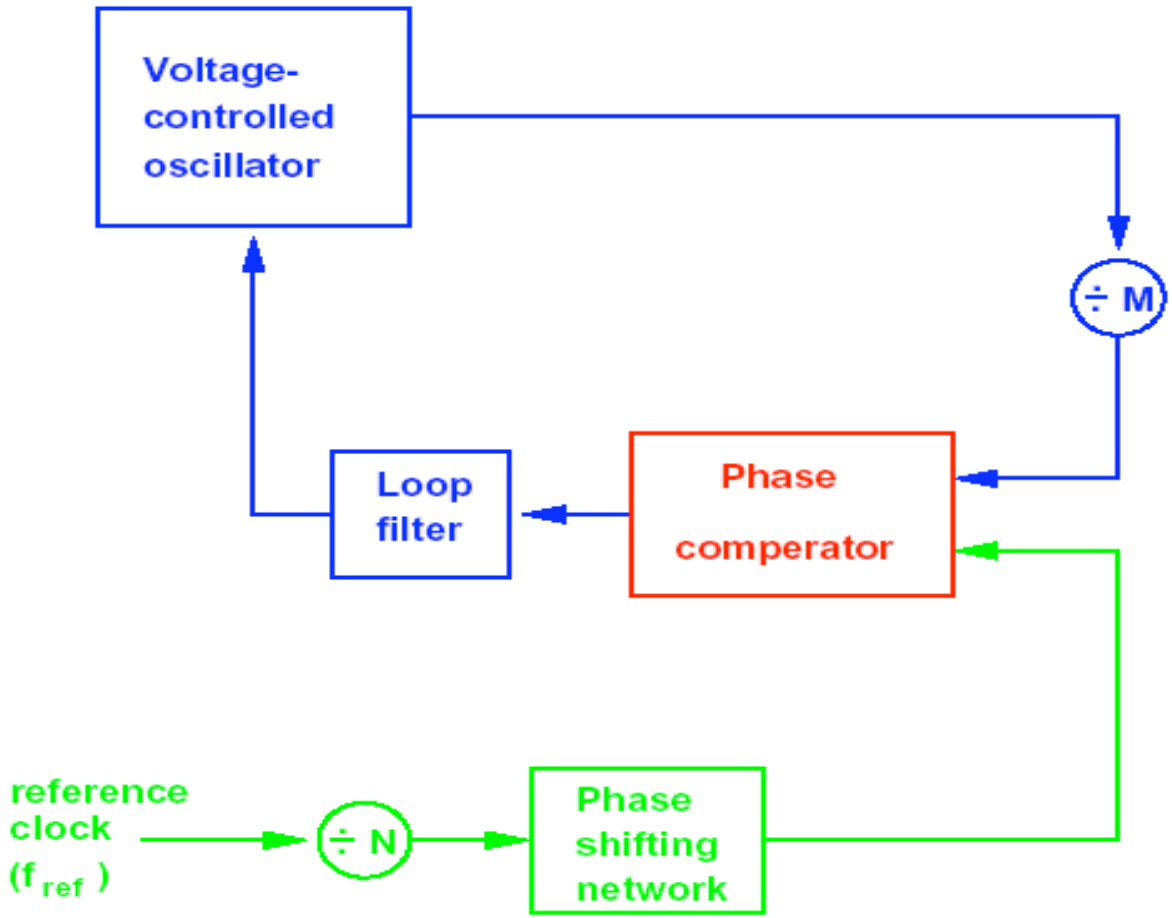
- 8 channels @ 120 ps LSB (normal resolution mode)
- 4 channels @ 60 ps LSB (high resolution mode)
- 16-bit dynamic range – 7.8 us @ 120 ps LSB, 3.9 us @ 60 ps LSB
- Multihit – buffers allow the storage of up to 16 hits/channel (32 for high resolution mode)
- Trigger Matching – allows for the selection of hits within a programmable time window and latency from the trigger signal
- Trigger buffering – up to 4 triggers may be stored for processing
- High rate capability – for trigger rates < 625 kHz, input hit rates > 4.4 MHz (normal resolution) or 7.2 MHz (high resolution) are possible

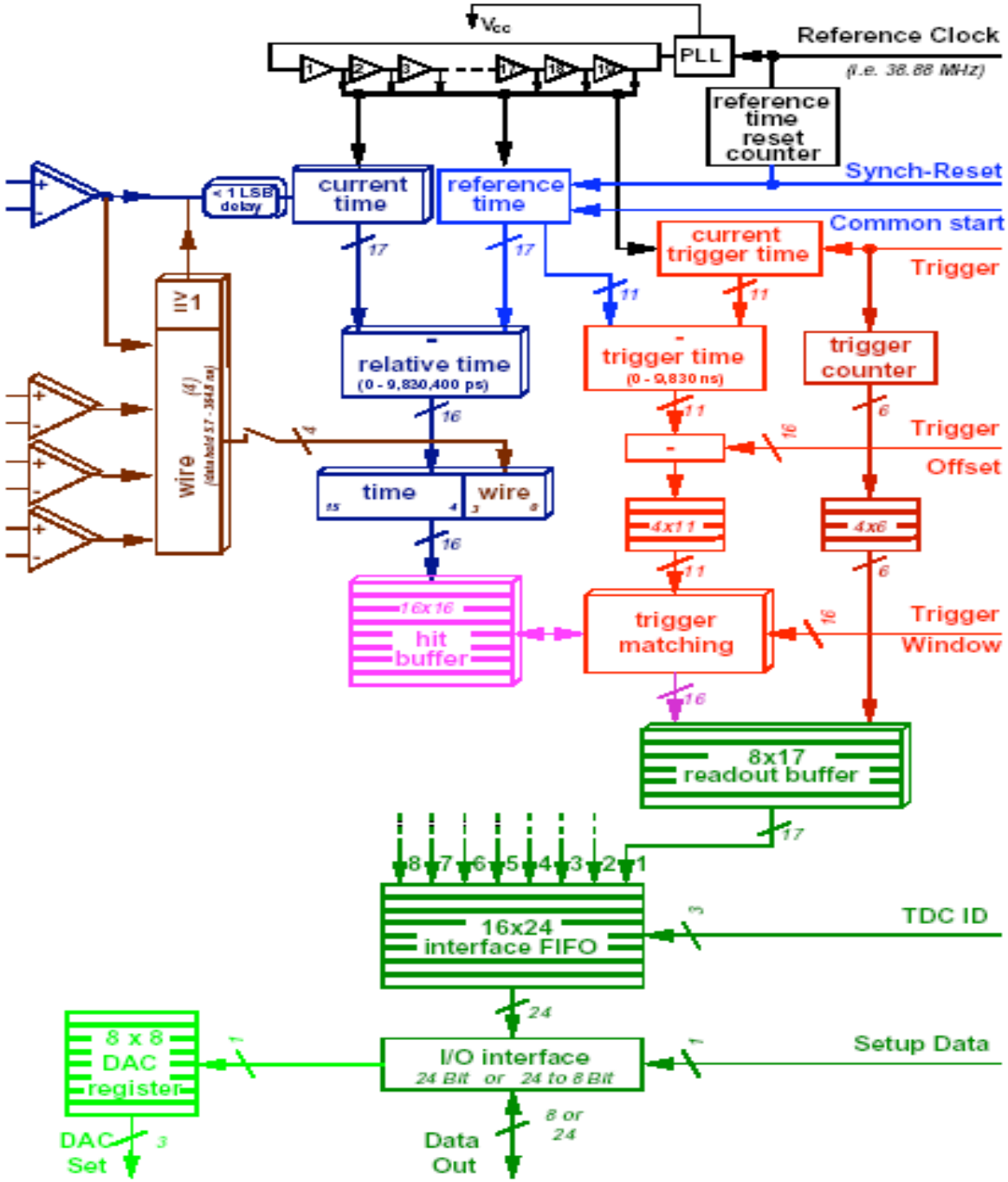
VCO for a fine- and coarse-time digitizing circuit



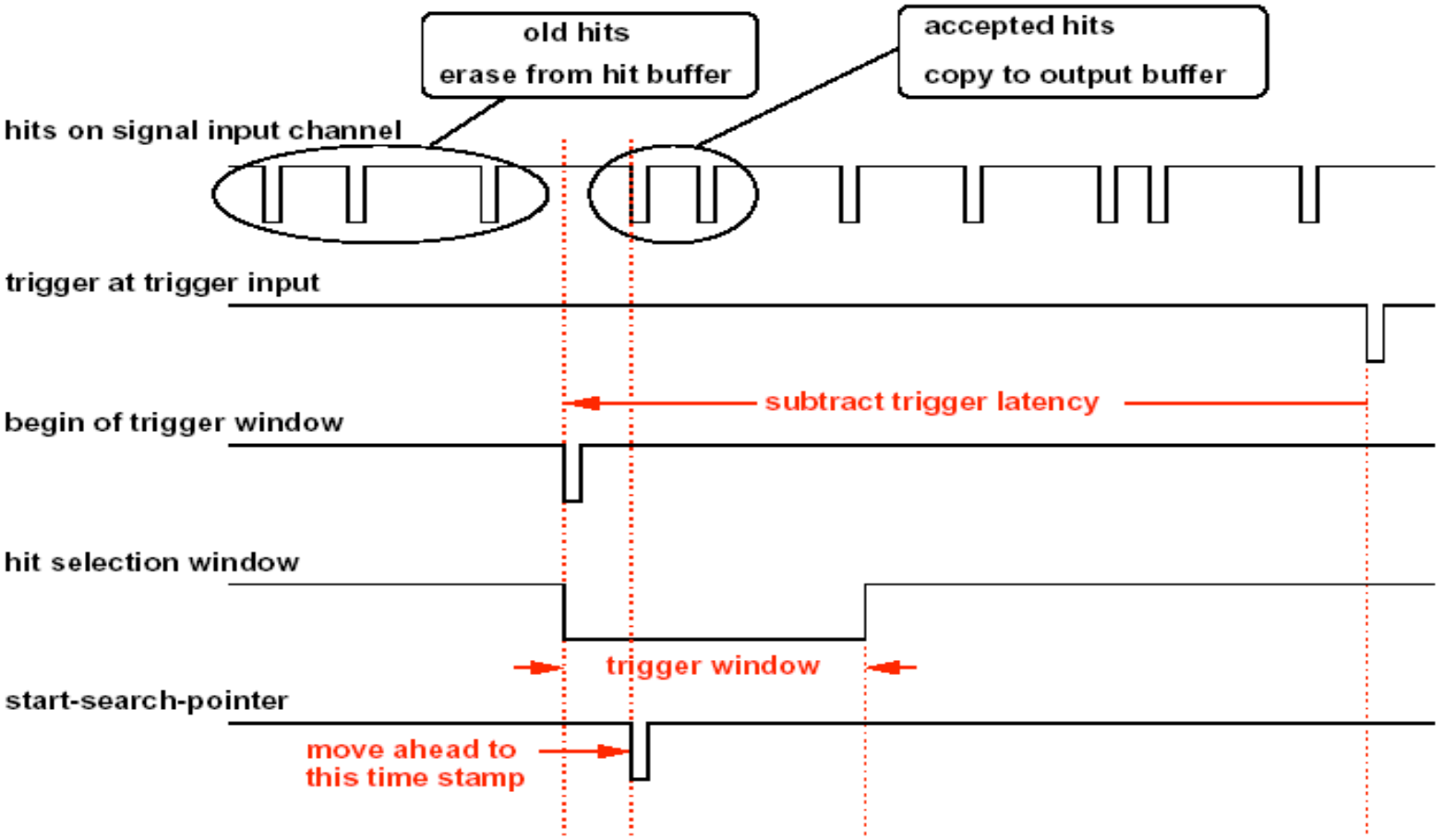
PLL based on an asymmetric ring oscillator and phase and frequency stabilization. PLL frequency is adjusted by the low (N) and high (M) frequency dividers.

$$f_{PLL} = \frac{M}{N} \times f_{ref}$$




Vcc
PLL
Reference Clock
(i.e. 38.88 MHz)
reference time reset counter
Synch-Reset
Common start
current time
reference time
< 1 LSB delay
current trigger time
Trigger
relative time
(0 - 9,830,400 ps)
trigger time
(0 - 9,830 ns)
trigger counter
Trigger Offset
wire
time
wire
4x11
4x6
16x16 hit buffer
trigger matching
Trigger Window
8x17 readout buffer
16x24 interface FIFO
TDC ID
8 x 8 DAC register
I/O interface
24 Bit or 24 to 8 Bit
Setup Data
DAC Set
Data Out
8 or 24

Trigger Matching Procedure



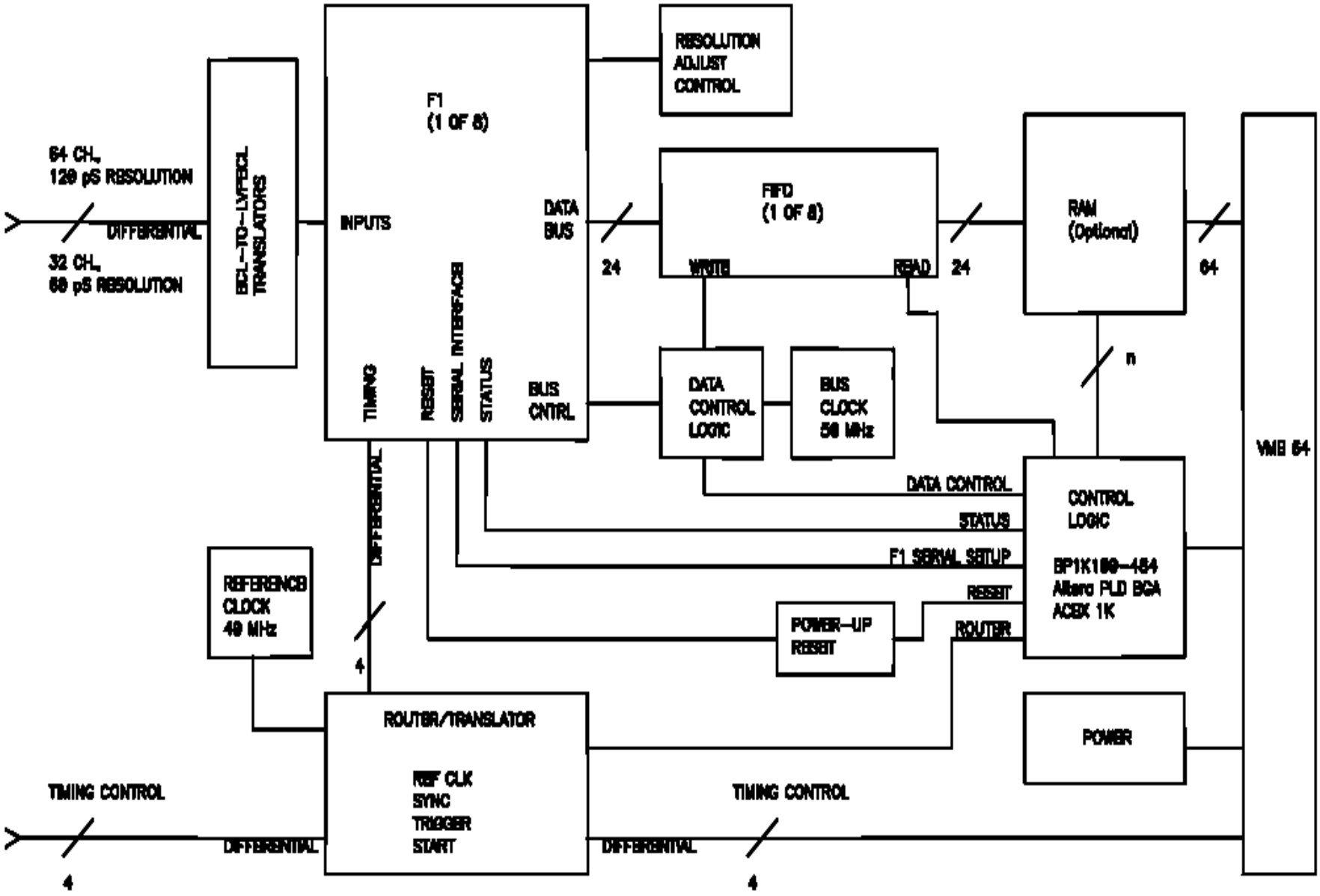
TDC Module Features

- 64 channels normal resolution, 32 channels high resolution
- 6U single slot VME64x slave – differential ECL inputs
- 128K word deep FIFO buffer for each F1 chip
- VME interface (64 bit) and control logic in a single FPGA
- FPGA has an internal 512 x 64 bit FIFO buffer
- Data from multiple chips that are associated with the same trigger are assembled into an event fragment
- Module can interrupt crate controller when a programmable number of event fragments are available
- A set of TDC modules may be read out as a single logical read using a multiblock protocol (token passing)
- On-board storage (non-volatile) and auto-loading of F1 chip configuration data

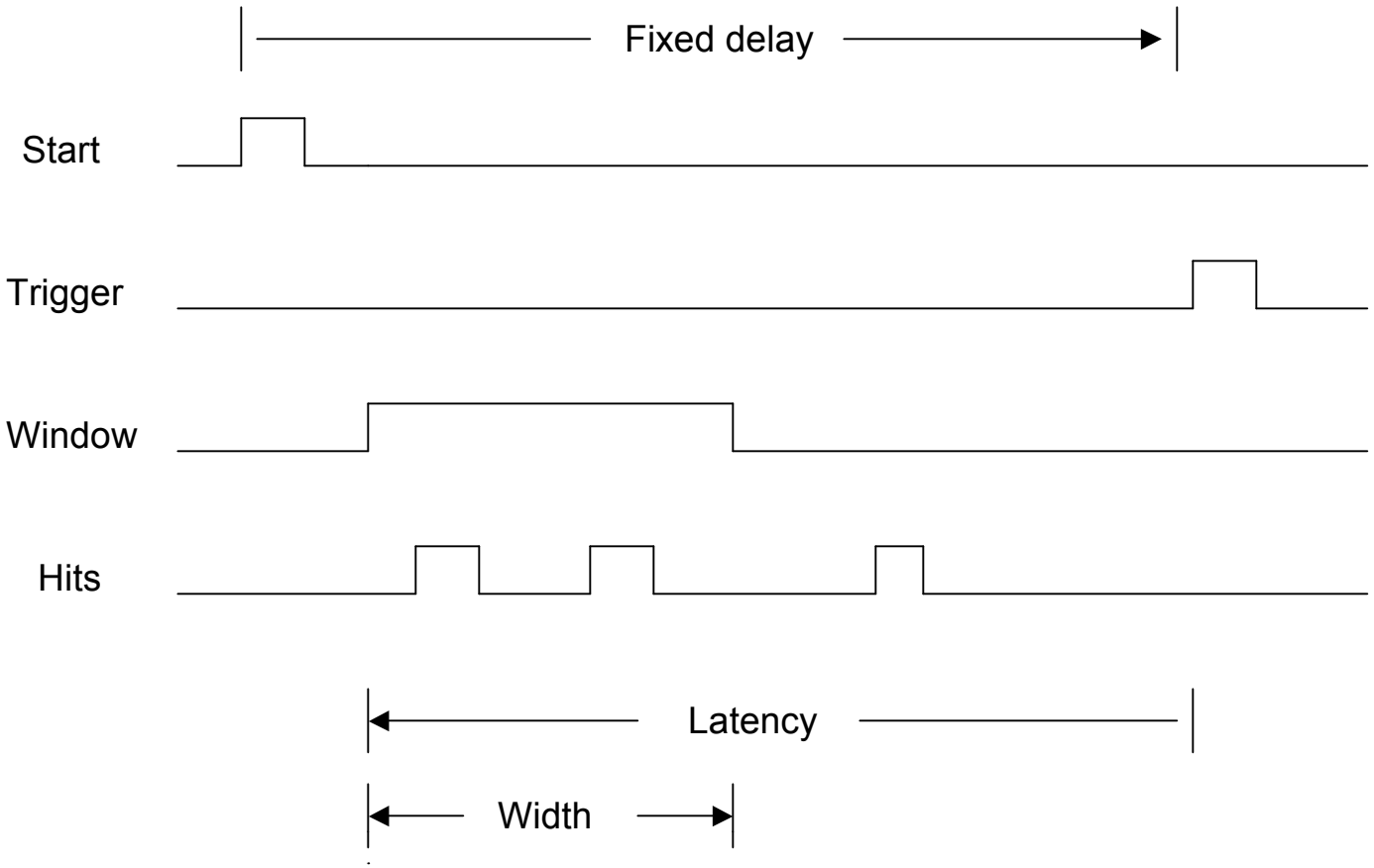
Implementation Details

- 12 layer printed circuit board – 5 mil traces/clearances
- Signal characteristics are preserved throughout the front end by use of differential PECL strip line routing (50 ohm)
- Components are surface mounted using both sides of the board
- FPGA is a single 484 pin BGA package
- 38 watts total power dissipation

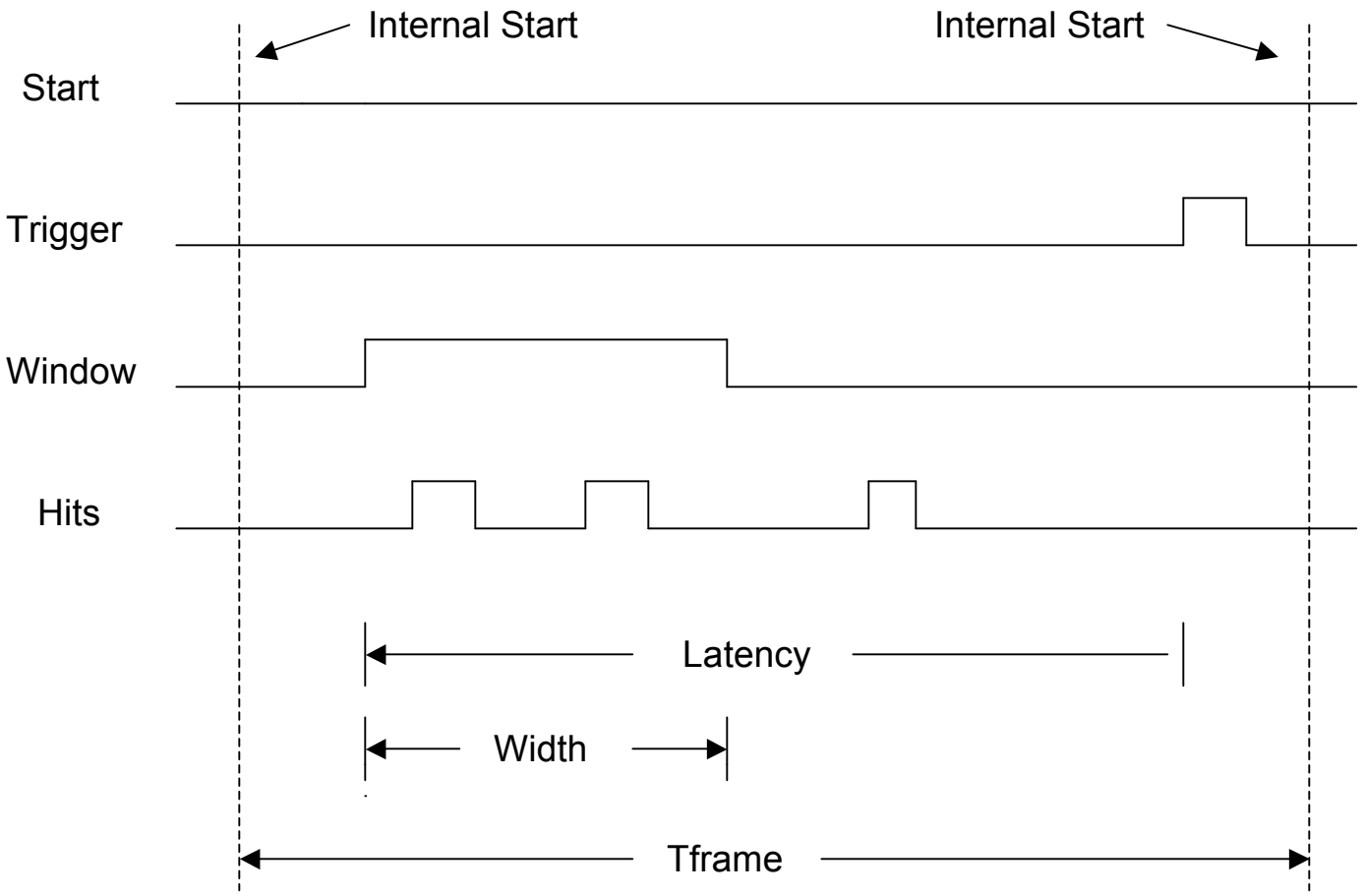
TDC Module Block Diagram



Non-synchronous Mode



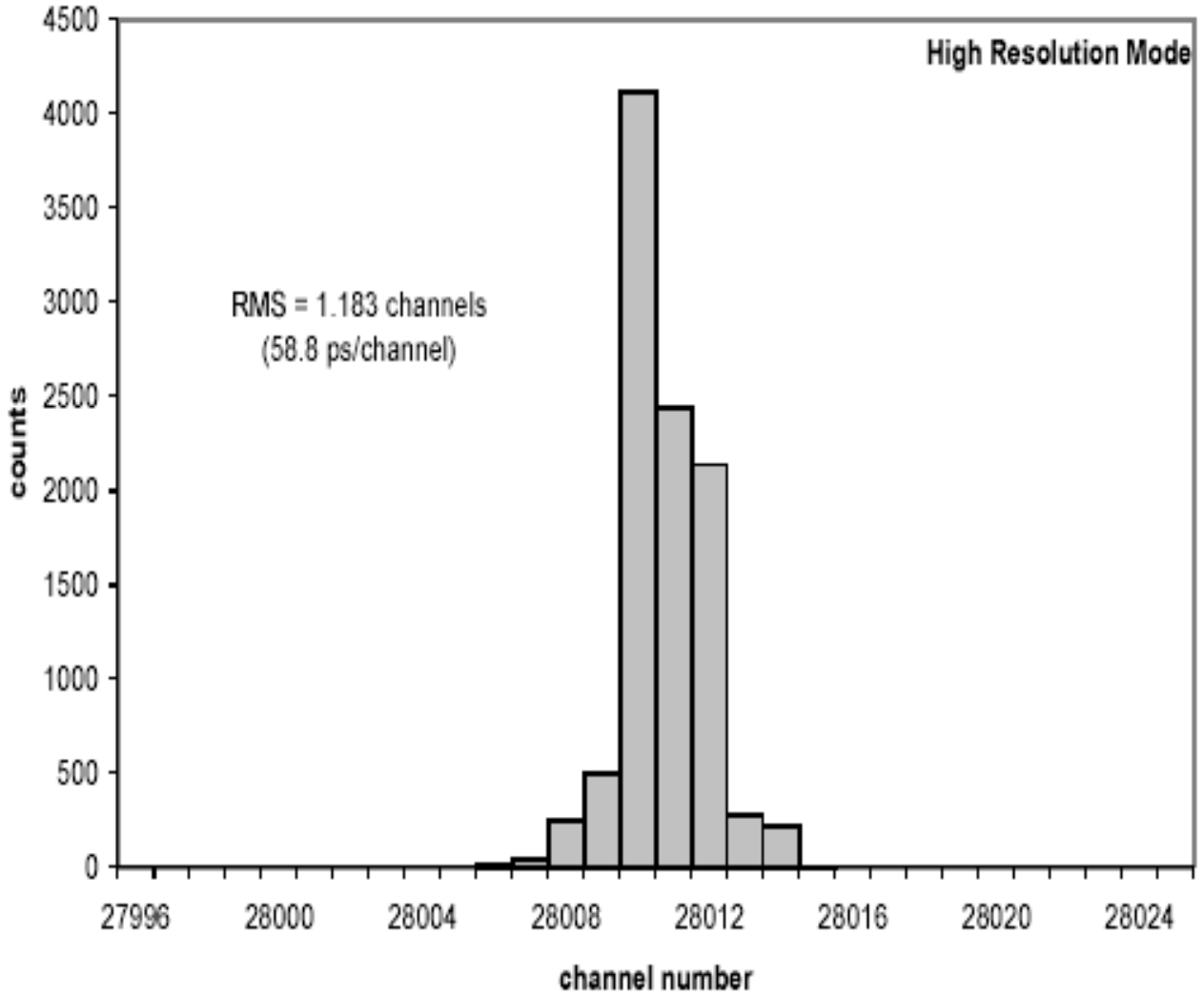
Synchronous Mode



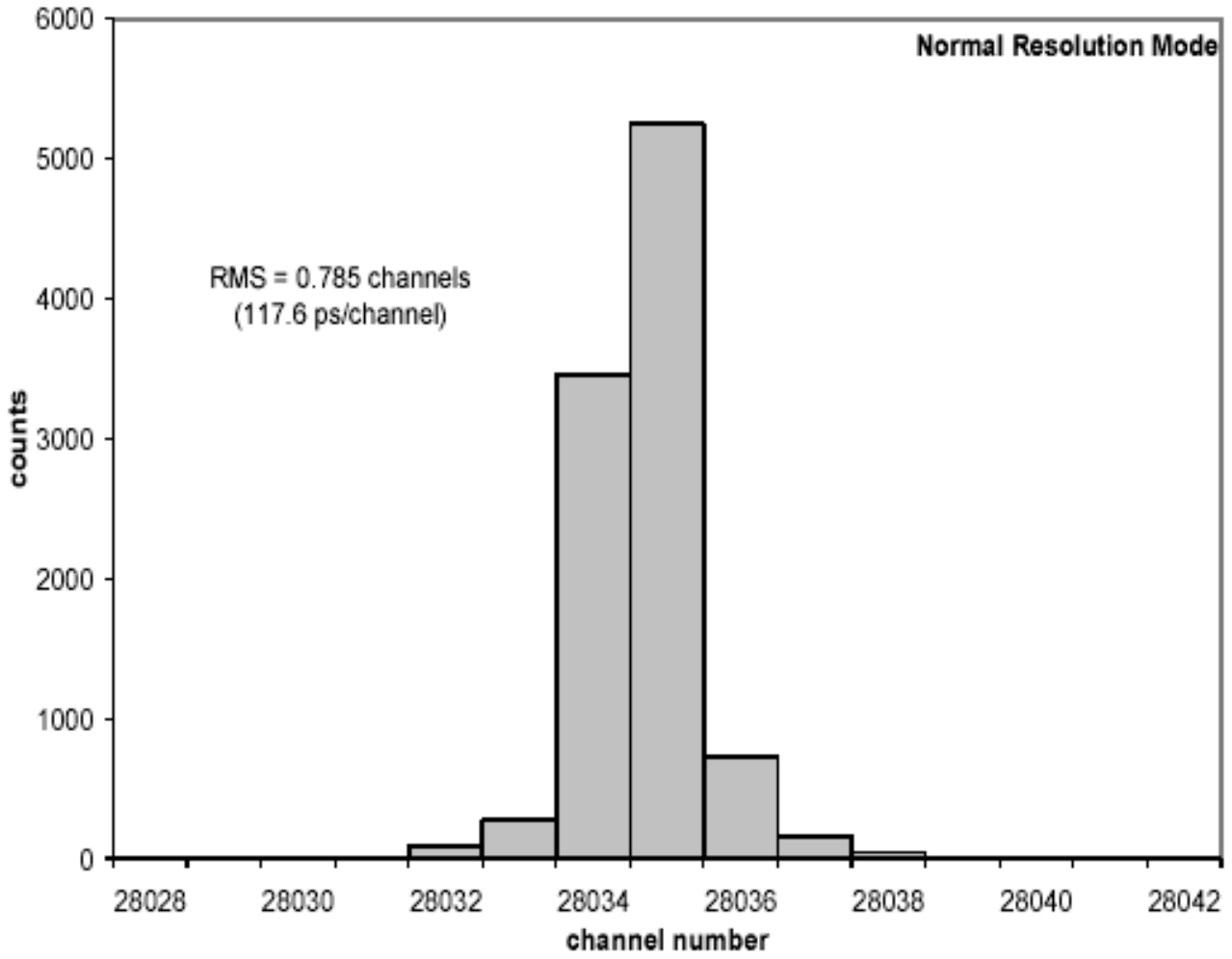
Tframe = N * 25 ns

Width < 0.4 * Tframe

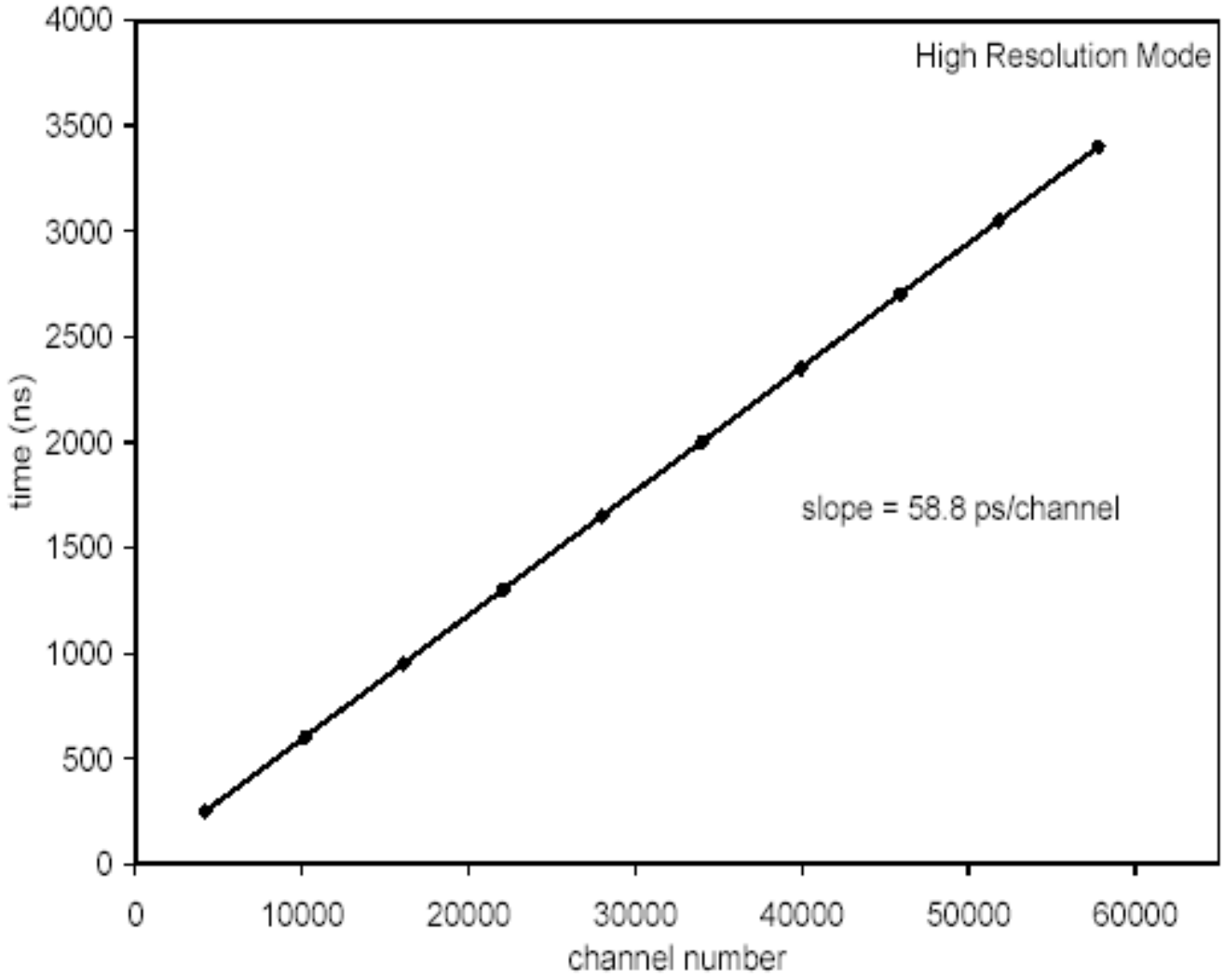
Latency < 0.9 * Tframe



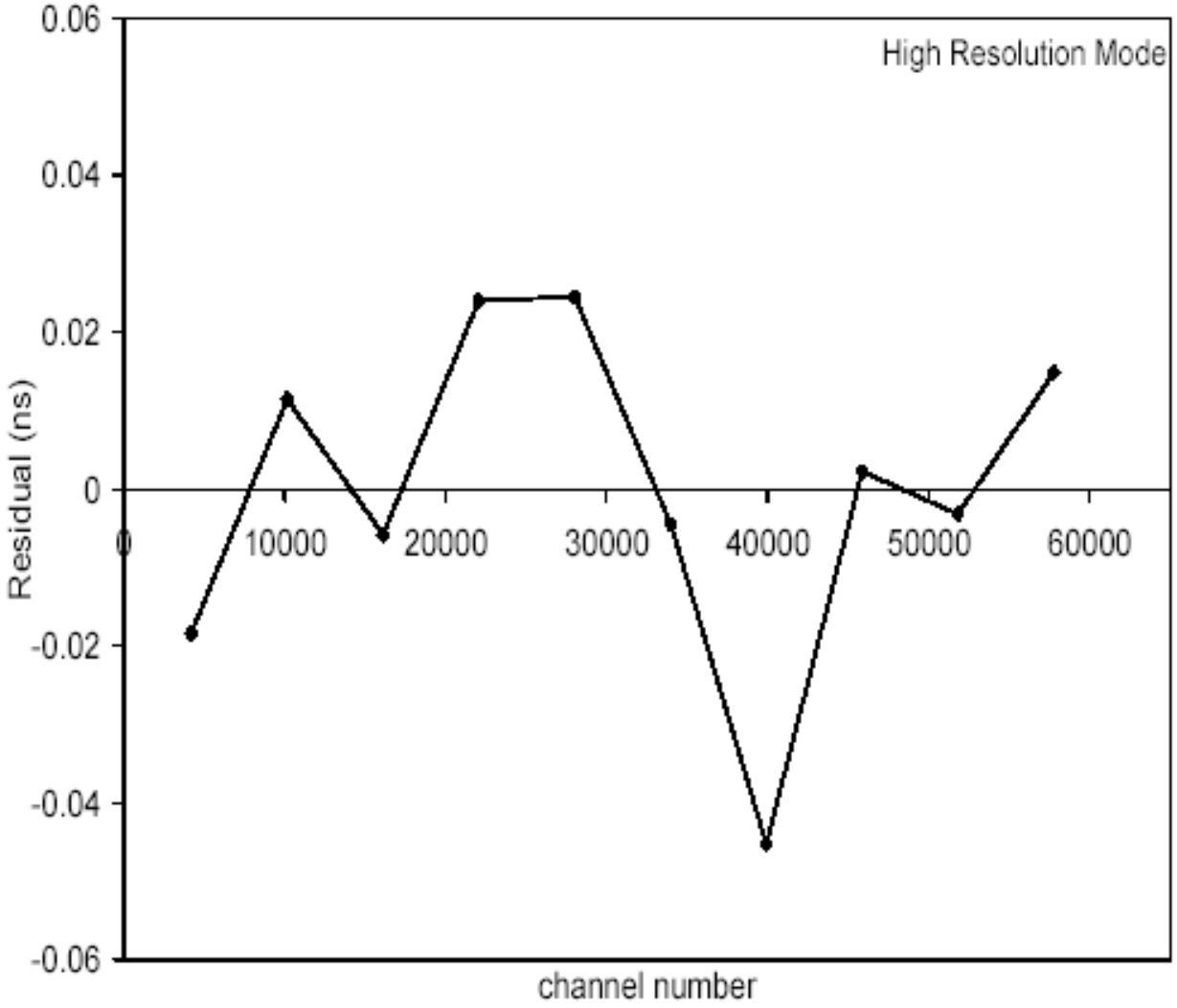
Timing distribution for an input signal that has a fixed time relationship to the *Start* signal. Unfolding the uncertainty of the input signal (33 ps) from the measured distribution yields a resolution (RMS) of 61.2 ps.



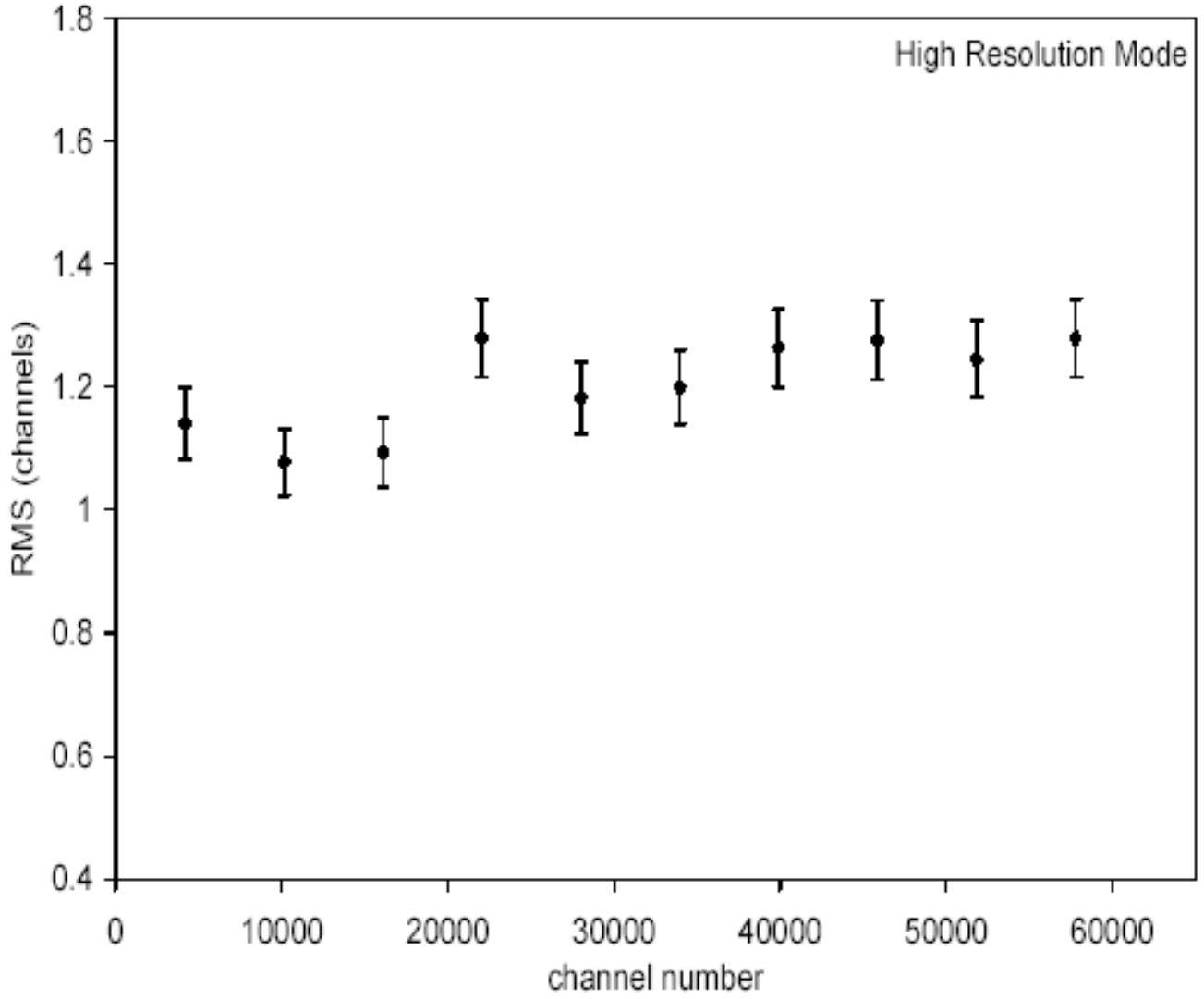
Timing distribution for an input signal that has a fixed time relationship to the *Start* signal. Unfolding the uncertainty of the input signal (33 ps) from the measured distribution yields a resolution (RMS) of 86.2 ps.



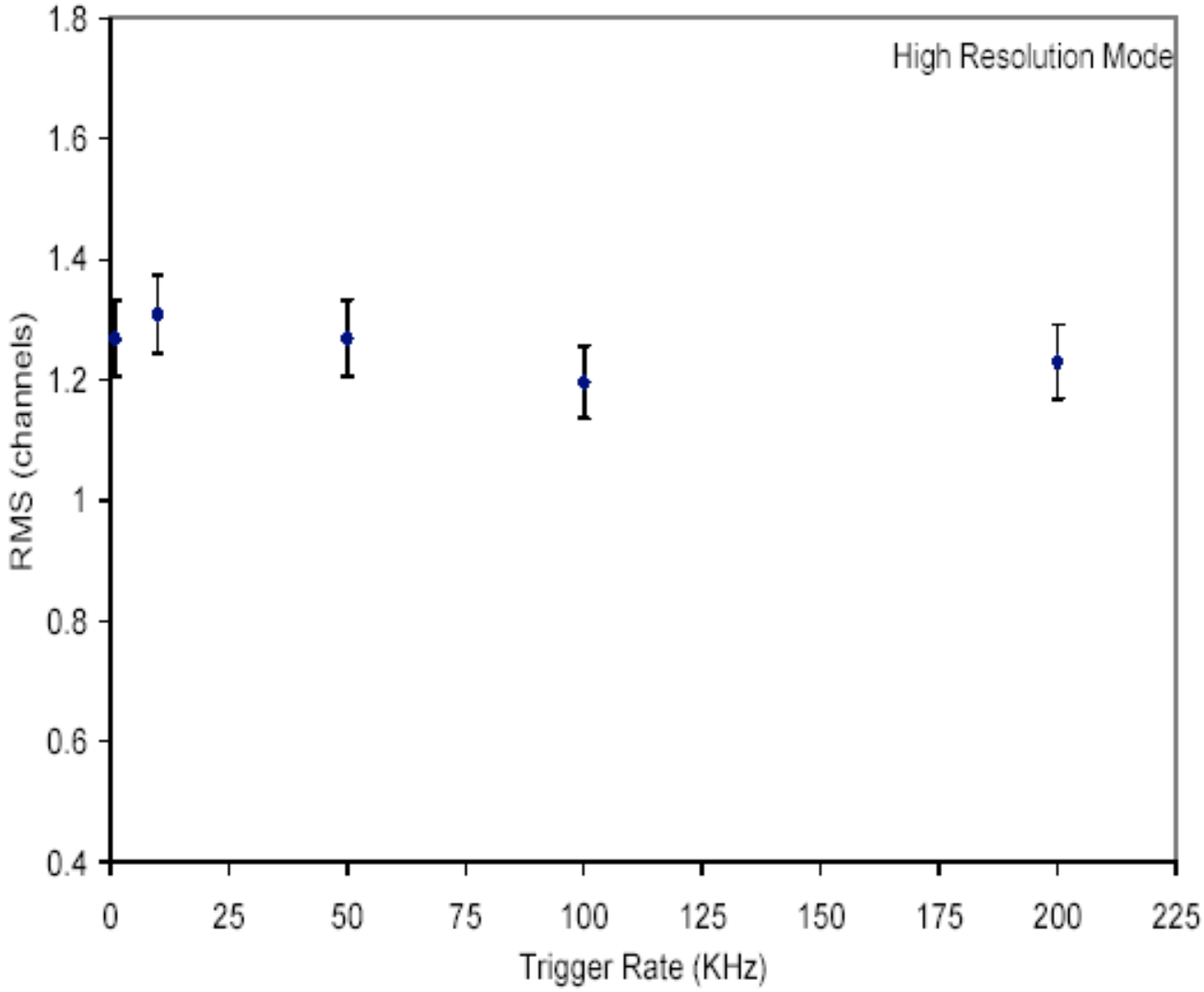
Transfer function for the TDC in high resolution mode.



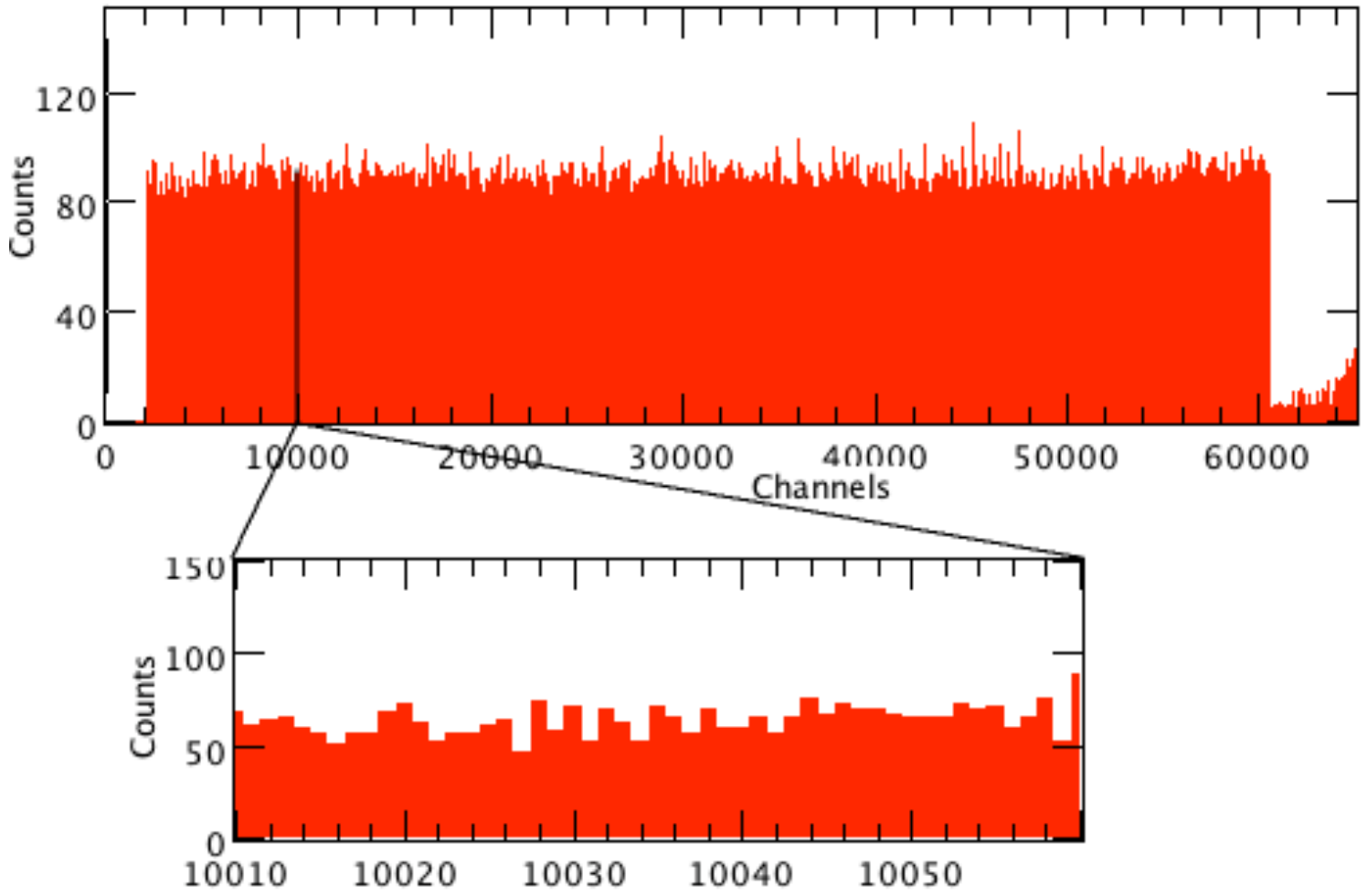
Residuals for the linear fit of the transfer function of the TDC in high resolution mode. Note that one TDC channel (bin) corresponds to about 0.06 ns.



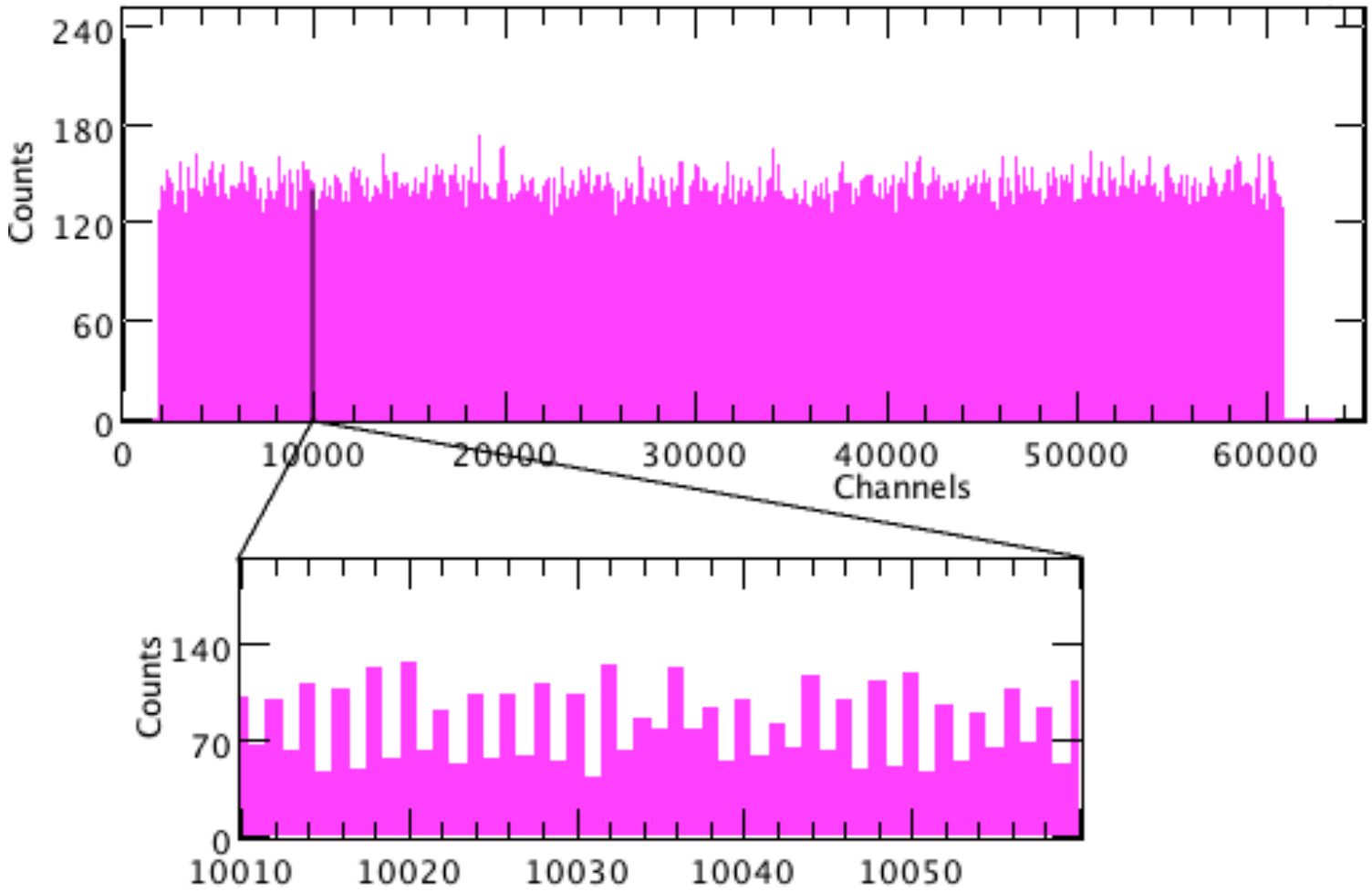
Resolution across the TDC dynamic range (high resolution mode).



Resolution as a function of trigger rate (high resolution mode).



Differential linearity (normal resolution mode).



Differential linearity (high resolution mode).

TDC Calibration (High Resolution)

- The signal propagation of each channel input can be delayed by approximately 1 LSB in 64 individual steps.

- In high resolution mode the choice for the delay is such that an even numbered channel is precisely 0.5 LSB later than its neighboring channel.

- In high resolution mode a second reference channel is used to increase the resolution of the standard reference channel. This second channel can also be delayed by 0.5 LSB (64 steps) with respect to the standard reference channel.

- Calibration amounts to adjusting these delays to minimize the observed resolutions. If we fix one of the channels of each input pair to have delay ‘zero’, there are 64 x 64 = 4096 combinations of delay to try.

- Brute force – 4096 runs
- Use non-synchronous mode to keep channel (pairs) independent
- Automate:
  - Initialize statistics
  - Adjust delays – do all channels of a board simultaneously
  - 2 K trigger run
  - Write statistics
  - Repeat…
- ~ 2 hrs per board - single output file has all information needed

- Analysis
  - Note that the reference channel delay is common to all channels of a chip, so one can't simply search for the minimum resolution of channels independently.
  - For a fixed reference channel delay, find the minimum input channel resolution for each input channel and save the corresponding input delay values.
  - Sum these resolutions .
  - Minimizing this sum over all possible reference delays identifies the best reference delay for the chip.
  - The saved input delay values corresponding to this reference delay are the appropriate input channel delays.
- Results – 10 to 15% improvement in resolution over default values (3F)

Control Signal Distribution

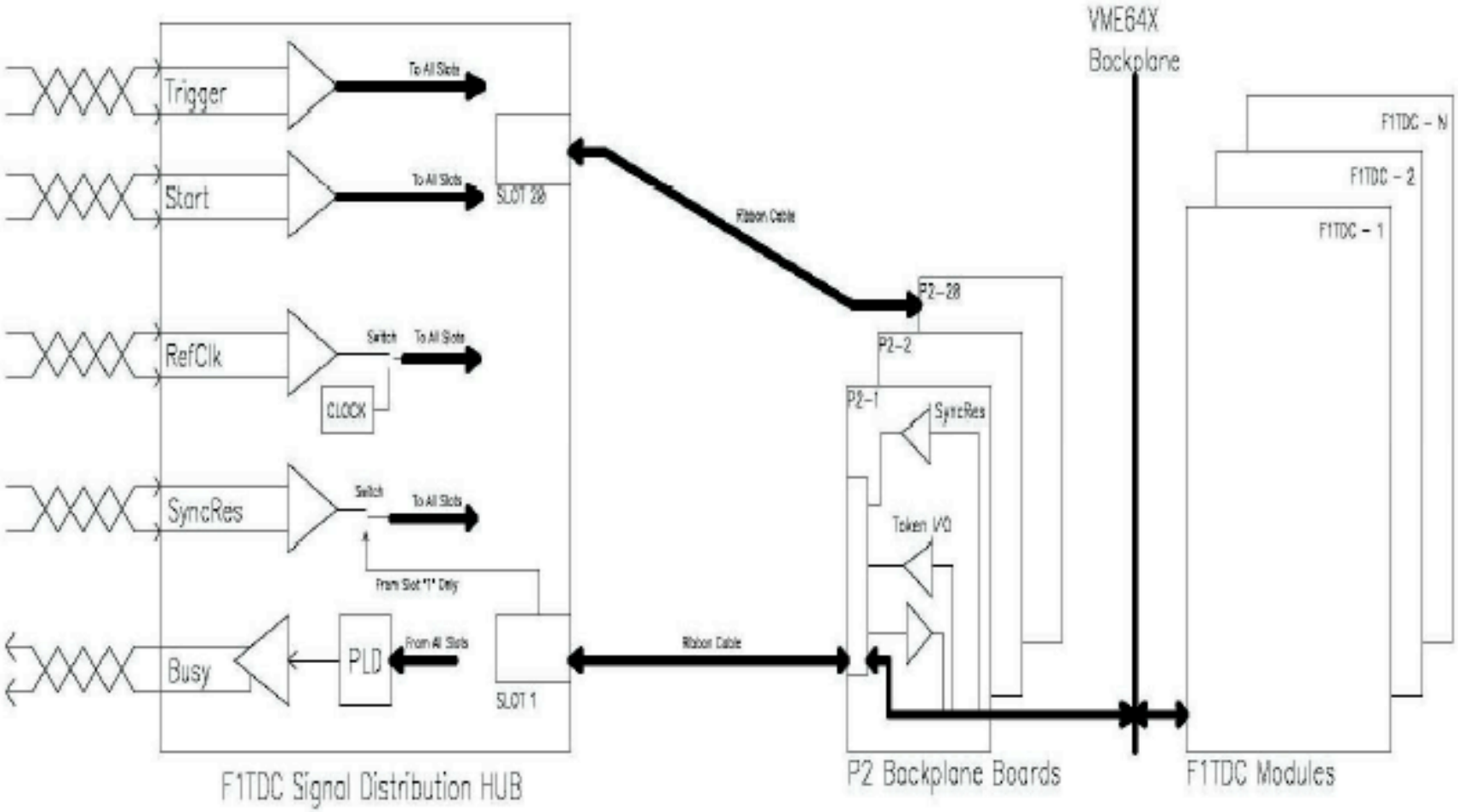
- Distribute: Clock, Trigger, Start, Sync-reset Collect: Busy

- Front panel distribution card
  - Supports up to 5 TDCs
  - Programmable internal/external clock and sync-reset selection
  - Can be cascaded to support > 5 TDCs
  - Separate slot-to-slot token-passing cables must be installed on backplane
  - VME64x module

- Backplane distribution system (Hub)
  - Supports up to 20 TDCs
  - Internal/external clock and sync-reset selection by hardware switch
  - Built-in token-passing lines
  - Write to register in 1st TDC generates a sync-reset signal which is distributed to all TDCs in the crate

- We can support a system of 5 TDC crates using a single front panel distribution card connected to 5 Hubs.

Backplane Signal Distribution



Current Board Status

- 50 TDC boards built in 1st run
- 34 passed rigorous initial testing
  - 12 to Hall B (eg3)
  - 9 to Hall C (HKS)
  - 1 to Hall A
  - 1 for Electronics Group test stand development
  - 11 for DAQ testing development
- 16 in repair queue
  - 8 have relatively simple problems and should be easily fixed
  - 7 have problems that need further investigation
  - 1 has a serious problem – firmware won't load

Testing

- 8 distinct operating modes tested
  - High resolution / normal resolution
  - Synchronous / Non-synchronous
  - Front control inputs / rear control inputs
- Resolution computed for all channels (on-the-fly)
- ~ 30 minutes per board

- 40 new boards arriving soon (late December)

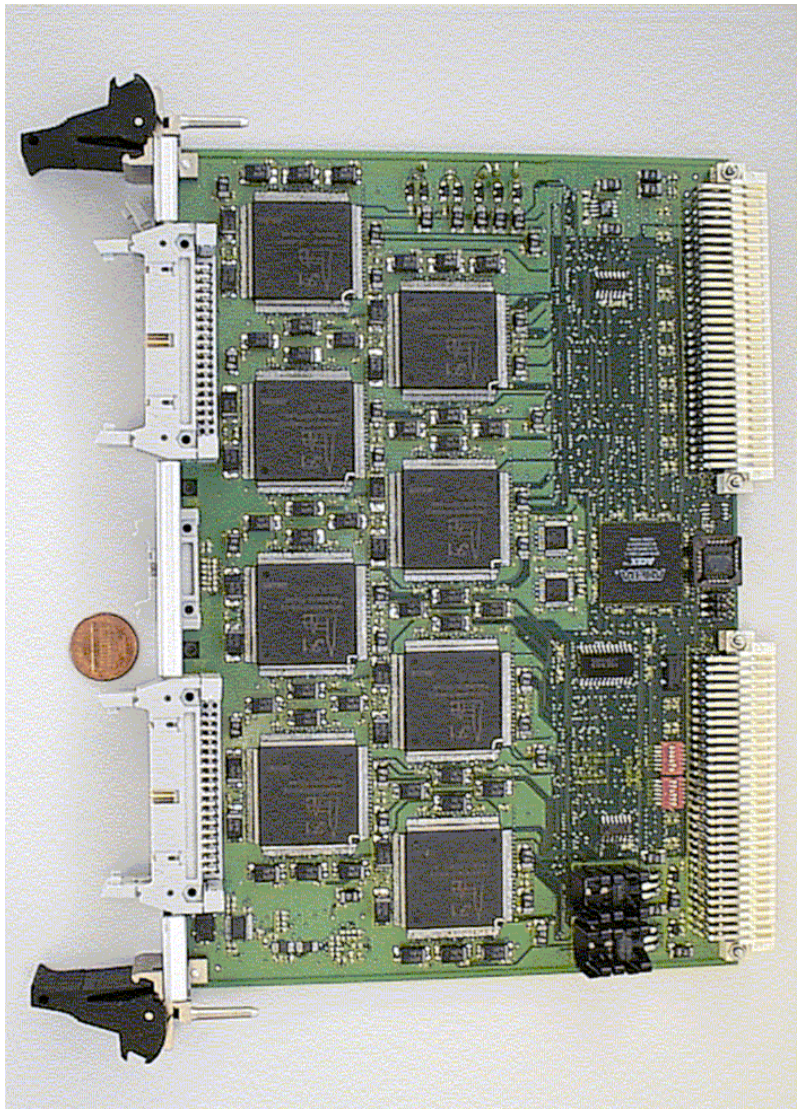
Software Status

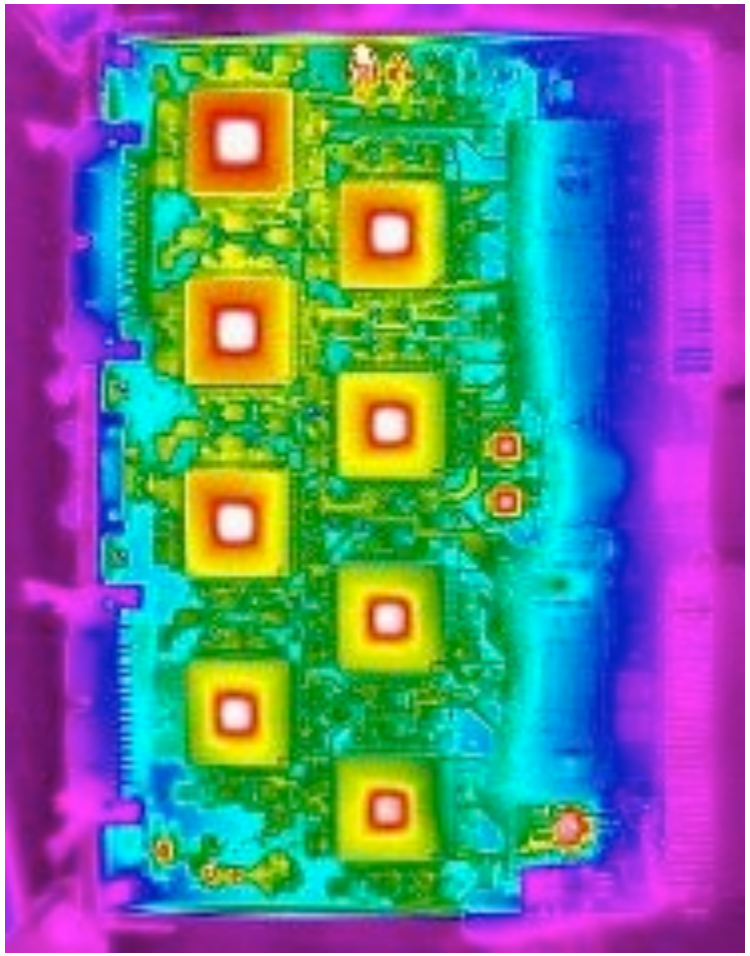
- Dave Abbott has assembled an extensive library of routines to configure, monitor, and read out F1 TDCs. These are compatible with CODA (data acquisition software for experiments).
- EJ has a set of test and analysis programs that run under VxWorks and Unix.
- Tanest Chinwanawich and Brian Eng are developing a test stand for the Electronics Group using Dave's software library and a Labview user interface.
- F1 TDC board user manual is available on-line.

What needs to be done

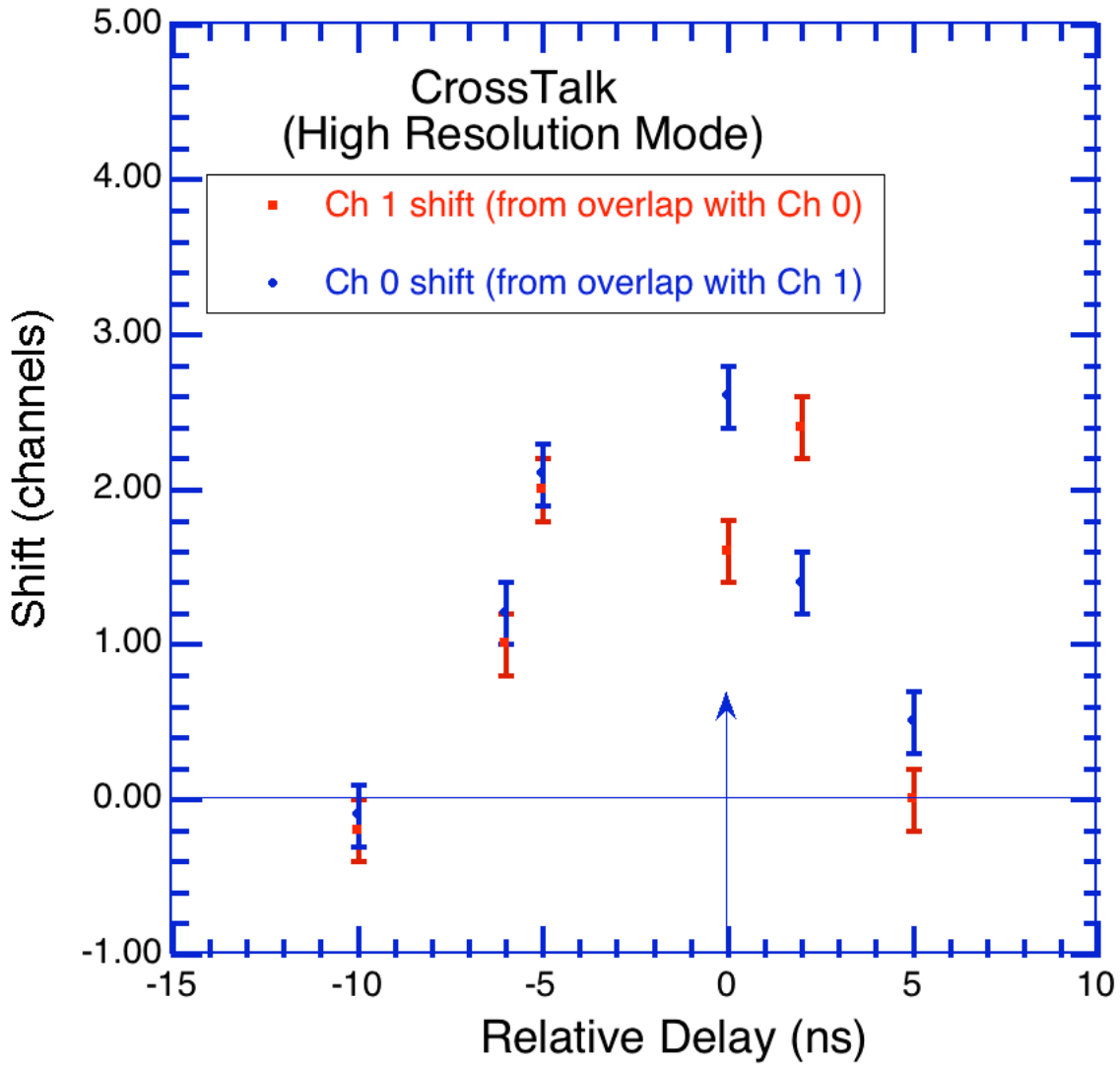
- Start fixing broken boards (since demand for boards is up)
- Continue multi-board resolution studies using the Hub
- Calibrate TDCs
- Implement auto configuration loading at power-up or board reset
- Implement new features (firmware upgrade) to enhance control and monitoring, and ease in recovery from error conditions
- Better understand some undocumented ‘features’ of the F1 chip

JLab TDC Module - Thermal Image





END



Example of cross talk for adjacent inputs of the F1 chip.

TABLE 1
CROSSTALK EFFECTS (MAGNITUDE AND WINDOW)

Inputs	0	1	2	3
0		+2.4 Ch -10ns - +5ns		
1	+2.6 Ch -10ns - +5ns		-1.5 Ch -5ns - +5ns	
2				+4.0 Ch -10ns - +5ns
3			+3.6 Ch -10ns - +5ns	

Summary of cross talk effects in the F1 chip (high resolution mode).

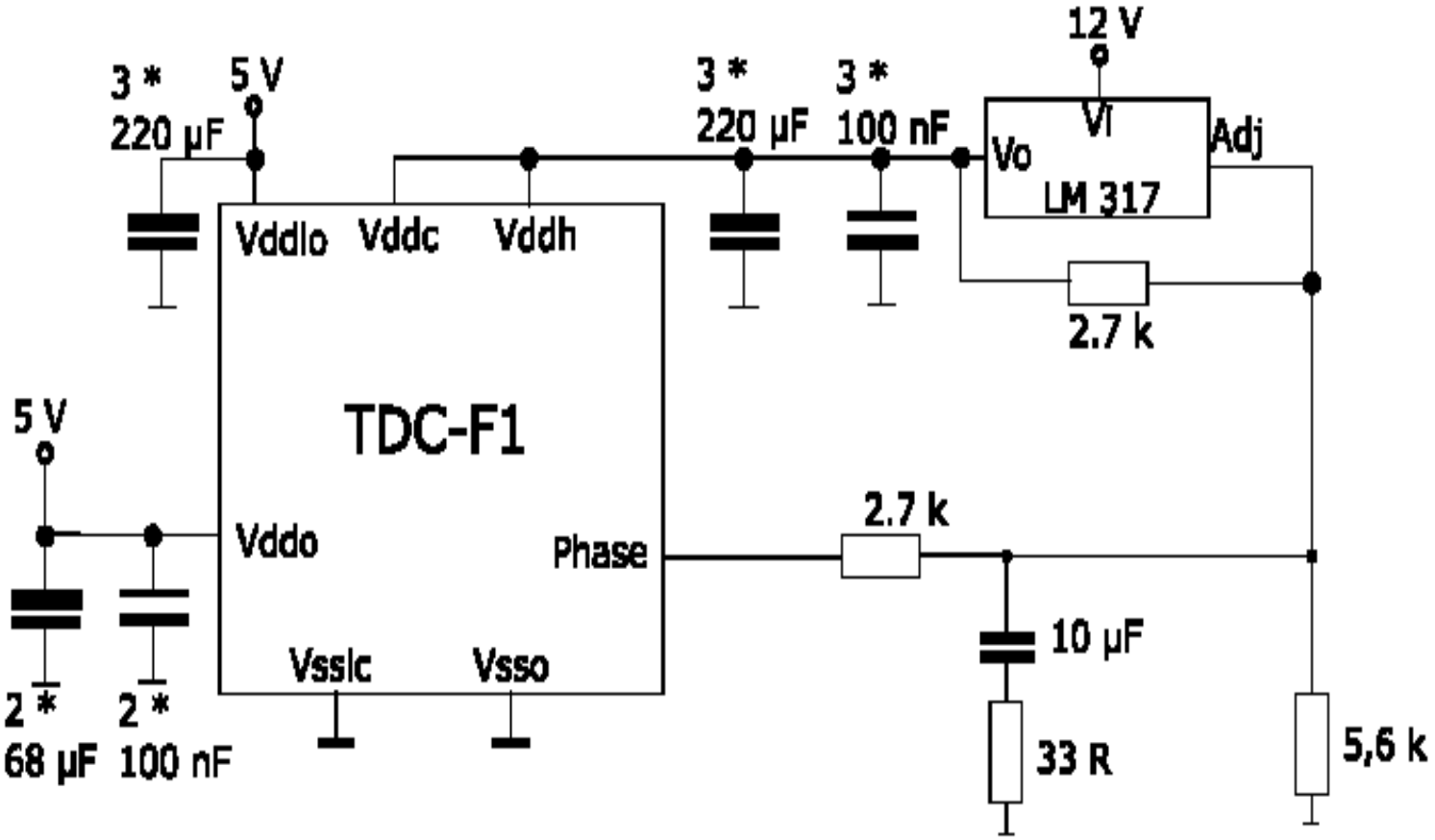
0	1 Bit Trigger-buffer overflow	6 Bit Event number	9 Bit Trigger time	1 Bit Xor setup register	3 Bit Chip Address	3 Bit Channel Address

header word

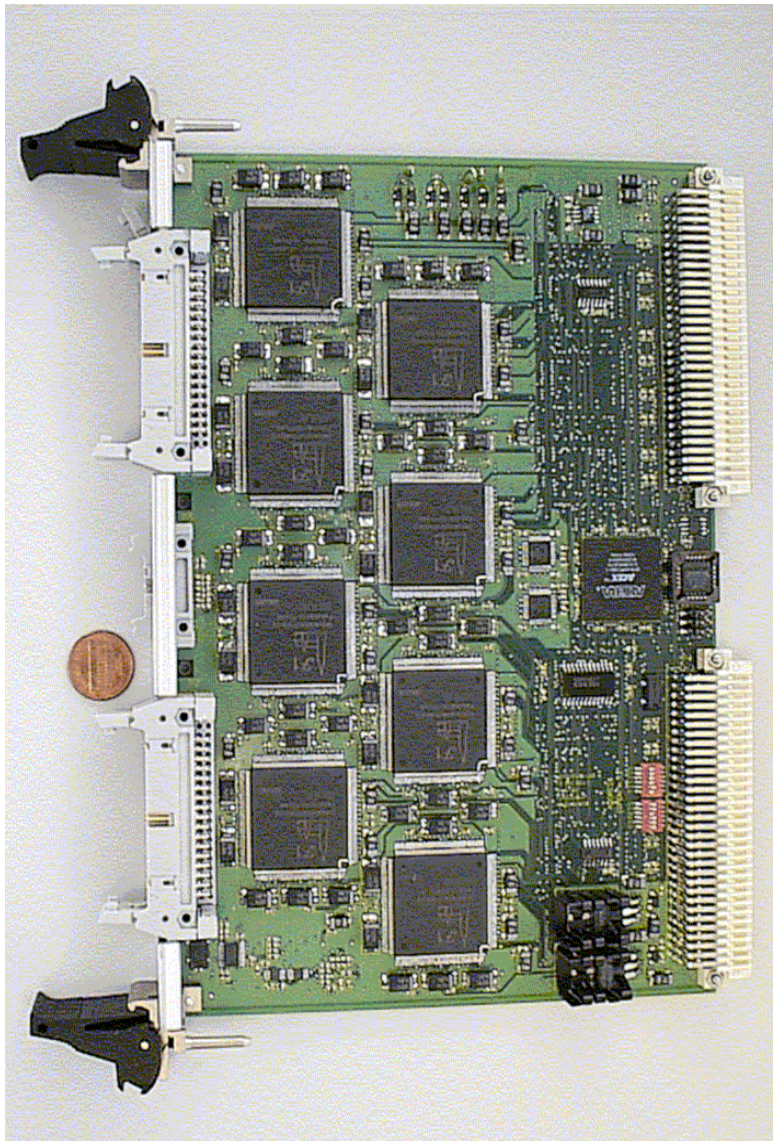
1	0	3 Bit Chip Address	3 Bit Channel Address	16 Bit Time (measured relativ to last synch. reset)

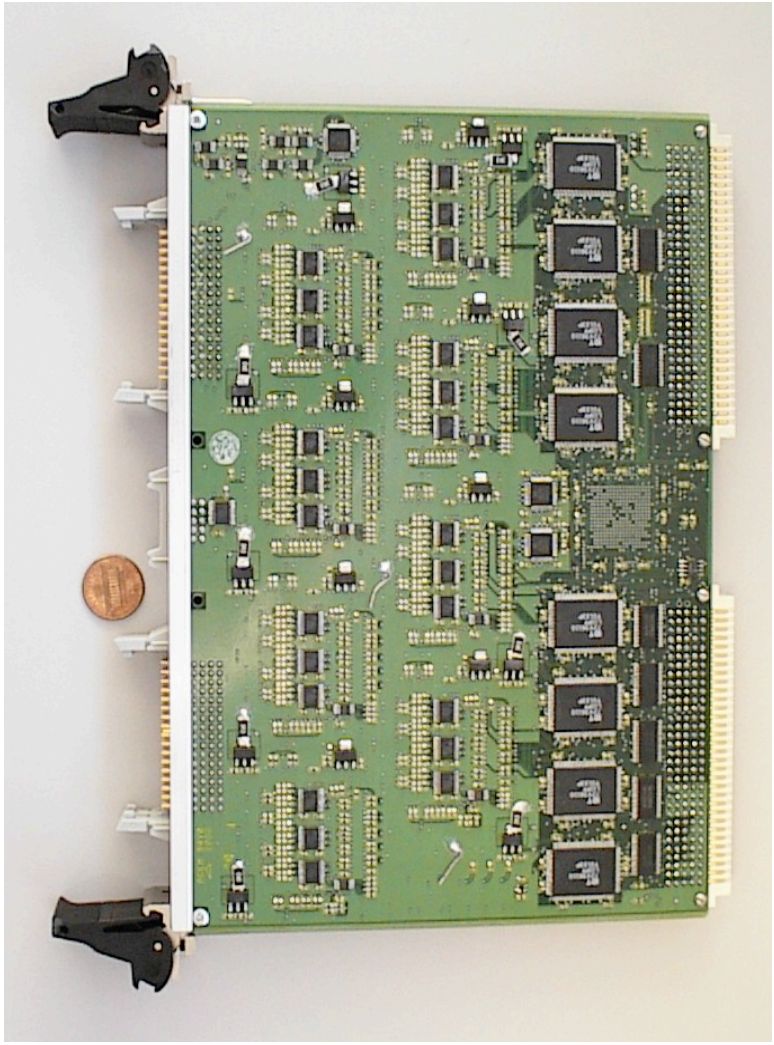
data word - time measurement

External Circuit for Resolution Lock



JLab TDC Module – Top & Bottom Sides





F1 TDC Chip Block Diagram