Agenda

- FADC Requirements Overview
- Chip Survey
- Two FADC Models
- FADC Architecture
- Project Guidelines

From FJB 10/19/2004 – FADC_MEETING_2

FADC TYPES & QUANTITIES

	8-10 bits 250 MSPS	10-12 bits 125 MSPS	8-12 bits 62.5 MSPS
Hall A	*~300**		
Hall B	*~2,500**		
Hall C	64		
Hall D	4,000	3,240	11,400
Total	6,864	3,240	11,400
Ch/chip	1	1	1, 2, 4, 8
Ch/Module	16	16	16, 32, 48, 64
# Modules	*A 19** *B 157** C 4 D 250	203	713,357,238,179
# Crates *(20 Modules per Crate)*	*A 1** *B 8** C 1 D 13	11	36, 18, 12, 9

** These quantities are estimates.*

FADC TYPES & QUANTITIES

	FADC-250 10 bits, 250 MSPS	FADC-65 8-12 bits, 62.5 MSPS
Hall A	*~300**	
Hall B	*~2,500**	
Hall C	64	
Hall D	4,000 + 3,240	11,400
Total	10,104	11,400
Ch/chip	1	8
Ch/Module	16	64
# Modules	*A 19** *B 157** C 4 D 250 + 203	179
# Crates *(20 Modules per Crate)*	*A 1** *B 8** C 1 D 13 + 11	9

** These quantities are estimates.*

ADC Chips – A Brief Market Survey (65, 125 & 250 MSPS)

65 MSPS --- 8-12 BITS (≥ 2 Channels/Chip)

Part #	# Bits	# Channels	Rate (MSPS)	Cost ($)
MAX1198	8	2	100	11
AD9288	8	2	80	7
AD9289	8	8	65	11
MAX1182	10	2	65	12
AD9216-65	10	2	65	DEC2004
ADS5277	10	8	65	40
AD9238-65	12	2	65	29
MAX1127	**12**	**4**	**65**	**36**
AD9229-65	**12**	**4**	**65**	**DEC04**
ADS5272	12	8	65	65

125 MSPS --- 10-12 BITS

Part #	# Bits	# Channels	Rate (MSPS)	Cost ($)
MAX1122	10	1	170	37
AD9411	10	1	170	43
LTC2234	10	1	135	28
MAX1213	12	1	170	69
AD9433	12	1	125	76
LTC2224	12	1	135	47

250 MSPS --- 8-10 BITS

Part #	# Bits	# Channels	Rate (MSPS)	Cost ($)
MAX1121	8	1	250	24
AD9480	8	1	250	22
SPT7721	8	1	250	20
MAX1124	**10**	**1**	**250**	**50**

Two FADC Models

- Developing one generic model platform is attractive because of limited resources:

  - FADC-250
  250 MSPS, 1 ch/chip ►16 Channel Module
  > Covers Both 250 and 125 MSPS Requirements
  > Plug-in Boards for Custom Data Processing Fulfils Users' Requirements.

- Higher Channel Density = Cost & Space Savings

  - FADC-65
  65 MSPS – 8 ch/chip ►64 Channel Module.

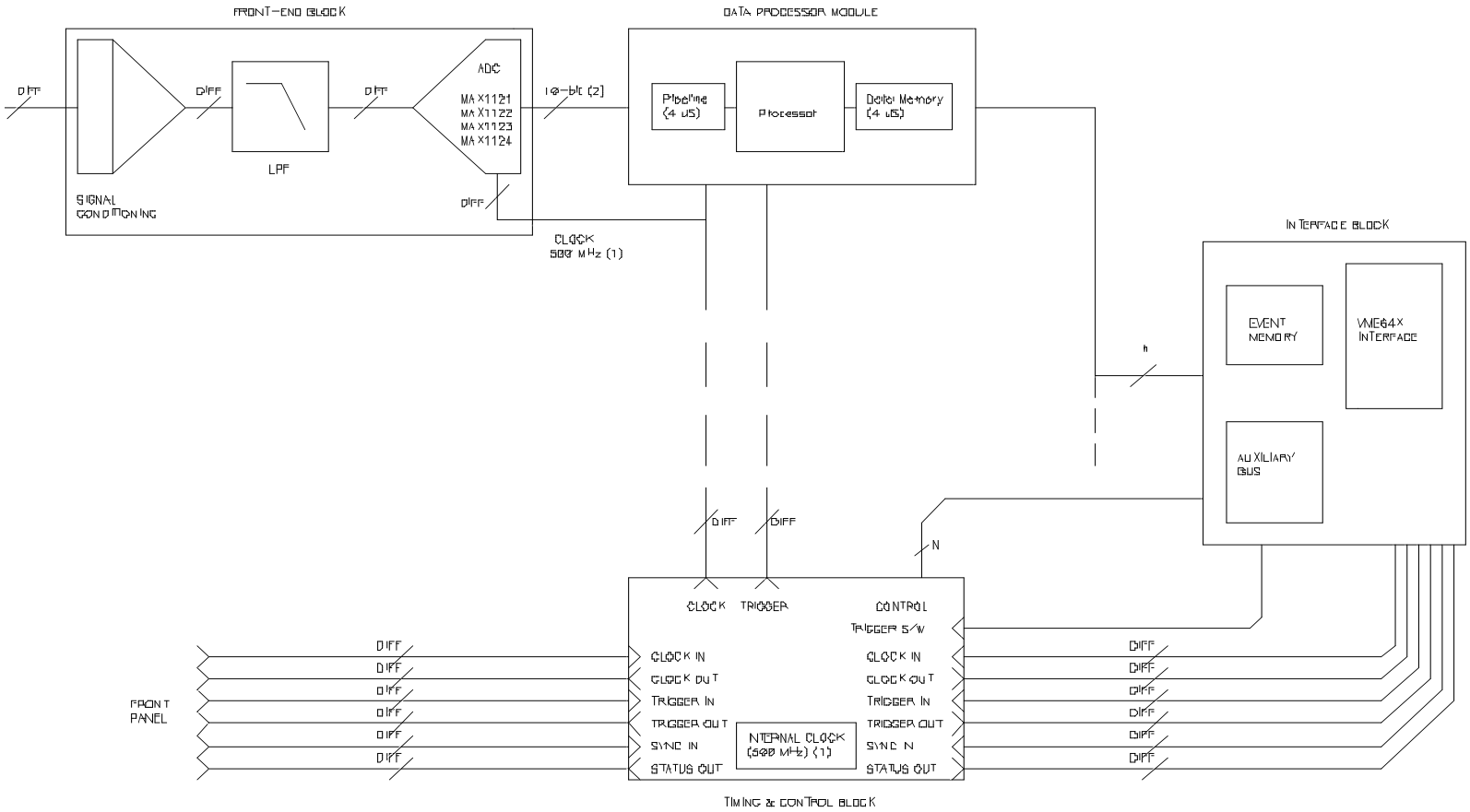
- One Design Architecture for Both Versions.
- Total System Cost is Lowered Considerably!

VME64x Flash ADC Modules…FADC-250 & FADC-65

Preliminary Specifications - Values in [ ] refer to FADC-65

Signal Inputs	Number	16 [64], Differential
Clock	Sampling	250 [62.5] MSPS, Differential
	Source	Internal and External
Control Inputs/Outputs	Clock In	IN, OUT - Differential (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Sync In	Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe
	Status Out	
Conversion Characteristics	Resolution	10 [12] bit
	INL	± 0.8 [0.6] LSB
	DNL	± 0.5 [0.3] LSB
	SNR	56.8 dB @ 100 MHz [70.5 dB @ 51 MHz] Input
Trigger Latency	8 µS	
Data Memory	8 µS	
Data Processing	Sparcification Windowing Energy & Value (Pedestal, Peak) Time (Threshold, Rise, Fall, relative to trigger) Operation (Arithmetic, Logical, Single & Multi-channel) Output Bus (Front Panel, Backplane, Bus)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320MB/sec)	
Packaging & Power	6U VME64x / +3.3V, +5V, +12V, -12V	

FADC Architecture



1 on these ADCs.

1. The 500 MHz clock is internally divided by two, yielding 250 MSPS.
2. 8-bit or 10-bit ADCs may be used.

FADC – A VME64x FLASH ADC
FUNCTIONAL BLOCK DIAGRAM
FJB, JLAB, 6 OCTOBER 2004
PRELIMINARY

FADC_BLOCK.SCH

Project Guidelines

- Concept & Specifications
  - Finalize Requirements With Users
  - Data Processing Algorithms Need To Be Specified & Tested
  - Data Structure and Format Need To Be Specified
- Resource Identification, Allocation & Scheduling
  - Who's going to do what and when?

Project Guidelines (cont.)

- Design & Layout - FJB, EJ, JP, PS
  - Module
  - Backplane
  - Timing & Control
- Test – Two Parallel Developments:
  - Labview – Closely Coupled to Design and Development – JP, EJ, TC, TT ??
  - Coda – Based on End-User Requirements – EJ, DA, Users
- Production Cycle – FJB, EJ, JP, PS
  - Procurement
  - Test
  - QC
  - Installation