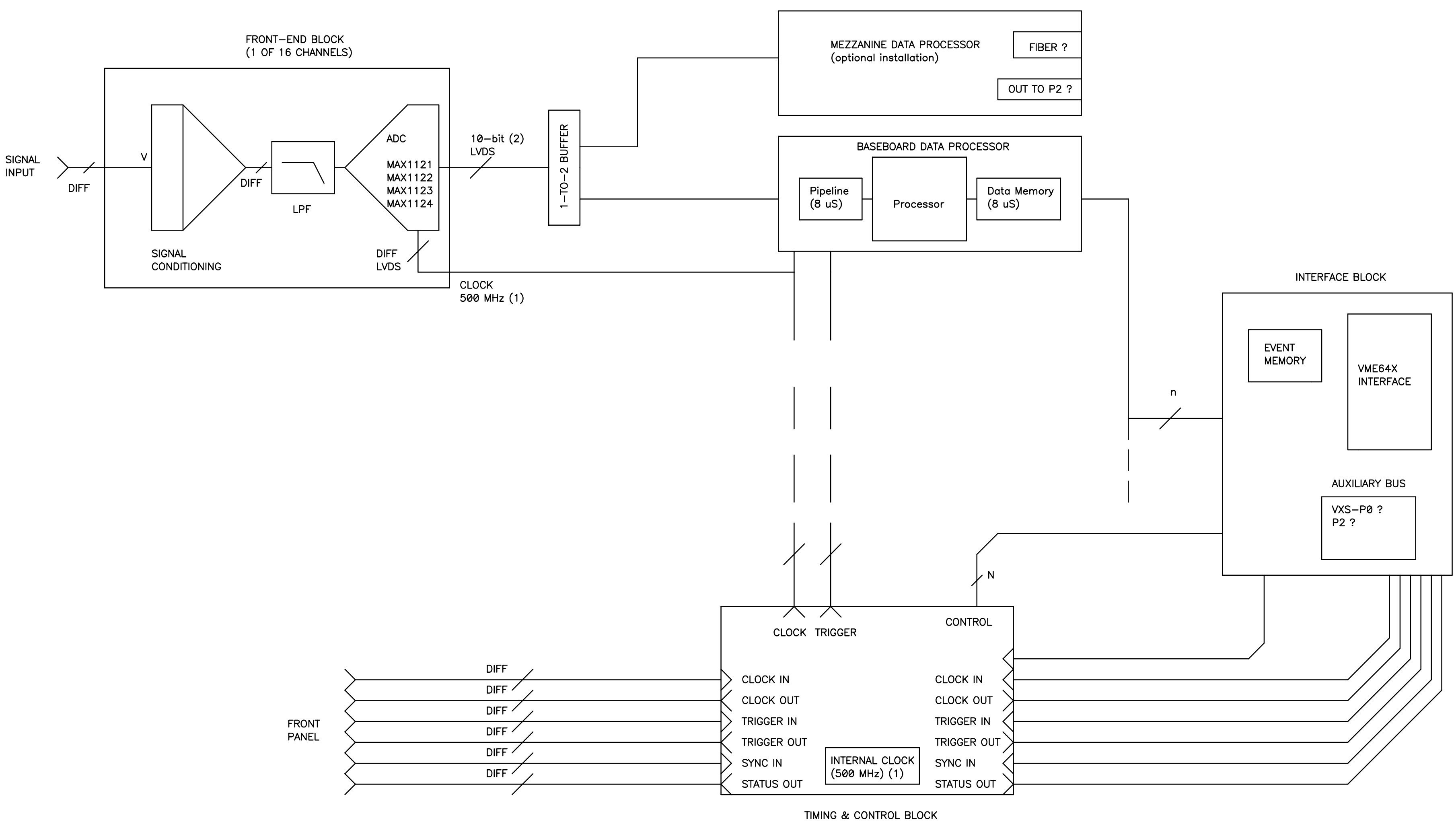
FADC ARCHITECTURE



NOTES on these ADCs:

1. The 500 MHz clock is internally divided by two, yelding 250 MSPS.
2. 8–bit or 10–bit ADCs may be used.

DWG. NO.		SH.	REV.

TITLE	FADC – A VME64x FLASH ADC FUNCTIONAL BLOCK DIAGRAM FJB, JLAB, 15 MARCH 2005 PRELIMINARY		
SIZE B	CAD I.D. NO. FADC_ BLOCK.SCH	DRAWING NO.	REV.
SCALE	SHOWN ON	SHEET OF	