April 7, 2005

Minutes from GlueX Electronics conference call

participants:

U Regina: Mauricio Barbi, Keith Wolbaum

Alberta: Lars Holm, Jim Pinfold

Jefferson Lab: Chris Cuevas, Fernando Barbosa, Ed Jastrzembski, Elliott Wolin, Dave Abbott

Indiana U: Paul Smith, scribe

Paul showed 3 slides (GlueX doc 456). The first shows how the board level energy sum could be reduced to 8 bits at 250 MHz and sent using LVDS to a summing slot over a standard 2.17 or VXS backplane. If necessary, both clock edges could be used to transmit the entire 12 bit sum over 6 pairs at 500 MHz. Crate level sums would be sent using LVDS or ECL on cables - the LGD fADCs will occupy no more than 20 crates which are all close to each other, so the cables would only be a few meters long. For the Barrel, this depends on exactly how 8 crates are distributed around the magnet, but it should be possible to keep the summing cables less than 5 meters. This avoids the high speed serial links. The slot to slot skew within a crate can be compensated for by adjustable per pin delays in newer FPGAs.

Slide 2 compares relative pricing for various backplane options; VXS is currently expensive because of the exotic laminate required. Only 12 slots are currently offered.

Slide 3 shows pricing for a PICMG 2.16 ethernet switch card; they are about half the cost of a VME or cPCI CPU card. Elliott pointed out there may be other reasons to want a crate-level CPU. There are industry standard “platform management” boards and software available for monitoring fans, power supplies, temperatures, etc; In cPCI this is the 2.9 standard; in VME this is VITA 38; the switched ethernet technology is VITA 31.1

JLab gave a brief update on their fADC R&D.

Alberta has sent their 4 channel prototype CFD to IU; it will be tested with cosmic rays and then in a beam test of the TOF this June at TRIUMF. They will have a report on preamps for the next conference call.

There was a discussion of topics that need to be addressed at the next GlueX collaboration meeting. These topics include the role of standards in GlueX and commonality with the existing and upgraded halls at JLab. This includes DAQ software issues as well as hardware maintenance. An important consideration is the allocation of manpower and the division of responsibilities and funding between the laboratory and the collaborating institutions. A time scale and procedure for making decisions needs to be established in preparation for moving the GlueX electronics system from R&D to implementation.

Next conference call: 2 PM EDT, April 28 (Thursday).

Next meeting: Day before GlueX collaboration meeting (May 11?), JLab