Noise Comparison of Some Preamps Relevant to FDC/prototype work

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Motivated by a desire to understand pulse shapes and noise levels from the FDC prototype, and in the full FDC, and to make a start on a simulation model of the readout electronics, I have made plots of the noise level in:

- the CLAS preamp (a transimpedance amplifier) read out by an integrating ADC, exactly (I believe) as being used with the FDC prototype
- preamp "X" – a charge-sensitive amplifier and 2nd order shaper with peaking time of about 40 ns, of my own design*
- the *original* ASD-8 chip†

There is at least one later version of the ASD-8 with slightly different noise characteristics, but I do not have the data. Nor do I have a simulation model of the ASD-8 chip – if we are seriously considering it we should contact Mitch Newcomer to obtain such a model to run our own simulations.

All of these plots are made using a short current pulse input to calibrate the charge gain of the system. In other words, with a real detector signal with its long tail the effective gain is reduced and hence the effective noise level (in terms of *total* signal charge rather than observed signal charge) is increased.‡ The way the noise is specified here is detector-independent and is customary. But for final simulation we will need of course to use realistic signal shapes.

Note that the ASD-8 chip is optimized for relatively low capacitance detectors. It may not be a good choice for the FDC cathodes, unless we get a modified version optimized for higher capacitance. Part of my goal in this note is to stimulate discussion of the FDC cathode preamplifier/shaper requirements.

In the FDC cathodes I estimate *(roughly – I guess it's maybe 20% high)* the capacitance to be

- 41 pF/m from a strip to all other strips
- 9 pF/m from a strip to the ground plane
- 9 pF/m from a strip to the wires
- 8 pF for connections

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* Which is *not* fully optimized, does not include the necessary tail cancellation, and includes the shaper only by "behavioural modelling" not actual circuit design (this should not make much difference since the shaper should not contribute significant noise in a proper design).

† This is the Mitch Newcomer ASD-8 not the Boston Muon Consortium ASD. On the latter there doesn't seem to be any published data with a capacitive detector but on the other hand there is a complete schematic so we can simulate it if desired.

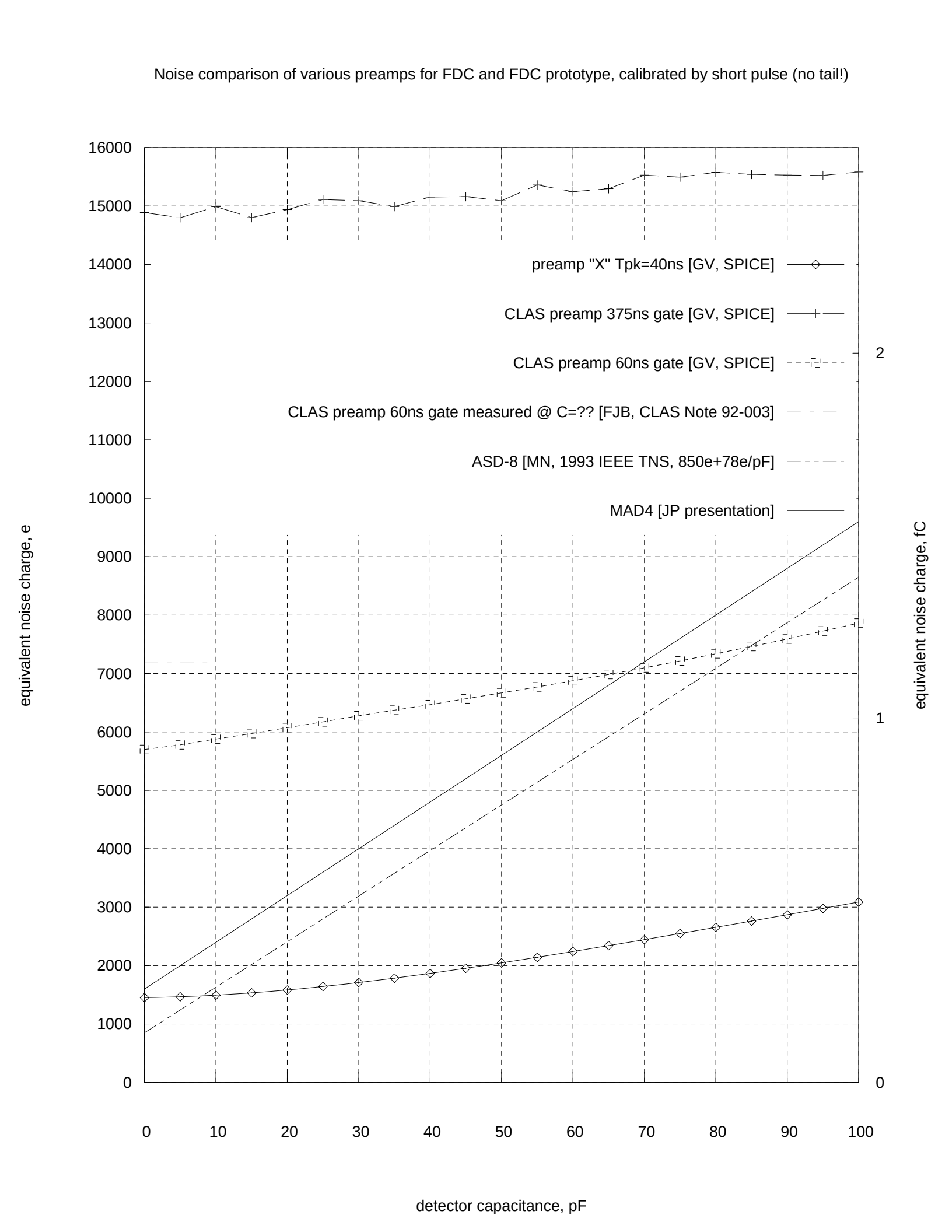
‡ This effect is already accounted for in the detector signal charge estimates, e.g. in GlueX-doc-412-v8

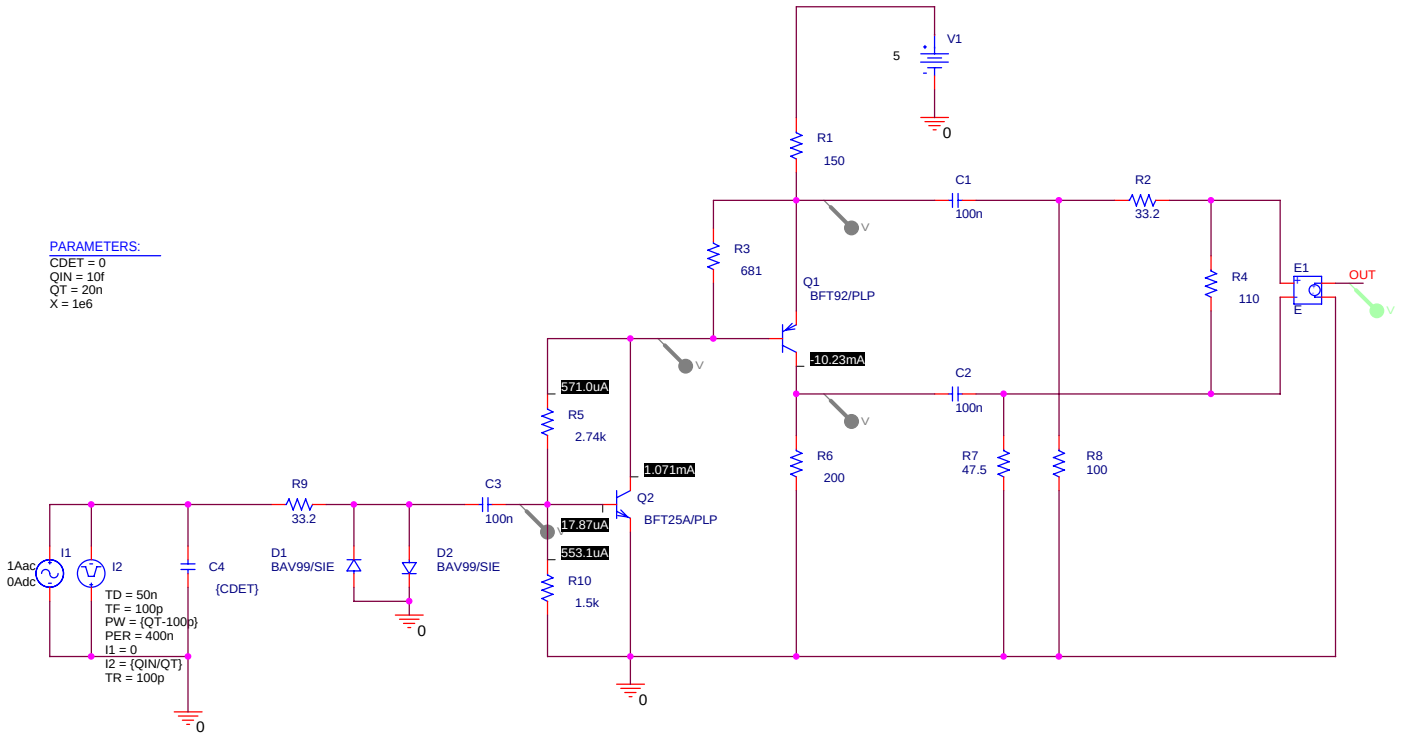
which is a total of 79 pF for the longest strips in the real chamber (1.2 m), or 23 pF for the longest strips in the prototype (0.25 m).

In the FDC cathodes the characteristic impedance is so low (neighborhood of 100 Ohms) that a far side termination resistor would cause extreme noise. In the FDC anodes and the CDC it could be considered, maybe, though I expect the noise will be worse. In any case I have not considered a far-side termination here and so the detector is basically capacitive. In other detectors such as ATLAS MDT the far-side termination is motivated (if I understand correctly) by the pretty long length 6 m and the rate capability 400 kHz.

Also I should mention that the peaking time will have to be some factor greater than the ADC sample interval, e.g., 16 ns, if we have any hope of measuring the peak amplitude from straightforward waveform sampling. For instance the original ASD-8 has a peaking time of order 10 ns which probably demands a higher sample rate than 62.5 MHz. This also has to be considered in the preamp specification.

Finally, note that this is only a preliminary study and should not be construed as an exhaustive survey of our noise options.


Noise comparison of various preamps for FDC and FDC prototype, calibrated by short pulse (no tail!)
equivalent noise charge, e
equivalent noise charge, fC
detector capacitance, pF
preamp "X" Tpk=40ns [GV, SPICE]
CLAS preamp 375ns gate [GV, SPICE]
CLAS preamp 60ns gate [GV, SPICE]
CLAS preamp 60ns gate measured @ C=?? [FJB, CLAS Note 92-003]
ASD-8 [MN, 1993 IEEE TNS, 850e+78e/pF]
MAD4 [JP presentation]
16000
15000
14000
13000
12000
11000
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
2
1
0
0
10
20
30
40
50
60
70
80
90
100



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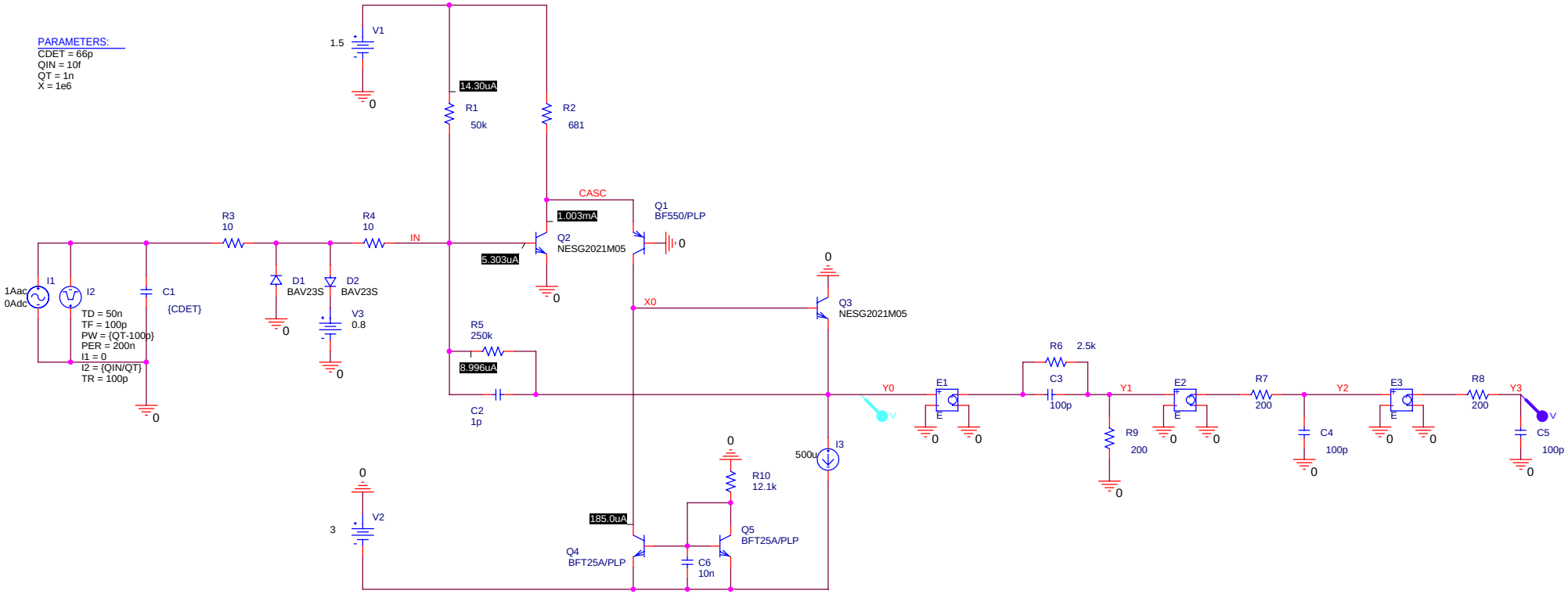
ANODES: AC COUPLED, C=2200pF 2.5kV R=1M, CDET=0-11pF+8pF STRAY
CATHODES: DC COUPLED, CDET=0-58pF+8pF STRAY



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