GlueX preamp chip teleconference meeting October 5, 2005
John Schaapman, scribe

summary
 and a few added comments (*) John Schaapman
                         (**) Gerrard Visser update
present:
U of A: Jim Pinfold, Lars Holm, John Schaapman
U Penn : Mitch Newcommer
U Indiana: Paul Smith
UICF : Gerrard Visser

A. Input Protection
   does it need to be internal to the chip?
   - external protection circuit is OK
      (new diode being investigated Part # ?)
   -CDC has 300 pF coupling cap and up to 2 Kv ~ 1.5 mJoule
   * FDC requirements ? anode? cathode ?

B. Signal Range
     1 fC noise level ~ 2LSB equiv 6,000 e
    10 fC minimum signal
     3 pC max signal
    - 10K feedback resistor OK

C. Output Signal
    - no back termination at preamp OK
    - 1 volt differential
    - can pre-offset the output
      i.e. larger positive swing than negative
    goes to differential receiver - can adjust baseline here
      gain and more shaping can be done here
                        to suite different detectors and ADCs
    - completly dc system after the chamber coupling capacitor

D. Cable
    110 ohm overall shield twist and flat
    length: 10 - 14 m
    crosstalk : check that it's lower than 1 %

overall crosstalk we are aiming for is less than 1 %
intermediate buffer: may want buffer at edge of detector
for noise control
- detector self shielding
- racks noisey

E. Preamp Input
differential
dummy input ? into chamber for noise cancellation?
* - does this affect channel count?
* test pulse input capability ?

F Baseline Restoration
- CDC 800 nsec drift time and 600 KHz rate
could this be a problem ?
- choice of gas not known
- chamber at atmospheric pressure
- can baseline restoration be done by algorithm ?

G. Shaping
10 nsec for preamp - err on short side
- external shaping can be added if needed
tail cancellation
- digital filter by FPGA ?
could do switchable shaping in preamp
- several selections - power down unselected stages
pole-zero enabled seperately ?
plots of individual chamber pulses would be usefull
- available soon - CDC later than FDC

H. Recovery Time from Large Signal
highest energy is 5 Gev gamma
- produces large current pulse all at once
- channel might be dead for 1 microsecond
- probably OK
- depends on rate that these events occur
- should try to simulate how often this will happen
- ASDs could handle 1 pC
- can do SPICE simulation to see effect on preamp
- neutrons ?

I. Connection from Chambers to preamp
  CDC - preamp external to gas volume
              - HV and coupling caps inside
      - 6 inch fanout inside chamber
           - crosstalk, capacitance, inductance ???
  FDC not determined yet
      - probably about 2 inches

J. Radiation Environment
   affects choice of process
   less than 1 MegaRad - check ?

K. Power Consumption
   1 - 2 ma per stage plus 10 ma for output stage
   15 - 20 ma per channel including the output driver
   supply voltage - technology dependant
     3 - 5 v (45 - 100 mW per channel)
   for BiPolar process
    negative supply or +/- 2 - 3 v preferred
                (60 - 120 mW per channel)

L. Number of Channels per chip
   should be able to do one chip type for all chambers
   8 or 4 channels
   4 channel chip advantages
     - possibly shorter input layout path
     - may be able to use Quickchip semi-custom process
                                              from MAXIM
   * total power dissipation per package may affect this
                                                 decision
        8 ch x 120 mW/ch = 960 mW
        4 ch x 120 mW/ch = 480 mW

M. Processes
   SiGe huge factor in cost
     - CMC can do 5 prototype chips free

** Gerrard Visser update **
- since CMC prototype chips are produced by MOSIS
  will be able to shift to mini-production of
  40 chips at MOSIS - price $ 27,000
  if area under 15 mm**2
- final production would need 2,400 8 channel parts
  - checking on price
- SiGe is a 3.3 v process

CMC also offers " GA911 : 2.5 GHz Bipolar Linear Array"
from Gennum Corp.

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* will double the chip count for a 4 ch chip
affect the total cost ?

Quickchip semi-custom by MAXIM an option for 4 channel chip

lots of simulation reduces the number of iterations

N. Comparator
in second generation chip could add selectable comparator
- comparator output would be switched to replace the analog
  signal to the output driver when enabled

O. Next Meeting
in about 2 weeks to decide on process most suitable

Please post additions or corrections.

Thanks, John

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** Gerrard Visser update #2 **
(new diode being investigated Part # ?)

Diodes Inc. # SDA004, I have these on a preamp board (for another project) just received this week, I will attempt to capture some waveforms of a clamped line while sparking down with various capacitances from 2kV. (I hope I can do this without breaking my scope...) I'll also measure the capacitance and leakage current. Any other suggestions how/what to test? Results in a week or two.

dummy input ? into chamber for noise cancellation?
* - does this affect channel count?

We should make sure that the dummy input is routed as far as possible along with the input input - in particular for the CDC it needs to got through the connector into the gas volume, at least if my understanding of the construction is correct. Curtis, comments?

- checking on price

I received a budgetary quote from MOSIS:
> Estimated cost is $120K
>> SUBMIT_DATE: 6/2006
>> SIZE_1: 3 x 4 mm
>> PROCESS: 5HP
>> RUN_TYPE: MPW
>> QUANTITY_1: 2400
>> WAFER_OR_DIE_1: DIE

I did not pursue a price on a CMOS process. I am guessing, though, that 120k is not many times the price of CMOS, maybe 1.5 - 2x at most...