# Glue-X FDC/CDC ADC Module

Preliminary Specifications

• Resolution: 12 bits

• Sample rate: 65 MS/s (today) – higher sample rate no doubt will be practical in years to come – to be cost effective this board will require high density ADC's, such as MAX1438 [ 8 ch / 17×17 $mm^2$ footprint, 11.6 ENOB @ ≤30 MHz, 114 mW/ch]

• Analog pulse shaping: TBD, anything we can do with a few op-amps is fine… Will be coordinated with preamp ASIC & board design.

• Channel count: 96 (1920 ch/crate, FDC → 8 crates)

• Inputs: 16 channels per 40 conductor cable (jacketed shielded twist-n-flat, standard connectors); 1 V (differential) full scale input, 110 Ohm termination. Gain and termination are set by resistor values (no jumpers). Split termination sets line voltage (preamp board will have current-mode driver).

• Preamp board power and control (if any) on same cables (8 conductors available); preamp power up to 100 mW/ch ok, fused and switchable under software control.

• Record length: Programmable up to 1024 (probably typically use ~100 samples??, cf. Simon's work on FDC proto).

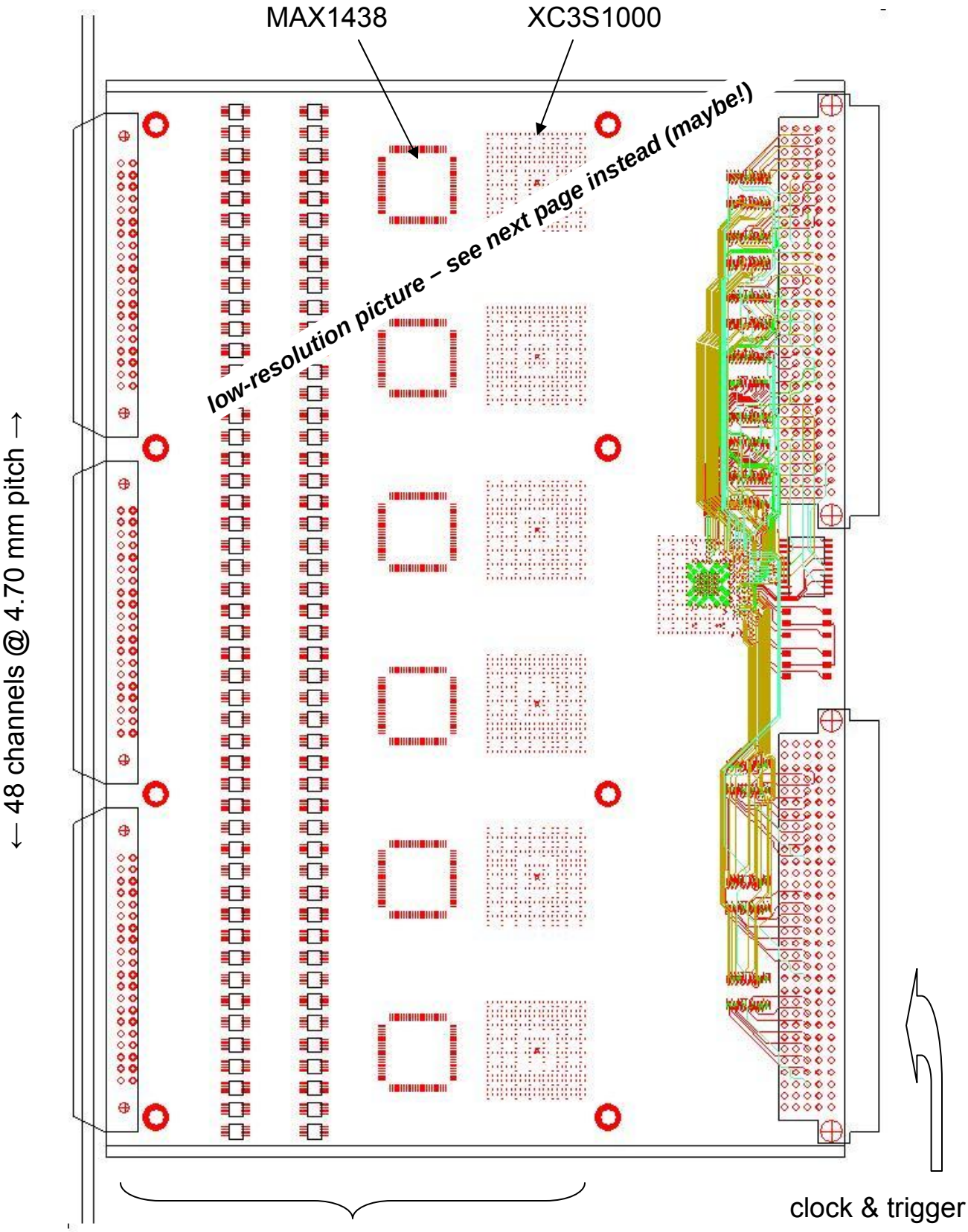
• Readout buffer: At least 2048 samples per channel (~20 events buffered on board @ 100 samples/event) – is this enough?

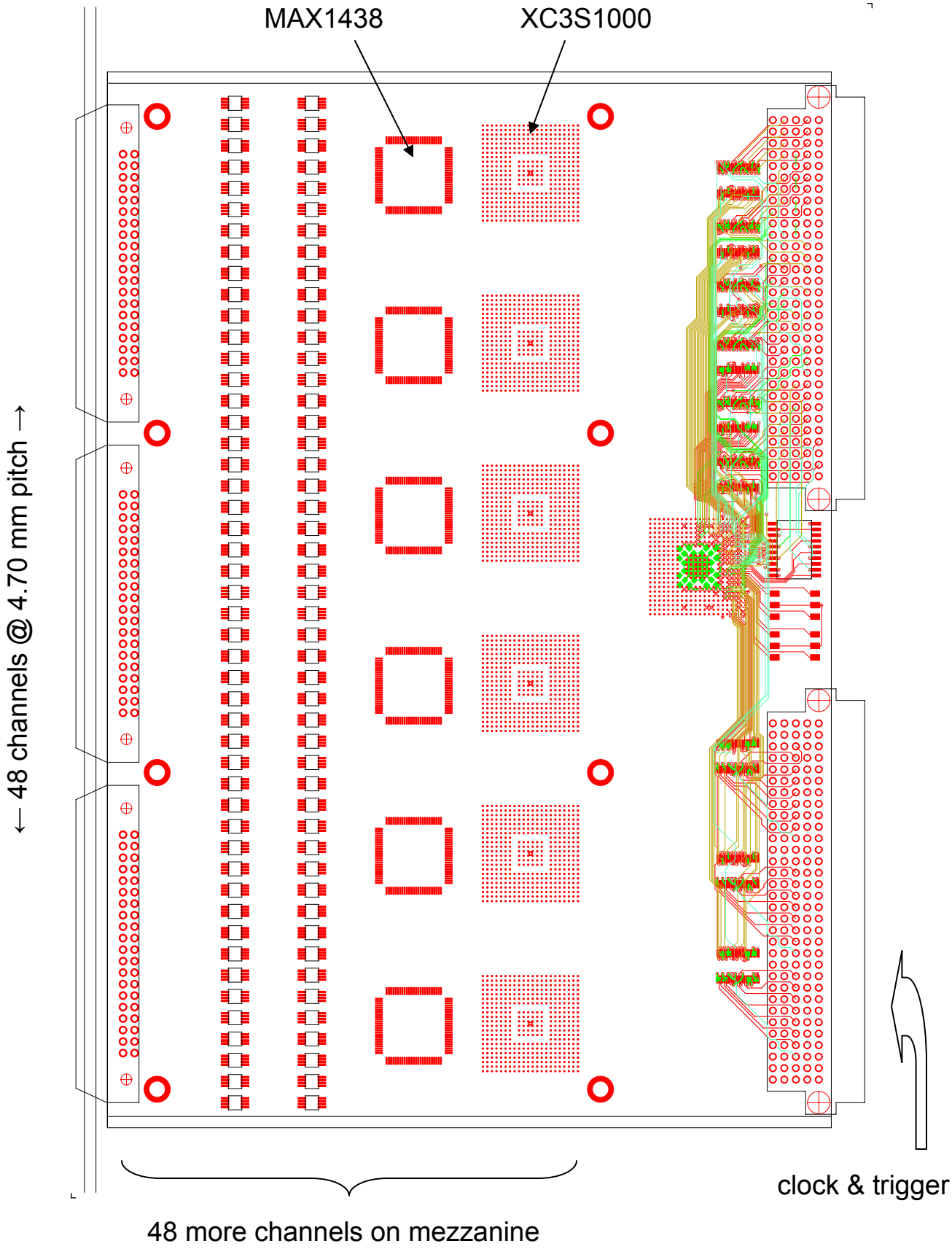
• Triggering: External trigger and event descriptor received from J2 pins (only). Possible internal trigger (digital discriminator) intended for test applications.

• Mechanical/Power: 6U VME, forced-air cooled, DC power mainly from VME64x supply voltages (+5, +3.3, ±12, 48 V, usage TBD); expect about 20 W per board (400 W per crate) + preamp power TBD

• Readout: VME64, 32 and/or 64 bit block transfers supported (~64 MB/s); 2eSST desired??; interrupts on buffer full / almost full

• *First boards planned available around 7/2006*


MAX1438
XC3S1000
low-resolution picture – see next page instead (maybe!)
← 48 channels @ 4.70 mm pitch →
clock & trigger
48 more channels on mezzanine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