Glue-X FDC/CDC ADC Module

Preliminary Specifications

• Resolution: 12 bits

• Sample rate: 65 MS/s (today) – higher sample rate no doubt will be practical in years to come – to be cost effective this board will require high density ADC's, such as MAX1438 [8 ch / 17×17 mm^2 footprint, 11.6 ENOB @ ≤30 MHz, 114 mW/ch]

• Analog pulse shaping: TBD, anything we can do with a few op-amps is fine… Will be coordinated with preamp ASIC & board design.

• Channel count: 96 (1920 ch/crate, FDC → 8 crates)

• Inputs: 16 channels per 40 conductor cable (jacketed shielded twist-n-flat, standard connectors); 1 V (differential) full scale input, 110 Ohm termination. Gain and termination are set by resistor values (no jumpers). Split termination sets line voltage (preamp board will have current-mode driver).

• Preamp board power and control (if any) on same cables (8 conductors available); preamp power up to 100 mW/ch ok, fused and switchable under software control.

• Record length: Programmable up to 1024 (probably typically use ~100 samples??, cf. Simon's work on FDC proto).

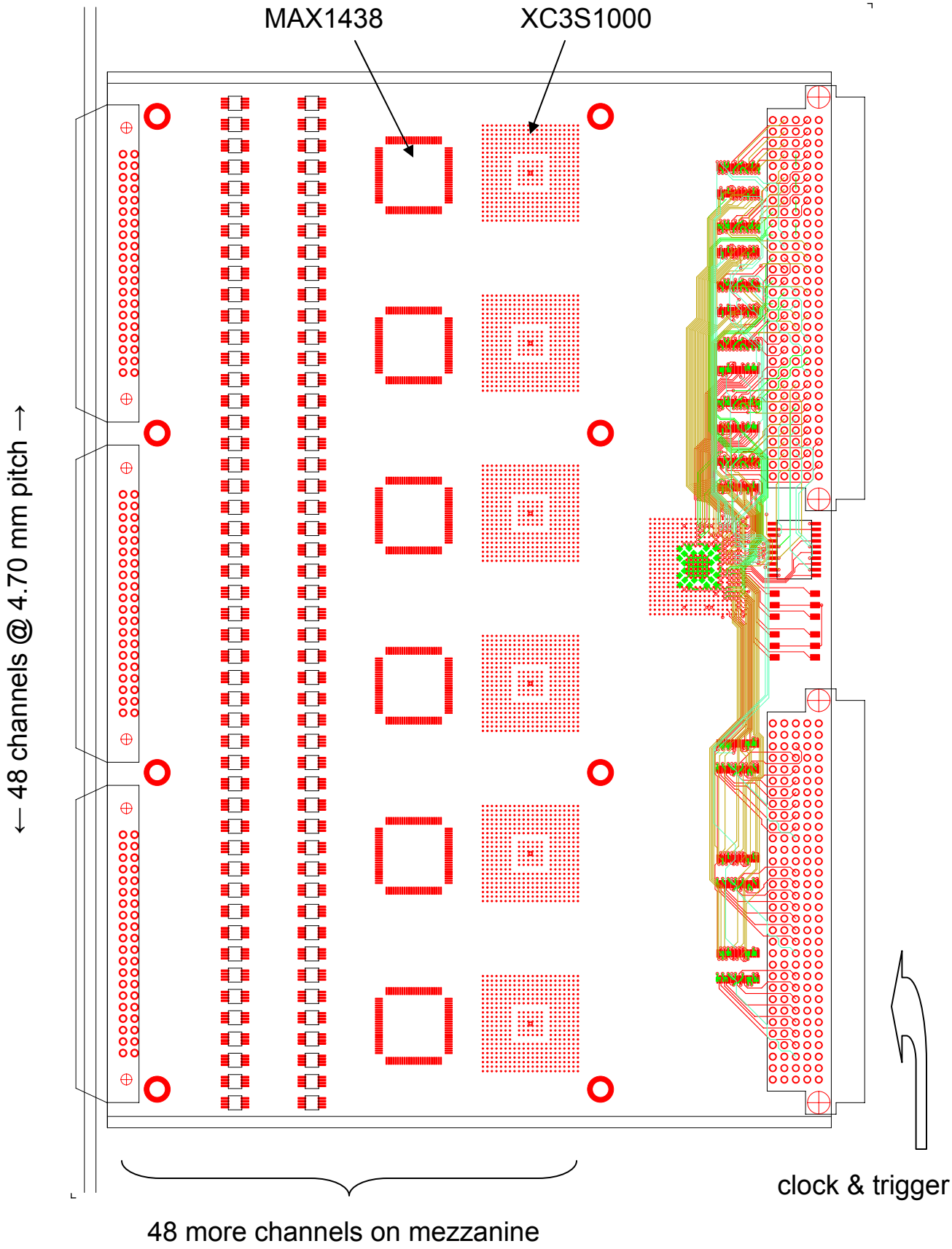
• Readout buffer: At least 2048 samples per channel (~20 events buffered on board @ 100 samples/event) – is this enough?

• Triggering: External trigger and event descriptor received from J2 pins (only). Possible internal trigger (digital discriminator) intended for test applications.

• Mechanical/Power: 6U VME, forced-air cooled, DC power mainly from VME64x supply voltages (+5, +3.3, ±12, 48 V, usage TBD); expect about 20 W per board (400 W per crate) + preamp power TBD

• Readout: VME64, 32 and/or 64 bit block transfers supported (~64 MB/s); 2eSST desired??; interrupts on buffer full / almost full

• *First boards planned available around 7/2006*


MAX1438
XC3S1000
← 48 channels @ 4.70 mm pitch →
clock & trigger
48 more channels on mezzanine

Drift Chamber FADC Board Procured Parts & Contract Assembly Costs
(excludes engineering labor and in-house (IUCF, IU, and/or Jlab) testing and repair

G. Visser, P. Smith, 7/11/2005
G.V. updated 9/21/2005 adding FY06 R&D budget columns and new ADC options
G.V. slightly revised 11/8/2005

Based on installed 14592 channels (4 pkg x 6 layer x (128 anodes + 480 cathodes) *[cable granularity 16]*), + 10% spares, * 1.02 yield factor (unrecoverably damaged boards)
→ → → **IT IS HERE COSTED AT** → → → **16416** channels

Specifications: 12 bit, 65 MSamples/s, >200 MHz bandwidth, >8 us memory depth, deadtimeless readout
NOTE: 10 bit may be sufficient, costs would be reduced, see alternate part below.
Costed assuming 64 channels per 6U VME module w/mezzanine - actual production is hoped to be 96 channels, if feasible (lower cost especially of crates)

Item	Cost ea	Qty/Ch	Cost/Ch	Total Line Cost	Basis	For R&D budget, 5 boards @ 64 ch Cost ea	Qty/Ch	Cost/Ch	Total Line Cost
ADC (ADS5273, 12-bit)	121	0.125	15.125	$248,292	MFG budgetary pricing	160	0.125	20	$6,400
Cable receiver & ADC driver	3	1	3	$49,248	engineering judgement; based on STAR EEMC MAPMT design	6	1	6	$1,920
FPGA (XC3S1000-4FG456C)	63	0.25	15.75	$258,552	distributor web pricing	75	0.25	18.75	$6,000
FPGA for VME logic (TBD - est. as XC3S1000-4FG456C)	63	0.015625	0.984375	$16,160	distributor web pricing	75	0.015625	1.171875	$375
VME bus interface chip (SN74VMEH22501GQLR)	1.87	0.140625	0.262969	$4,317	distributor web pricing	2	0.140625	0.28125	$90
Analog power regulators	60	0.015625	0.9375	$15,390	estimated based on STAR EEMC MAPMT design	50	0.015625	0.78125	$250
Digital power regulators	40	0.015625	0.625	$10,260	estimated based on STAR EEMC MAPMT design	30	0.015625	0.46875	$150
clock & clock distribution	40	0.015625	0.625	$10,260	engineering judgment	50	0.015625	0.78125	$250
input connectors (40C header RA w/latch)	1.54	0.0625	0.09625	$1,580	distributor web pricing	2	0.0625	0.125	$40
VME64 connectors (Harting 02-01-160-1101)	16.93	0.015625	0.264531	$4,343	distributor web pricing	15	0.015625	0.234375	$75
misc. components (mostly R & C)	0.007	36	0.252	$4,137	estimated based on STAR EEMC MAPMT design	0.05	36	1.8	$576
board (main)	150	0.03125	4.6875	$76,950	engineering judgement, toy webquote	500	0.03125	15.625	$5,000
board (mezzanine)	100	0.03125	3.125	$51,300	engineering judgement	300	0.03125	9.375	$3,000
front panel	80	0.015625	1.25	$20,520	taken from PMT FADC estimates	300	0.015625	4.6875	$1,500
contract assembly (main & mezzanine)	300	0.015625	4.6875	$76,950	engineering judgment experience from STAR, discussions w/ Chris Cuevas	600	0.015625	9.375	$3,000
		TOTAL	51.67263	$848,258			**total/ch**	**$89**	
ALTERNATES FOR ITEM 1:									
ADC (ADS5277, 10-bit)	32	0.125	4	$65,664	MFG budgetary pricing				
ADC (MAX1438, 12-bit 65MSPS)	54.85	0.125	6.85625	$112,552		93.25	0.125	11.65625	
ADC (MAXxxx, 10-bit 65MSPS)		0.125							
R&D and NRE Items									
TI eval board						250			$250
Maxim eval board (very nice, with FPGA!)						800			$800
miscellaneous components for prototyping						1000			$1,000
miscellaneous components to interface w/ detector prototypes						2000			$2,000
pcb fab NRE 2x						2000			$2,000
assembly NRE 2x						2000			$2,000
								TOTAL	**$36,676**

General information:
The above is based on using TI's 8-channel ADC chips with serial LVDS output.
At present this is the highest density packaging, with package size of 14 mm square - however it will likely be improved upon in future by other manufacturers.
I am conservatively estimating one FPGA for every 4 channels, although if the processing turns out to be relatively simple it may well be possible to have one FPGA for every 8 channels.

Schedule:
We produced 9,600 channels of "FADC" for the STAR EEMC MAPMT readout in less than 2 years, despite slippage in the availability of funds.
Although this here is 1.5 x as many channels, in STAR it was 4 channels per FEE board, and there were 4 additional supporting boards required (1 @ 16 channels ea, 3 @ 192 channels each), therefore the complexity of the assembly and test effort in STAR exceeded what will be necessary here, and I am 100% confident in completing the build in less than 2 years, including all testing.
Design can also certainly be accomplished within a single year, once the specifications are frozen.