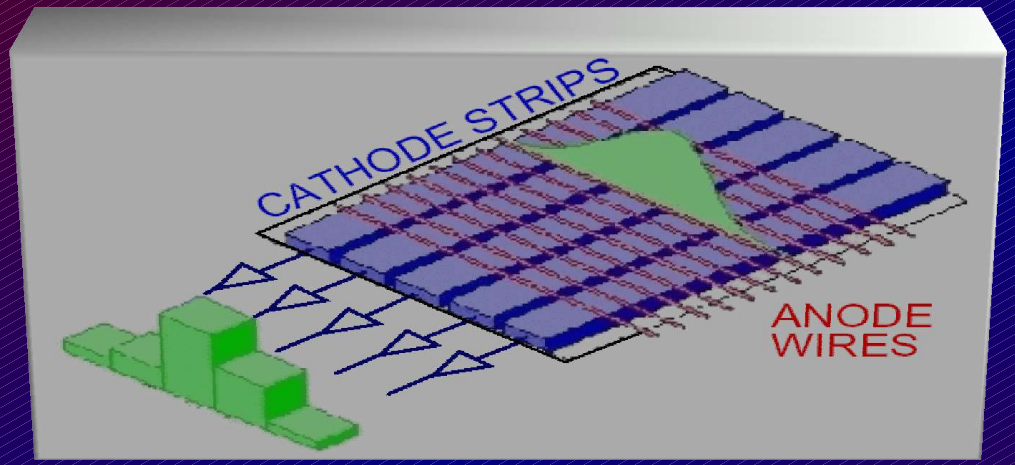
# FDC Status



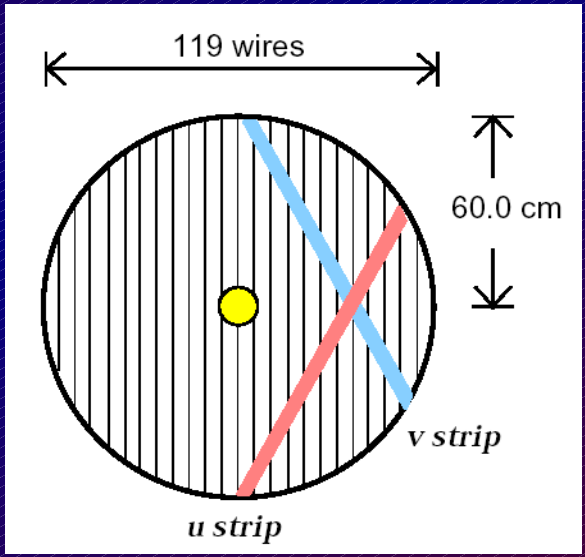

Simon Taylor and Daniel S. Carman
Ohio University

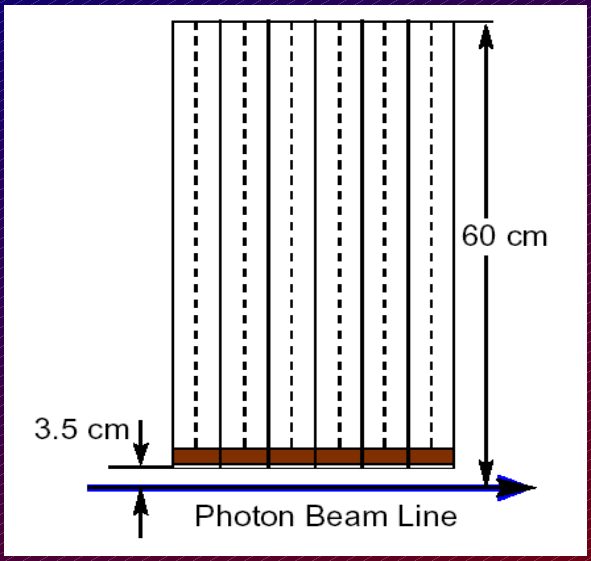
GlueX meeting
November 10, 2005

# Overview

- Purpose: measure momenta of forward-going tracks up to ~20° (relative to photon beam line)
  - Sandwich design: 6 layers/package
    - Each layer: cathode / anode / cathode
    - Cathode planes divided into strips
    - Nominal configuration: read out strips with Flash ADCs, anode wires with TDCs
  - Adjacent layers rotated by 60° with respect to each other
  - 4 packages (currently) equidistant along z

Front



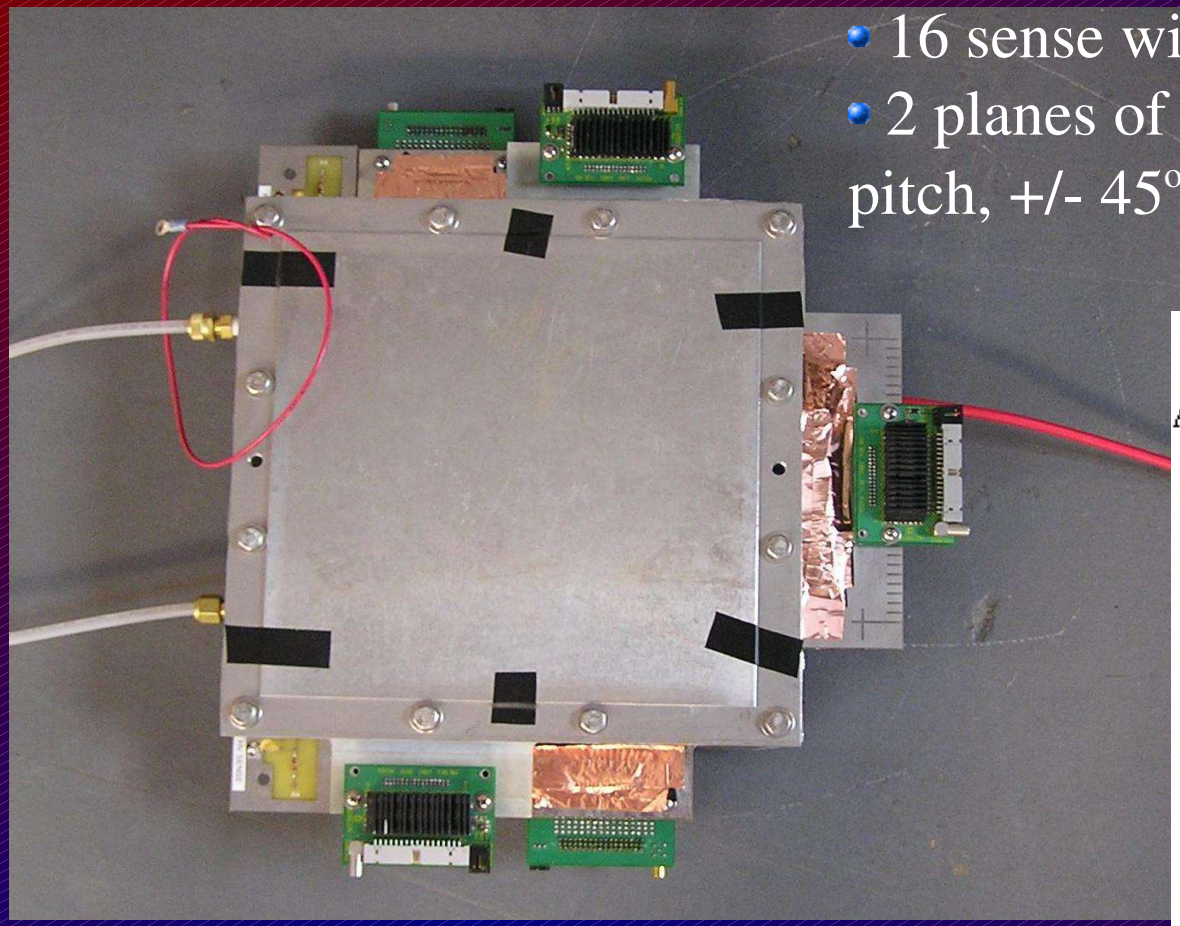




Side

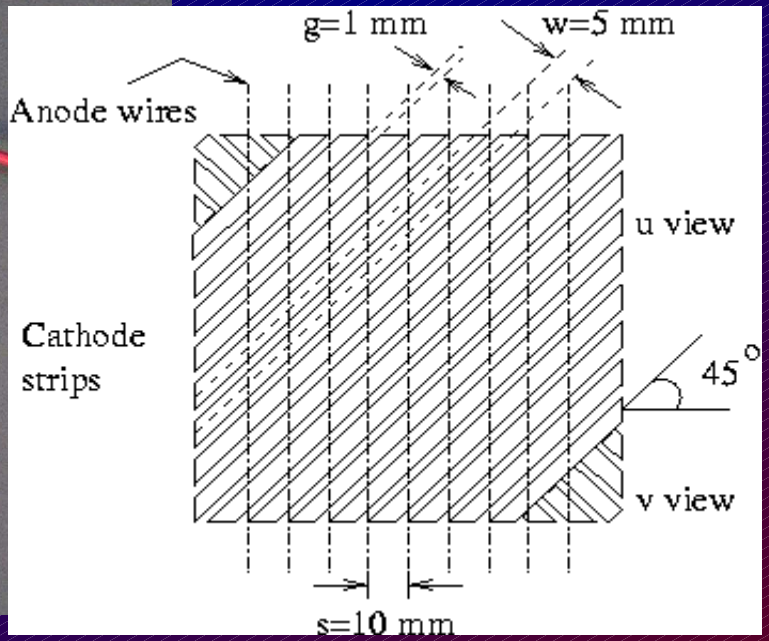
# FDC design parameters as of Oct 24

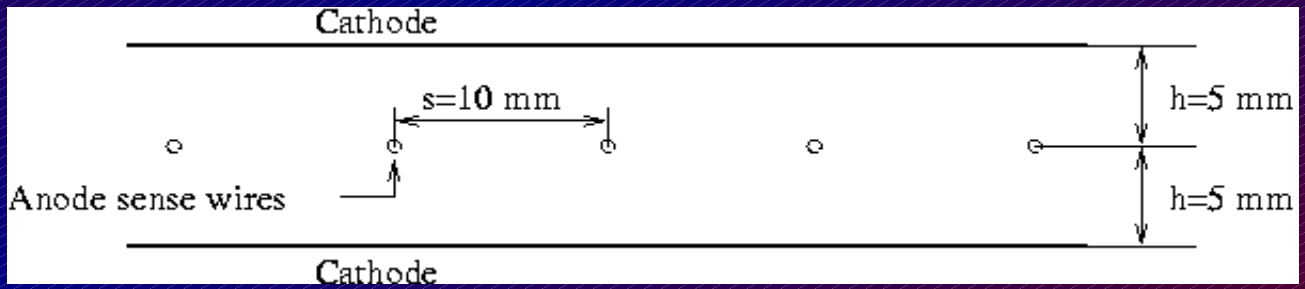
| Parameter | Value |
|---|---|
| Wire spacing $s$ | 10 mm (anode-anode), 5 mm (anode-field) |
| Anode-cathode distance, $d$ | 5.0 mm |
| Cathode readout pitch, $w$ | 5.0 mm |
| Gap between cathode strips, $w_g$ | 1.0 mm |
| Width of cathode strips | 4.0 mm |
| Capacitance between strips | 21 pF/m |
| Total strip capacitance | 56 pF/m + 8 pF |
| Resistance between strips | $\sim$20 M$\Omega$ |
| Anode wire radius, $r_a$ | 0.010 mm |
| Wire capacitance per unit length, $C_0$ | $\sim$9 pF/m |
| Gas gain | $5\times10^5$ |
| Operating voltage at nominal gain | 1800 V |
| Electric field at cathode, $E_c$ | $<$1 kV/cm |
| Electric field on anode wire surface | 280 kV/cm |
| Field-shaping wire radius | 0.040 mm |
| Electric field on field-shaping wire surface | 15 kV/cm |
| Positive ion mobility, $\mu^+$ | 1.3 cm$^2$/V/s |
| Total ion pairs | 94/cm |
| Minimum wire tension | 50 gm |
| Total charge collected | $\sim$15.5 pC |
| Charge collected in 30 ns (%) | $\sim$20% |

# FDC prototype



- 16 sense wires with 10 mm pitch
- 2 planes of 32 cathode strips with 5 mm pitch, +/- 45° with respect to the wires



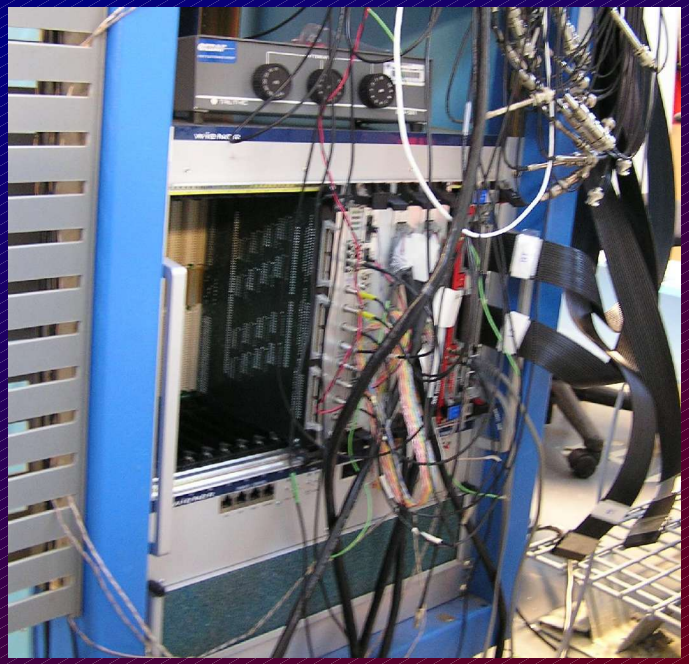



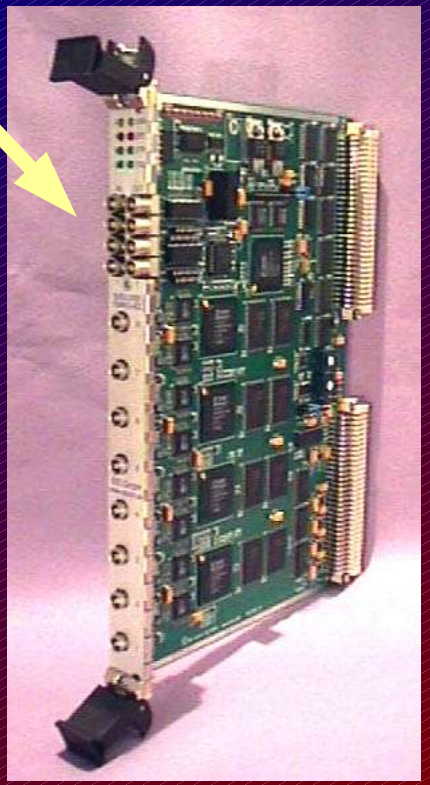

Goal: measure space point with <150 μm resolution in each coordinate

Standard configuration in literature: no field wires...

# Upgrades to FDC daq

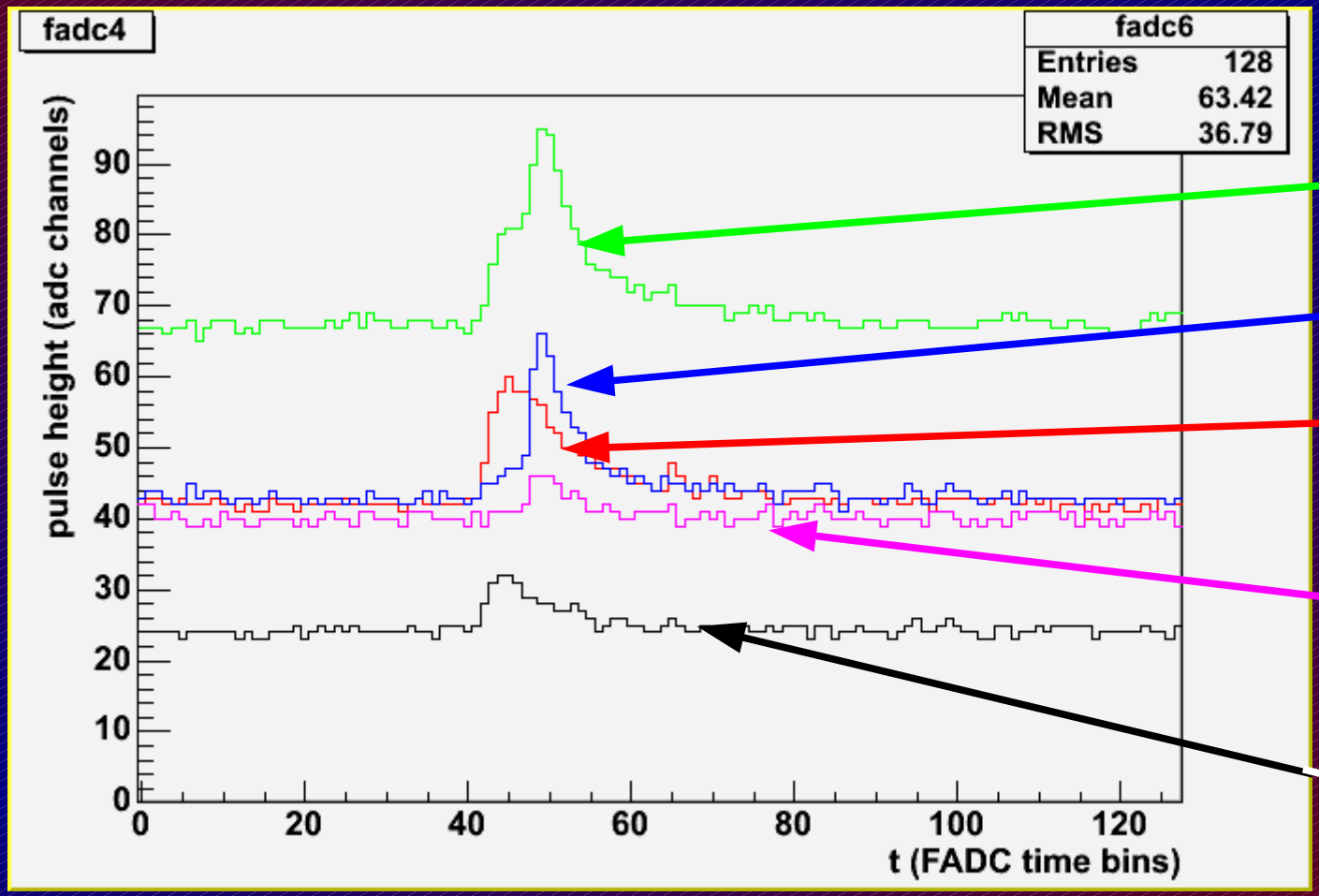
- Readout hardware completely in VME (no more FASTBUS!)
  - Cathode signals integrated using CAEN V792 (charge-integrating) ADCs
  - FDC anode wire timing signals and test stand chamber signals digitized using F1 TDC modules
  - Some cathode signals read out with Struck SIS3300 FADC
    - 8 channels @105 MHz per channel
    - (1 MHz - 105 MHz configurable)
    - 2 banks x 128K samples/channel memory
    - 0 $\leftrightarrow$ -5 V input range





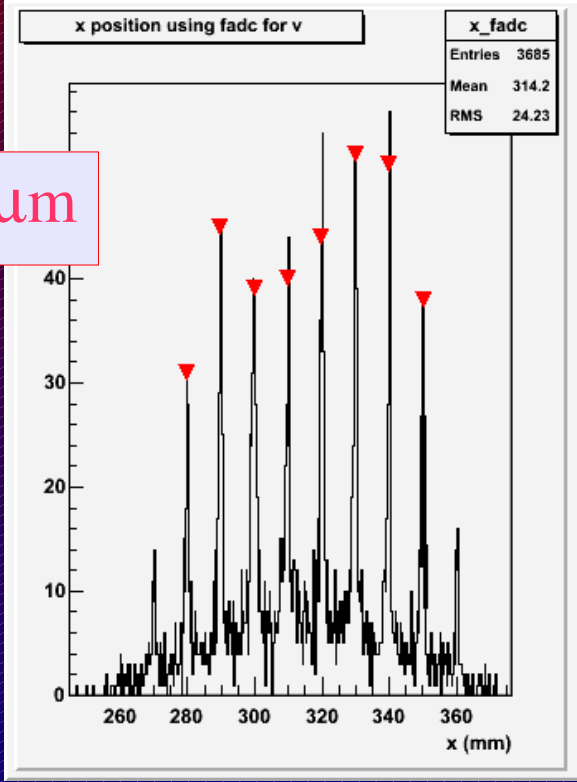
# Sample Event with FADC readout

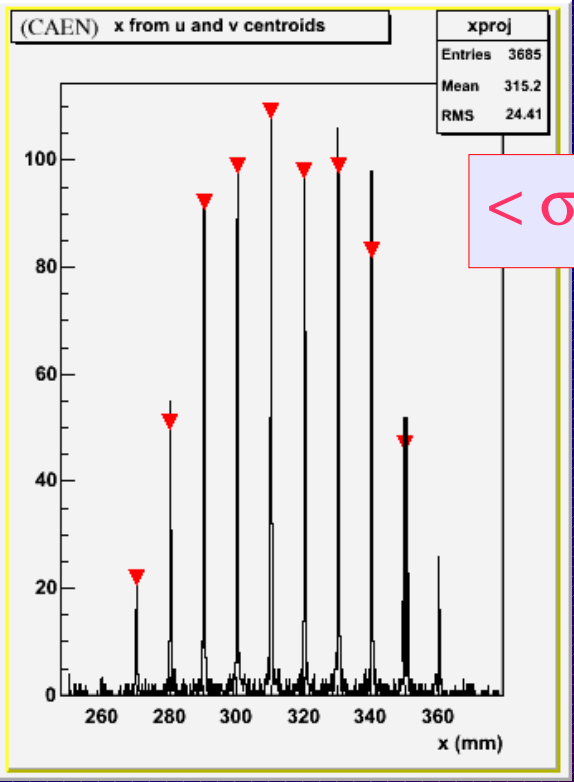
Six adjacent strips (11-16 on bottom view) read out with Flash ADCs.
(minimum postamp gain for comparison to previous data)



# Position resolution (no cut on #wires)

$< \sigma_x >$=549.3 μm




$< \sigma_x >$=173.2 μm

FADC readout for one view

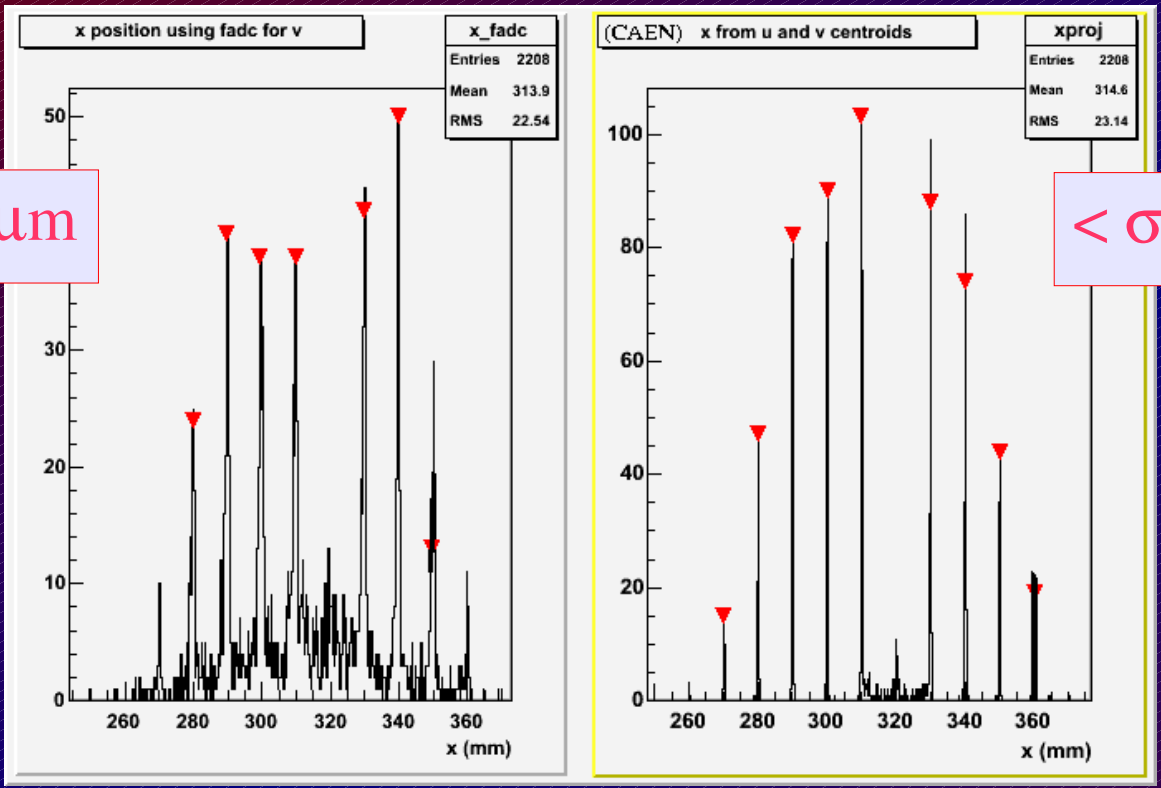
CAEN readout for both views

VPI postamp set to minimum gain (≈1)

| x (mm) | $\sigma_x$(with FADC)($\mu$m) | $\sigma_x$ (w/o FADC)($\mu$m) |
|---|---|---|
| 270.1 | 660.8 | 175.5 |
| 280.1 | 464.1 | 174.3 |
| 290.2 | 558.8 | 168.5 |
| 300.1 | 630.1 | 176.9 |
| 310.1 | 672.2 | 199.5 |
| 320.1 | 682.5 | 171.8 |
| 330.2 | 487.3 | 149.8 |
| 340.2 | 373.3 | 161.7 |
| 350.2 | 427.1 | 180.5 |
| average: | 549.3 | 173.2 |

# Position resolution (one wire required)

$< \sigma_x >$=505.8 μm




$< \sigma_x >$=151.5 μm

FADC readout for one view

CAEN readout for both views

VPI postamp set to minimum gain (≈1)

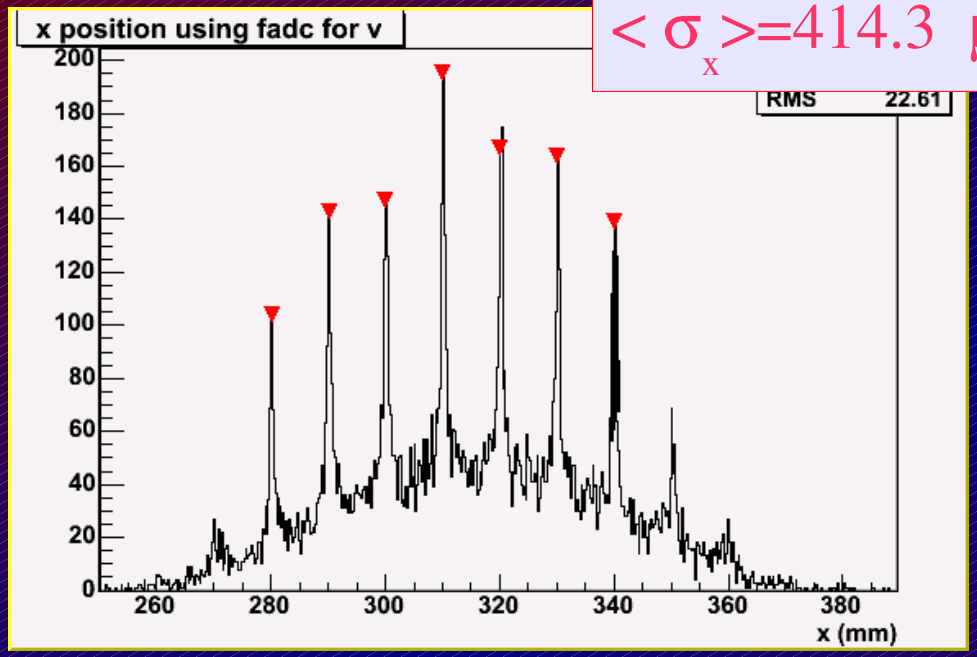
| x (mm) | $\sigma_x$(with FADC)($\mu$m) | $\sigma_x$ (w/o FADC)($\mu$m) |
|---|---|---|
| 270.1 | 398.6 | 159.0 |
| 280.1 | 560.6 | 150.9 |
| 290.1 | 489.1 | 156.6 |
| 300.1 | 760.0 | 162.9 |
| 310.2 | 644.5 | 175.6 |
| 330.2 | 444.0 | 145.6 |
| 340.2 | 349.6 | 150.3 |
| 350.2 | 640.6 | 144.4 |
| 360.2 | 265.8 | 117.8 |
| average: | 505.8 | 151.5 |

Design resolution achieved!

# Effect of increasing postamp gain

Increased postamp gain to maximum for strips read out by FADC

- Postamp gain ~ 6-8

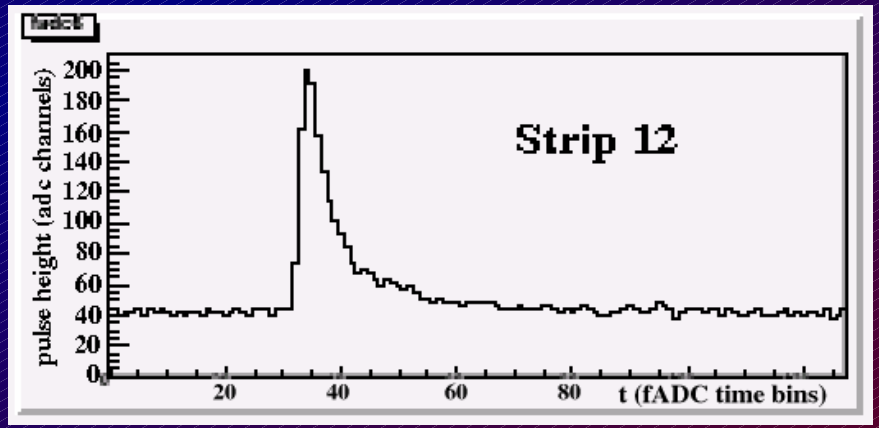



$< \sigma_x >$=414.3 μm ← compare to 549.3 μm

No cut on # of anode wires

| x(mm) | $\sigma_x(\mu m)$ |
|---|---|
| 280.1 | 362.6 |
| 290.2 | 457.1 |
| 300.1 | 397.2 |
| 310.1 | 394.4 |
| 320.2 | 403.3 |
| 330.2 | 477.9 |
| 340.2 | 407.7 |

Sample FADC distribution:



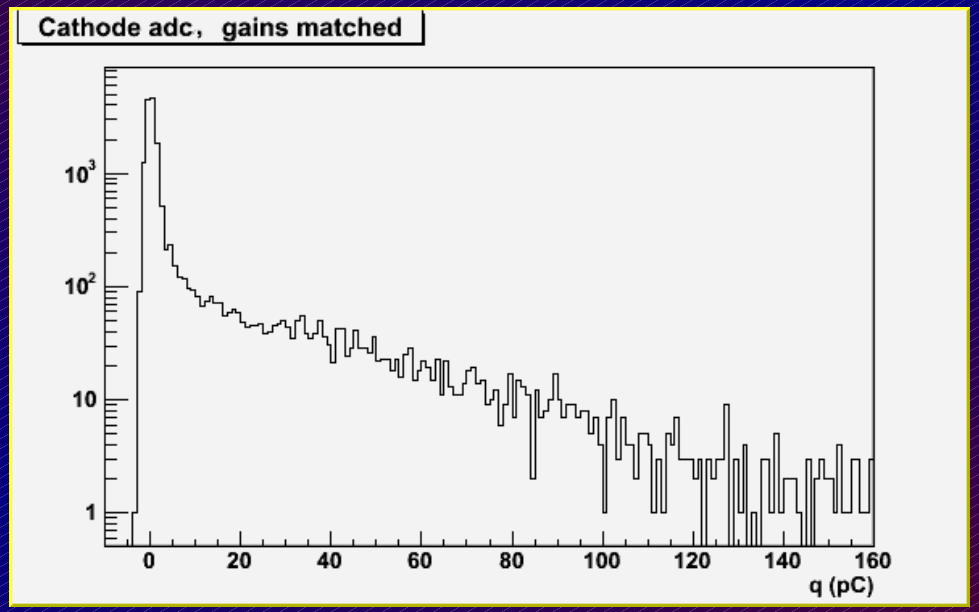

Pulse heights still cover small fraction of 12 bit range

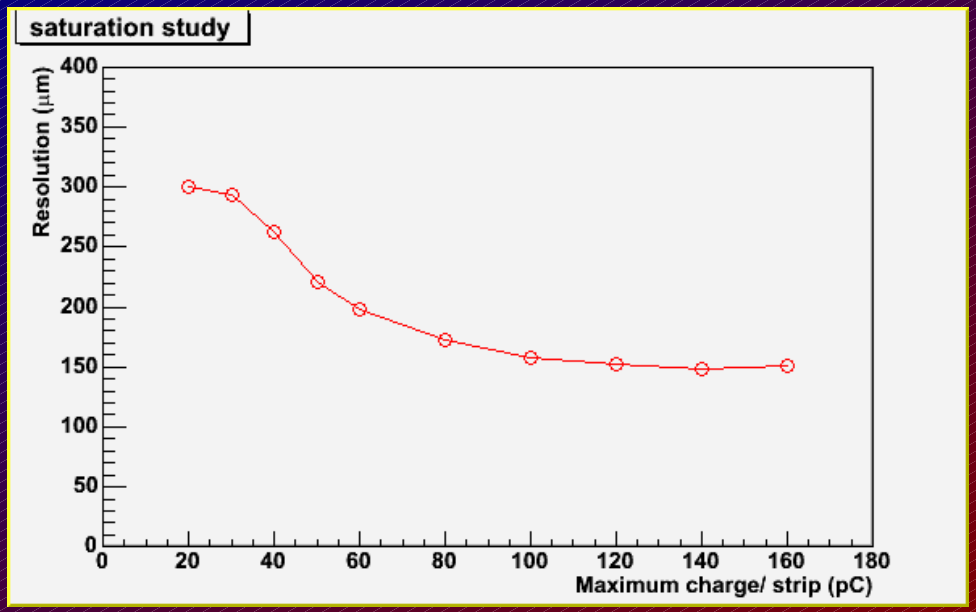
→ modify input range of FADC (to 0 ↔ -0.5 V?)

# Charge saturation study

Studied effect of “clipping” of cathode strip signals

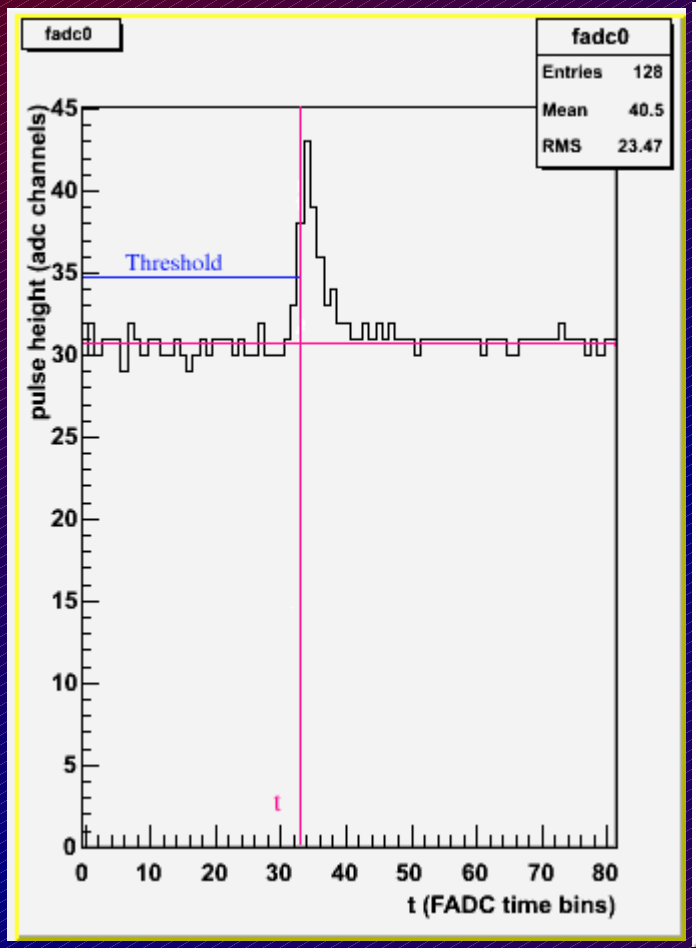
- Varied maximum charge allowed per strip
- Strip charge set to maximum if it exceeds this threshold
- Used CAEN ADCs for both views
- Required only one anode wire/event

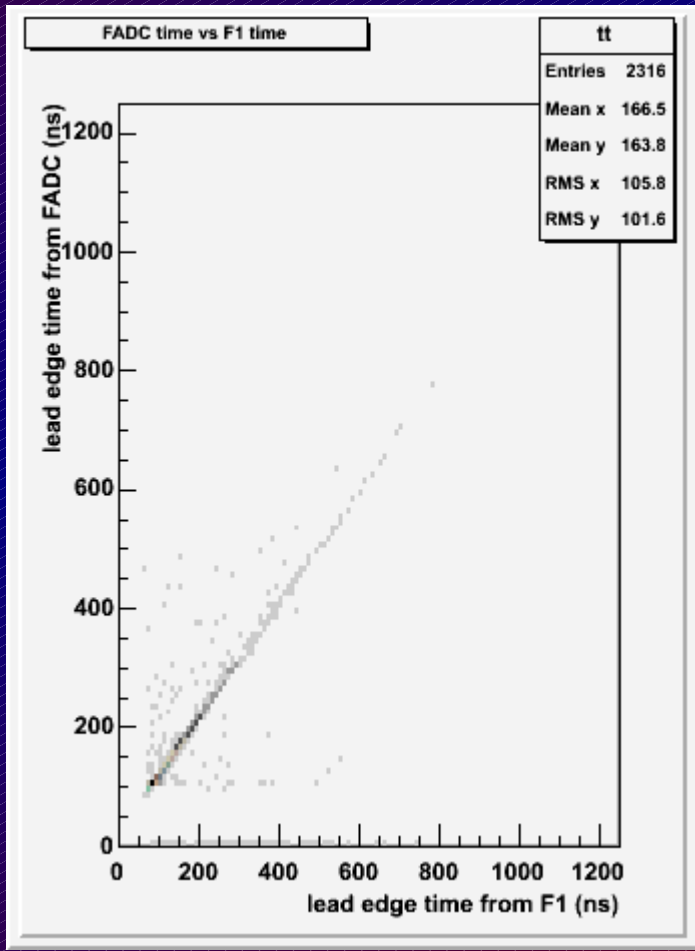


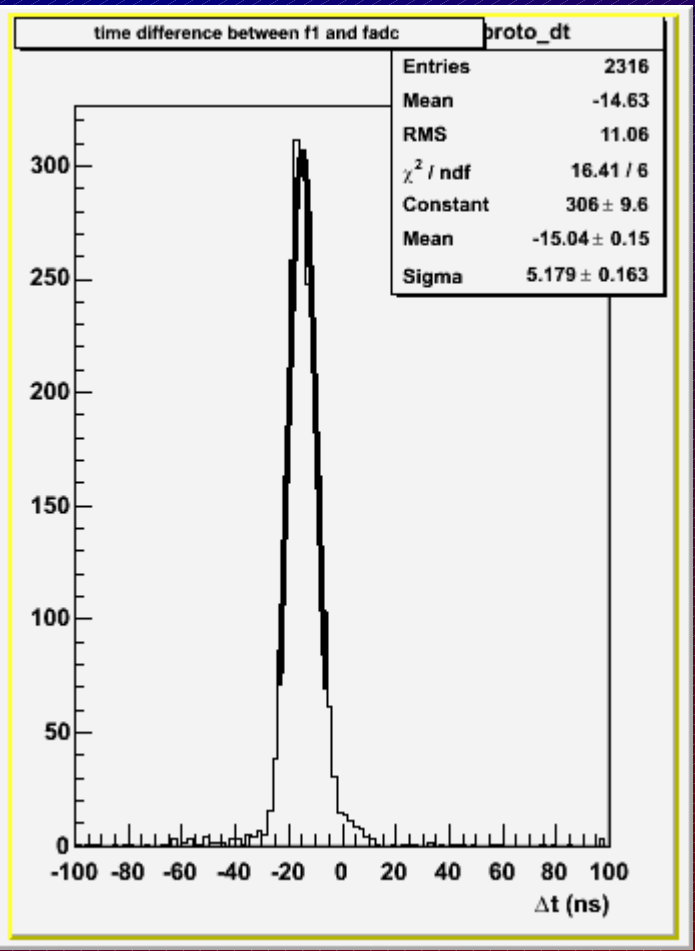



# Leading-edge timing for Wire 11

- Used low gain output of postamp for flash ADC
- Flash ADC time: center of bin at which pulse height exceeds 4 counts above background.
- Compare to time from F1 TDC using leading-edge discriminator



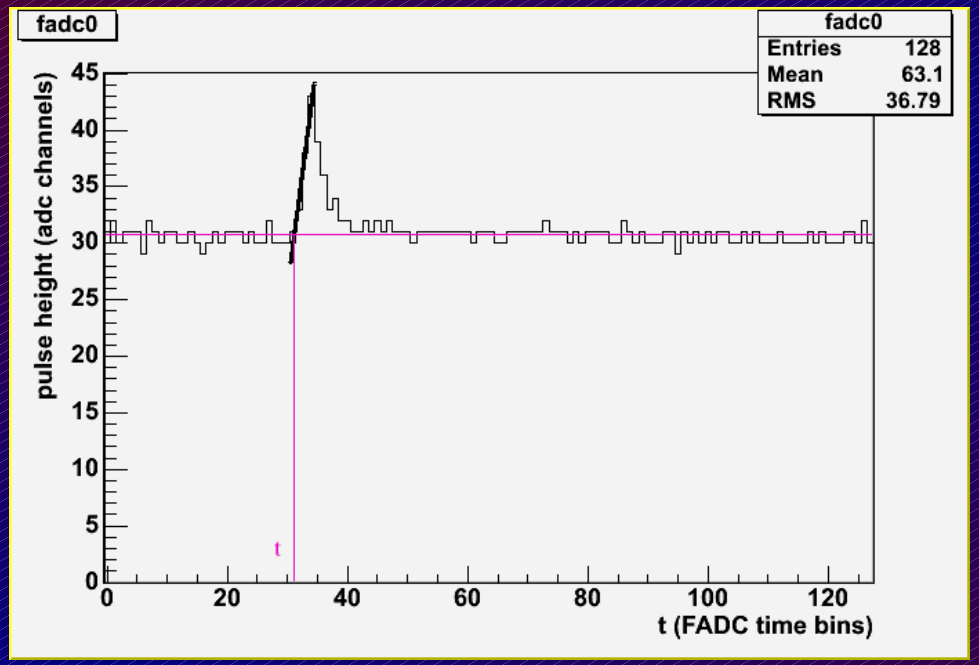



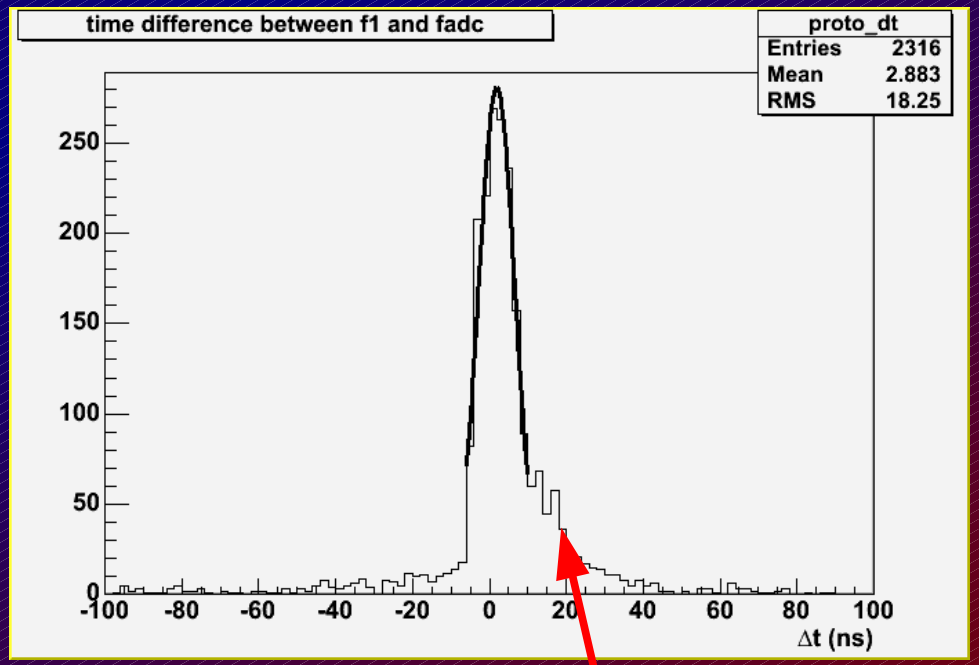

Resolution of timing peak ~ 5.2 ns...

# Wire 11 timing, method 2

Linear fit starting at time bin containing maximum amplitude and 2 bins before, extrapolate to point where line crosses background level.

Same postamp gain condition as before



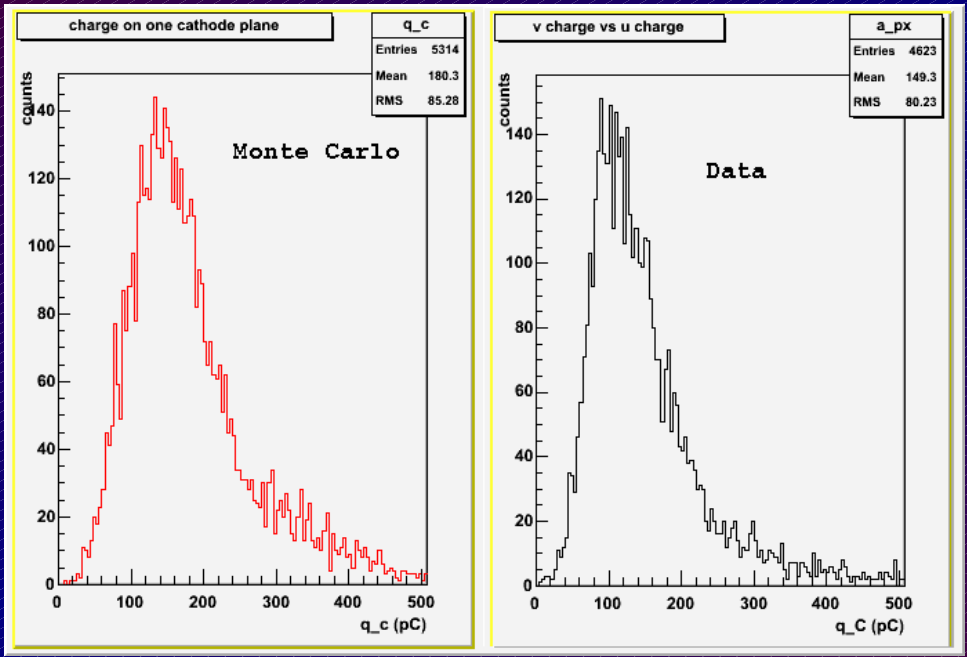




Asymmetric tail...

Resolution ~ 4.7 ns, no better than simple leading edge method

# Monte Carlo development

- Modifications to HDGeant:
  - Approximation for ion-pair statistics → Compound Poisson Distribution
    - Ignore time-development of anode signal
  - Gas gain based on prototype studies using Sauli gain formula
  - Induced charge on cathode planes based on Gatti/Mathieson formula
    - Overlapping distributions summed in strips where overlap occurs




Induced charge on one cathode plane
(~minimum ionizing particles)

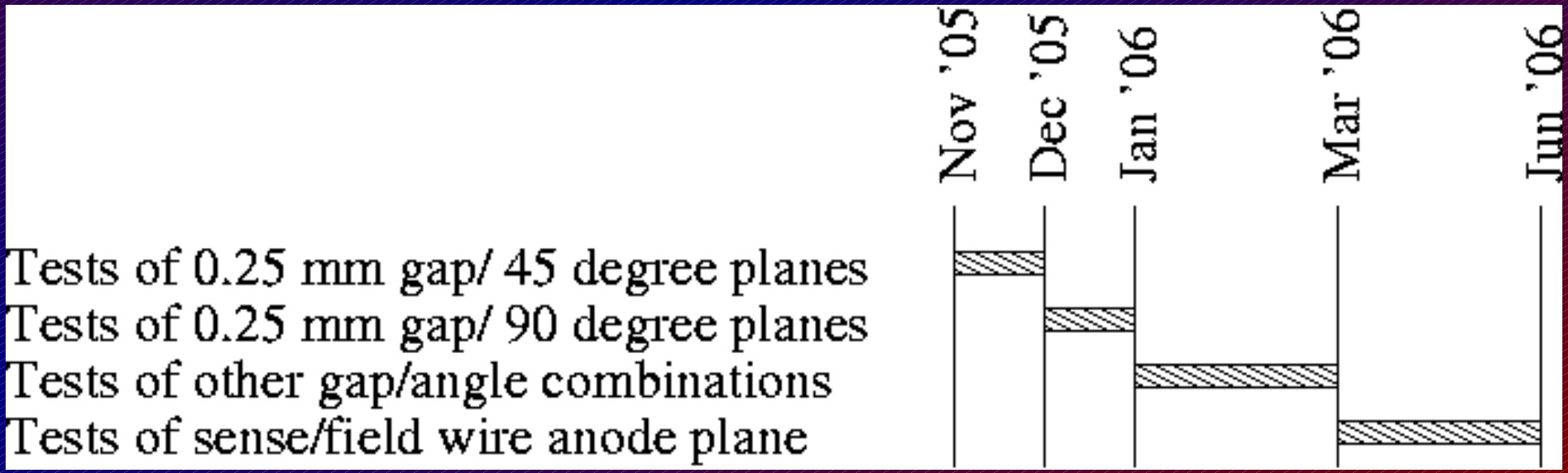
Purpose: to provide more realistic hits for development of FDC reconstruction algorithms and for use in tracking instead of cheat hits...

# Electronics meeting at Ohio U.

- GEANT simulations (Ryan Mitchell) → factor for estimated range of expected signals:
  - CDC=30, FDC anodes=10, FDC cathodes=100
- Need full simulation: track through gas volume → clumped ionization → drift trajectories → current waveforms
  - Optimize preamp shaping time / sampling rate / bit depth
- Want dE/dx information from FDCs to plug PID holes
  - Problematic to use cathodes?
  - Recommended instrumenting anode readout with Flash-ADCs
- Timing: goal = 2 ns resolution → need 125 Msample/s FADCs?
- Gerard Visser: preliminary design for 65 Msample/s FADC
  - 96 channels in 6U VME64x module
- Proposed purchase more Struck FADCs for prototype studies
- Full scale FDC prototype design: how make/support cathode planes?

# Plans for immediate future

- Study different gap configurations (gap between cathode strips)
  - Compare 1 mm gap to 0.25 mm (currently in place) and 0.5 mm
- Study different strip orientation (45° w.r.t. wires or 90° w.r.t. wires?)
  - 0.25 mm gap with 90° orientation next set to be studied
- Study different wire plane configuration (alternating sense/field wires)
  - Repeat tests with various cathode planes
  - Can we obtain same resolution as for sense-wire only configuration?

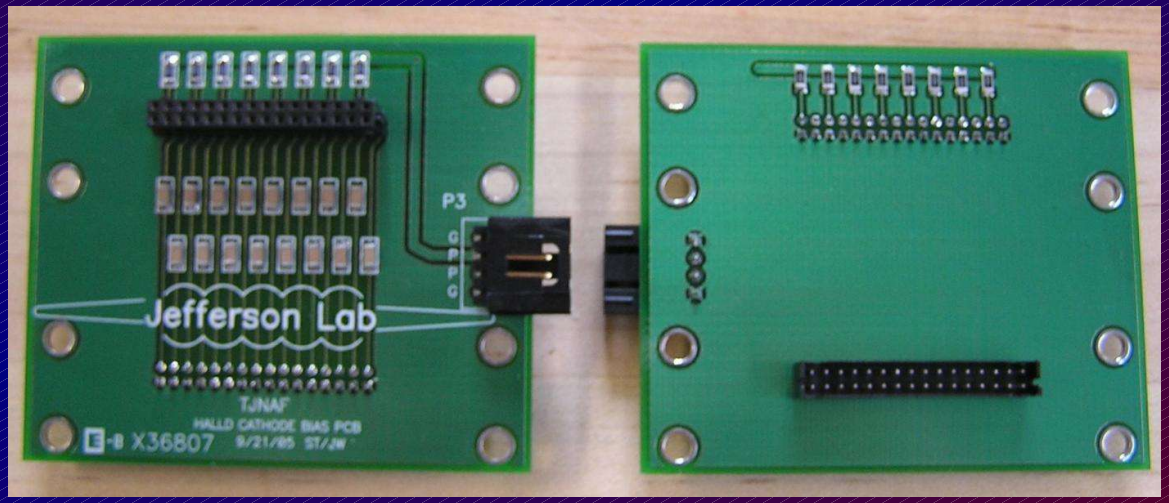


# Biasing the cathode boards

Planned anode plane configuration: both sense and field wires

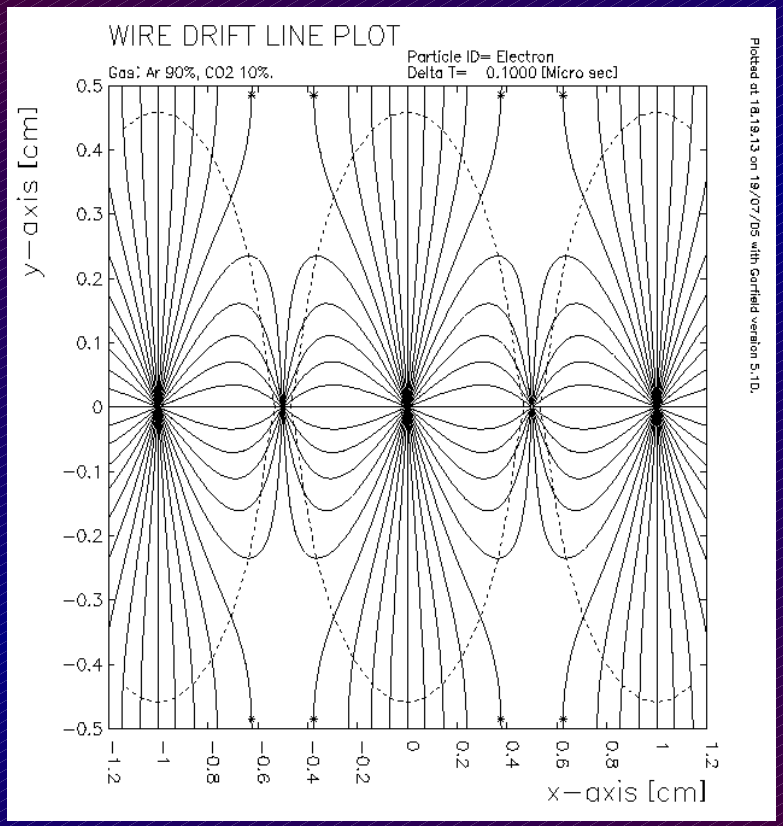
- For optimal electric field configuration, need to bias cathode planes

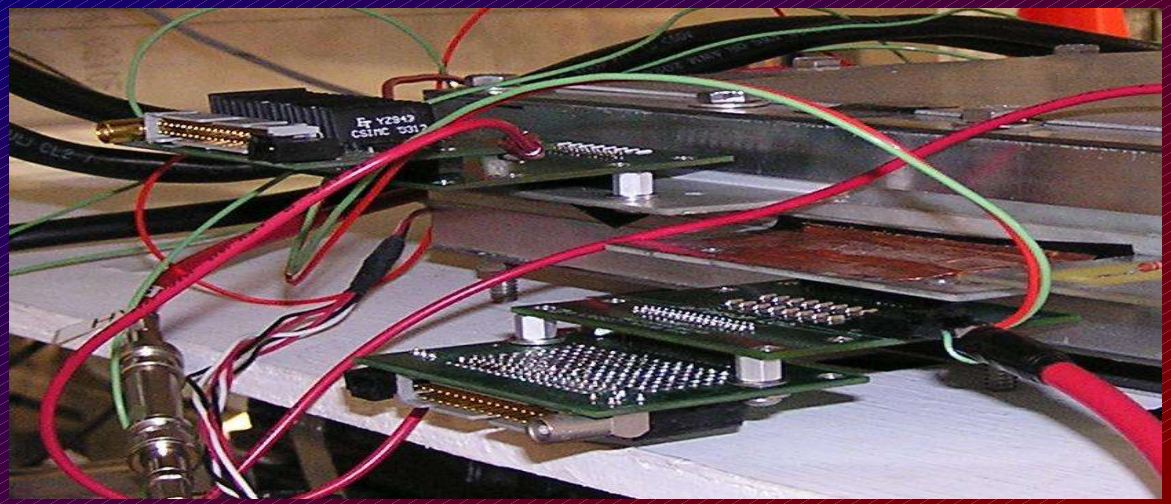
Intermediate board designed by Jeff Wilson:




Garfield calculation with

$V_s$=+1500 V, $V_f$=-750 V, $V_c$=-200 V

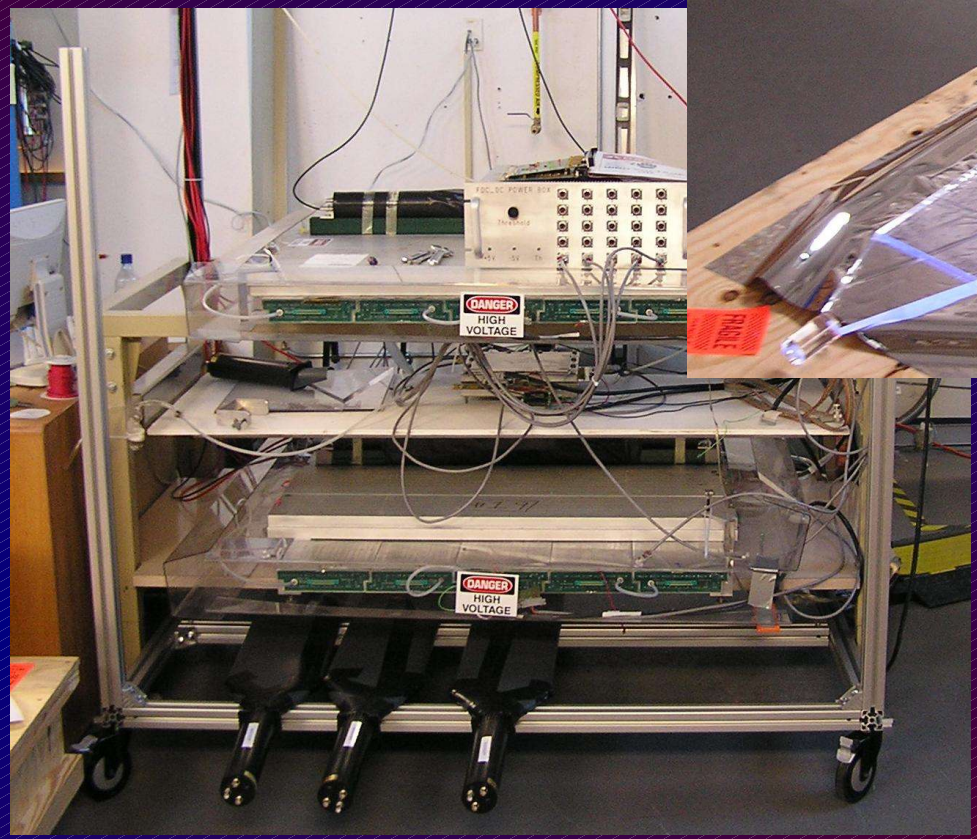


# Scintillator hodoscope upgrade

12 scintillator array under construction

- Each scintillator = 1.3 cm × 20 cm × 120 cm
- 6 above prototype, 6 below
- Designed to cover 1.2 m diameter full-scale FDC prototype
- Plan: study resolution vs. angle of incidence





New HV mainframe:

# Three-year plan

- Stage I: detailed studies of small-scale prototype
  - Goal: optimize chamber electrode structure to satisfy resolution requirement
  - Define chamber pulse characteristics
  - Define necessary electronics capabilities
  - Define operating points for different gas mixtures
  - Time frame for completion ~ 1 year
- Stage II: design and construction of full-scale prototype
  - Determine method for supporting cathode strips over 1.2 m with ~50 μm level flatness
  - Complete circuit board design
  - Cosmic ray tests with wide trigger scintillator coverage
  - Tests in magnetic field
  - Beam tests for dE/dx studies
  - Time frame for completion ~ 3 years
- Personnel: Simon Taylor and Daniel S. Carman, Ohio U.
  - Need additional design manpower to complete project within time frame!

# Backup slides

# Cathode charge after amplification

$$\mathcal{Q} = N_{ion} \cdot F_{att} \cdot F_{ind} \cdot F_{sh} \cdot \mathcal{G}_{amp} \cdot \mathcal{G}_{gas} \cdot 1.60 \times 10^{-19}\ \mathrm{C/e.}$$

- Estimate from Sauli: $N_{ion} = 94$ ion pairs/cm (minimum ionizing particles)
- $1\text{-}F_{att}$ = fraction of drift electrons lost due to reattachment to chamber gas molecules. Assume $F_{att}=1$ (pure $ArCO_2$ gas)
- $F_{ind} = 0.5$, fraction of anode charge induced on one cathode plane
- $F_{sh}$ = fraction of anode charge collected for a given pre-shaping time
  - Assume $F_{sh}=1$ (no pre-shaping currently used)

- Electronic amplification: assume postamps have gain of 1.

Preamp gain: $$\mathcal{G}_{amp} = 2.2\ \mathrm{mV}/\mu\mathrm{A} \cdot \frac{1}{50\ \Omega} = 44$$

# Estimate of gas gain

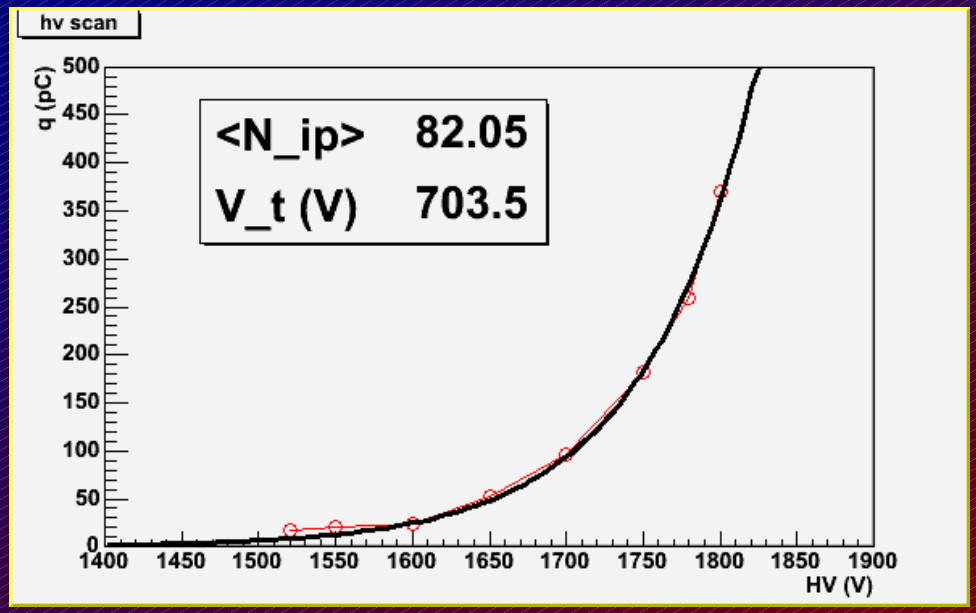
$$\mathcal{Q} = N_{ion} \cdot F_{att} \cdot F_{ind} \cdot F_{sh} \cdot \mathcal{G}_{amp} \cdot \mathcal{G}_{gas} \cdot 1.60 \times 10^{-19}\ \mathrm{C/e.}$$

Gas gain from Sauli and fit to prototype data:

$$\mathcal{G}_{gas} = \exp\left[2\sqrt{\frac{kNCV_0 a}{2\pi\epsilon_0}}\left(\sqrt{\frac{V_0}{V_T}} - 1\right)\right]$$

- $V_0$=operating voltage=1.8 kV
- $V_T$=threshold voltage

- a=0.001 cm = anode wire radius
- k=1.8 ×$10^{-17}$ $cm^2$/V
- N=2.42 ×$10^{19}$ molecules/$cm^3$ (30ºC)
- $\varepsilon_0$ = 8.85 pF/m
- C= 8.34 pF/m




Gas gain = 4.7 ×$10^5$

# Cathode charge before amplification

$$Q_{cathode} = N_{ion}\, F_{ind}\, G_{gas} \times 1.6 \times 10^{-19}\ C = 94 \times 0.5 \times 4.7 \times 10^{5} \times 1.6 \times 10^{-19}\ C$$

$$= 3.53\ pC$$

(after preamp/postamp = 155.3 pC)

Assuming that most of charge is distributed over 3 adjacent strips:
Estimate for "typical" charge on a strip for single tracks = 1.18 pC