9 November 2005

# Minutes of GlueX Electronics Meeting at Jefferson Lab

Present:

IU: P. Smith (scribe), Ryan Mitchell

JLab: Chris Cuevas, Dave Abbott, Ed Jastrzembski, Fernando Barbosa, John Musson, Elton Smith

UConn: Richard Jones

Ohio: Simon Taylor

CNU: Dave Doughty, Walt Miller

IUCF: Gerard Visser (by phone)

Chris Cuevas presented the costs of a small VME test crate:

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| 8 slot VME64X: | $3K |
| CPU: | $3K |
| Trigger interface: | $1K |
| Trigger/Clock dist: | $1K |

The JLab F1 TDC boards are about $3.7K each. To get this price, about 25 need to built in a batch.

The first JLab 250 Msps flash ADC prototype board is scheduled for the summer of 2006. Boards are expected to be available for GlueX tests in late 2006 or early 2007. The estimated cost is $4K per board.

The VXS implementation of the energy sum will require Xilinx 4VFX20 chips. The version of this chip which supports 10 gigabits per second serial transceivers has been delayed by Xilinx, but slower versions are available now for testing.

One new feature of the JLab FADC board are DACs used to control input offsets.

Elma has quoted a 21 slot VXS crate at ~$10K.

Gerard presented his preliminary design for a 65 Msps FADC intended for digitizing FDC cathode signals. The expected density is 96 channels on a 6U board - 48 channels are on the main board, and 48 channels are on a mezzanine. Connections to the chamber preamps are through a 40 conductor shielded, jacketed, twisted pair cable. 8 conductors are available for power, control, and test signals. 32 conductors bring in the differential signals from 16 channels. This cable needs to go into the mechanical design of the FDC and support structure and clearance for it allowed for.

Gerard's estimate of costs are $89/channel for the R&D quantity of 5 boards, and $52/channel for production quantities. More details are in GlueX-doc-541. Gerard believes about 20 events can be buffered in the FPGA memory. This is probably inadequate for GlueX; more like 200 events need to be buffered to keep the CPU interrupts at a manageable rate. Gerard will look into this further, and add FIFOs if necessary.

There is no particular reason the 65 Msps sampling clock needs to be synchronized to the accelerator clock.

John Musson stated that the JLab master oscillator of 1497 MHz is always on. The timing jitter is about 1 ps which is equivalent to 1 degree of phase. The upgrade will distribute accelerator timing signals on single mode fibers - this technique has been demonstrated to have jitter of 100 - 300 fs.

Fernando Barbosa stated the jitter specification for the 12 bit version of the 250 Msps convertor chips is 300 fs.

Gerard briefly described the STAR scheme for event ID - 20 bits are distributed for every beam crossing which includes a 12 bit "token" and an 8 bit "action" fields.

The current plan for GlueX event ID is based on the F1 TDC chip implementation; each board has a trigger counter, and a channel based time counter (this is the ring buffer address in the FADCs). This time counter "stamps" the arrival time of the trigger, and if the time stamps from different channels don't agree the event is corrupt.

There was more discussion of the pros and cons of phase locking the TDC and ADC clocks to the accelerator. John Musson proposed a signal from a beam current monitor could be used to phase lock a clock derived from the master oscillator to the actual arrival time of the electrons.

The other possibility for GlueX is to monitor the beam timing in a TDC and ADC channel. The arrival time of electrons can then be subtracted from measured time in the analysis. There was agreement that these schemes can and should be tested in Hall B soon by instrumenting the Hall B tagger with the JLab F1 TDC.

There was some discussion of “civil” issues relating to the Hall D complex. It was agreed that no “extra” grounding between the various buildings was desirable. All interconnections between buildings will be via fiber optic cables. Pipes should be provided for these interconnnections - the number and size need to be determined soon. Paul showed a sketch of the GlueX rack layout which had the racks moving along with their associated detectors. (See GlueX-doc-543) Either this scheme or one in which the detector cables have sufficient slack needs to be settled on and designed soon. The intent is to be able to operate the various GlueX detectors in their extracted positions without uncabling. There was a preference for the moving rack solution since this minimizes overall cable length, although this introduces other issues; the power cables need slack in this scheme for example. The idea of cable trenches in the GlueX floor was discussed and thought to be undesirable; the preference is for overhead cable trays. There should be pipes for fibers from the Hall D detector building into the counting house, and at least one pipe for fibers from the tagger building to the detector building.