GlueX Electronics Status Report

6-7 April 2006
Indiana University

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Physics Division
Group Leader -- *Fast* Electronics

Topics:

- Flash ADC
- VXS
- Schedule

Flash ADC Development

- Requirements for a new Flash ADC module have been developing for over a year.
- Hall groups understand the cost savings of replacing aging and obsolete FastBus ADCs with a new design. Examples:
  - F1TDC replaces single hit 1872A
  - Flash ADC will replace 1881.
  - Flash ADC will eliminate signal delay cables and provide 'pipelined' data directly from detector electronics
  - Flash ADC specifications and detailed requirements are a 'work in progress'. ADC information can be processed and used in Level 1 trigger systems, and design will depend on further simulation efforts.

Flash ADC Development

- Requirements have been received and reviewed from:

  Hall A – DIS Parity Experiment [E05-007]

  Hall B – No formal written requirements, however they are interested in the summing features for the calorimeter and to eliminate Fastbus 1881 modules

  Hall C – Spin Asymmetries of the Nucleon Experiment [SANE]

  GlueX – Chapter 7

Flash ADC Development

- "Converting" the requirements to schematics and copper layout is always the most time consuming part of the total design.
- Many of the requirement documents do not list summing, but the final board must be able to include this feature for GlueX.
- The prototype fADC will be designed to test as many requirements as possible, and provide valuable experience with new technology [VXS], and some of the latest Fpga devices, simulation & verification tools.

Flash ADC Status - Prototype

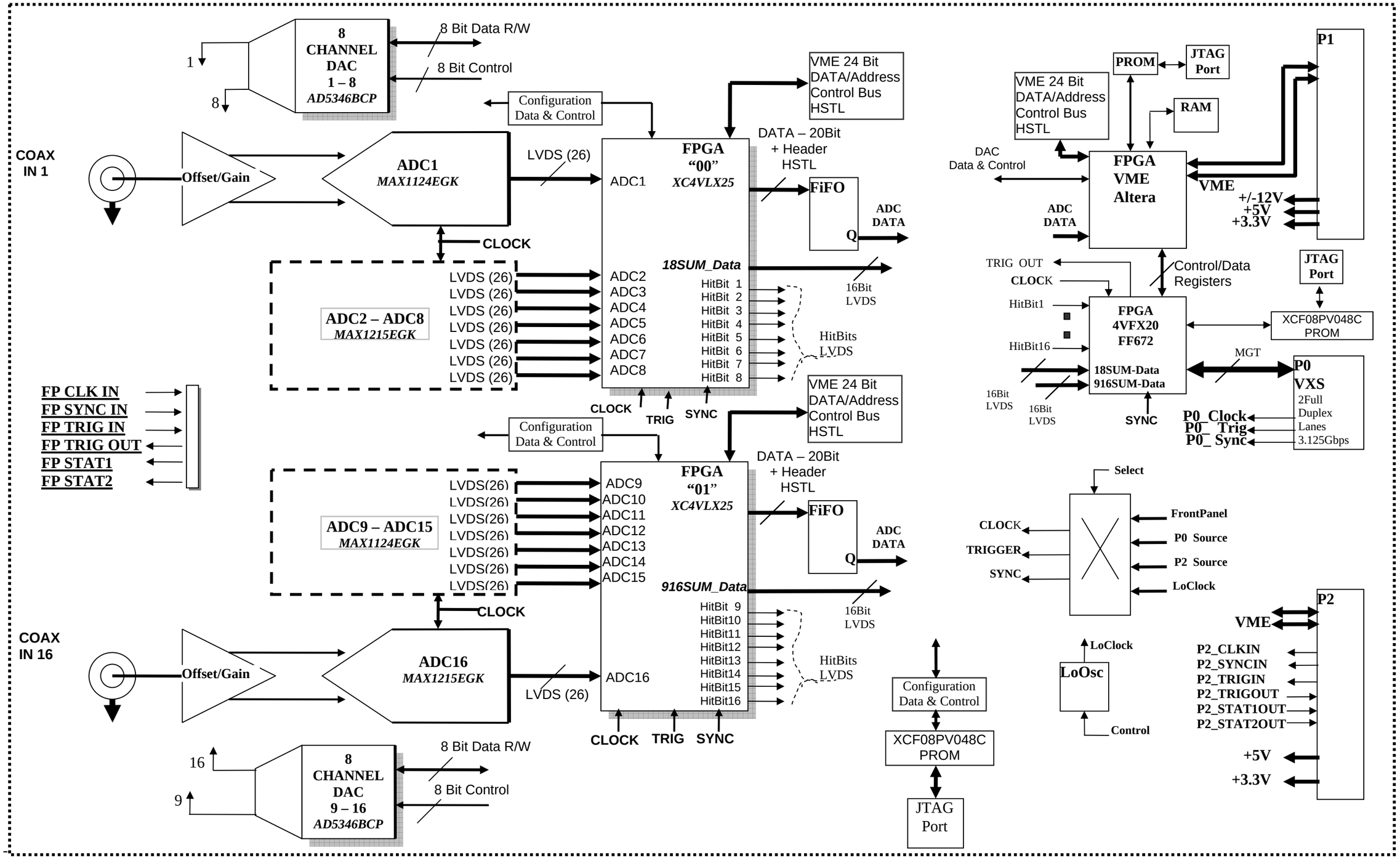
- Block Diagram

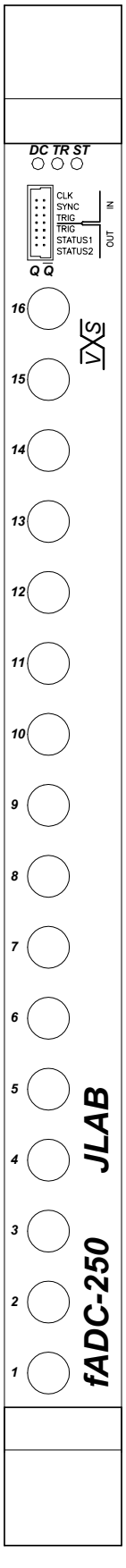
  This diagram is not intended for extreme details, but we have made several important decisions for Fpga selection and the prototype will not implement the ‘mezzanine’ idea.
- Schematic

  Schematic for the input section including sample clock distribution is complete. The sheets include the VME and VXS bus connectors.
- Printed Circuit Board

  Input section of the board is complete. Additional picture shows a ‘conceptual’ view with Fpgas placed on the board.
- Components

  XC4VFX20 parts ordered and received. These parts have all 8 MGT units operational at 3.125Gbps. 10 bit Maxim ADC parts ordered and received. All other parts are stock items.

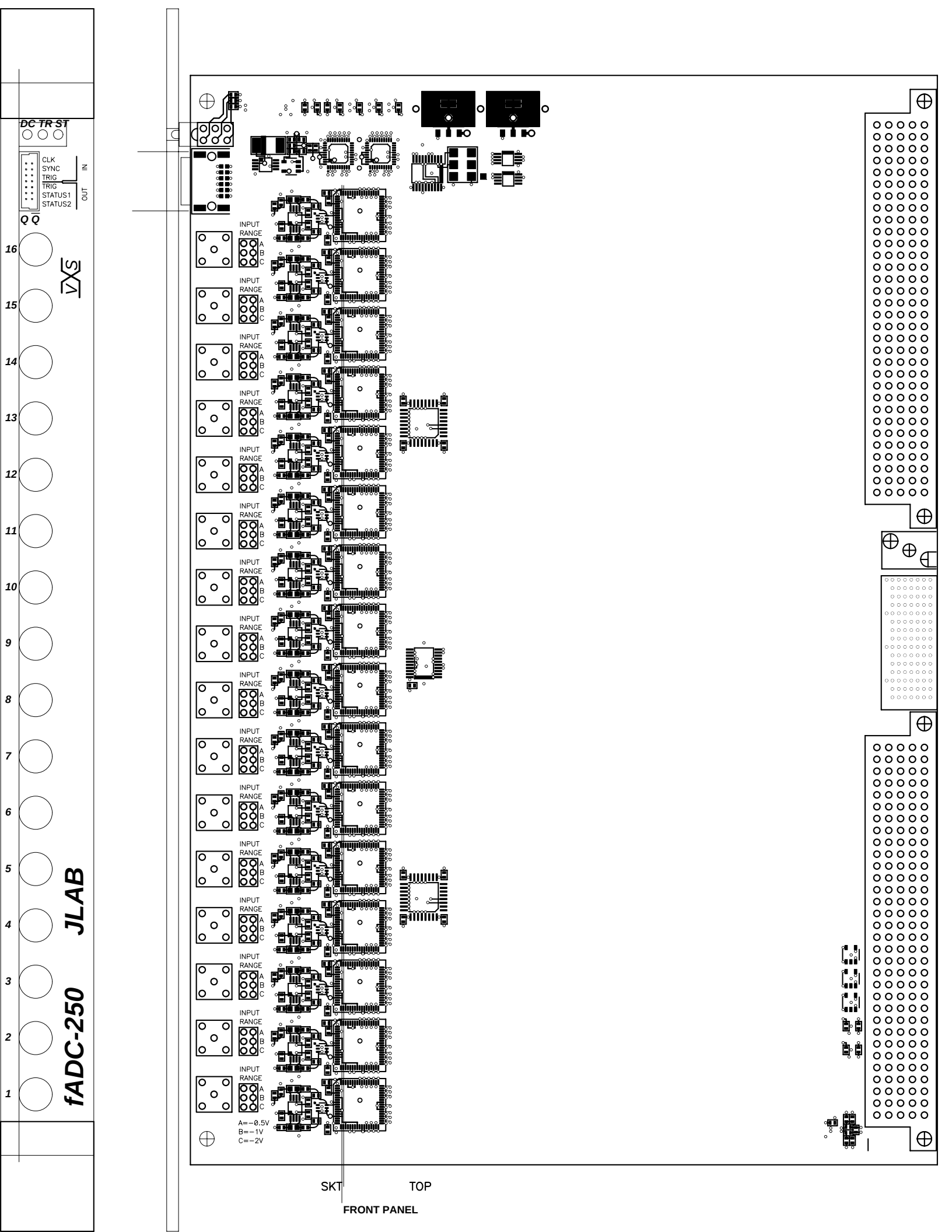

8 CHANNEL DAC 1 – 8 AD5346BCP
8 Bit Data R/W
8 Bit Control
Configuration Data & Control
VME 24 Bit DATA/Address Control Bus HSTL
COAX IN 1
Offset/Gain
ADC1 MAX1124EGK
LVDS (26)
FPGA "00" XC4VLX25
DATA – 20Bit + Header HSTL
FiFO
ADC DATA
Q
CLOCK
18SUM_Data
16Bit LVDS
ADC2 – ADC8 MAX1215EGK
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
HitBit 1
HitBit 2
HitBit 3
HitBit 4
HitBit 5
HitBit 6
HitBit 7
HitBit 8
HitBits LVDS
TRIG
SYNC
FP CLK IN
FP SYNC IN
FP TRIG IN
FP TRIG OUT
FP STAT1
FP STAT2
ADC9 – ADC15 MAX1124EGK
FPGA "01" XC4VLX25
916SUM_Data
ADC9
ADC10
ADC11
ADC12
ADC13
ADC14
ADC15
HitBit 9
HitBit10
HitBit11
HitBit12
HitBit13
HitBit14
HitBit15
HitBit16
COAX IN 16
ADC16 MAX1215EGK
ADC16
16
9
8 CHANNEL DAC 9 – 16 AD5346BCP
PROM
JTAG Port
RAM
DAC Data & Control
FPGA VME Altera
VME
+/-12V
+5V
+3.3V
P1
ADC DATA
TRIG OUT
CLOCK
Control/Data Registers
HitBit1
HitBit16
FPGA 4VFX20 FF672
18SUM-Data
916SUM-Data
16Bit LVDS
SYNC
MGT
XCF08PV048C PROM
P0
VXS
2Full
Duplex
Lanes
3.125Gbps
P0_Clock
P0_ Trig
P0_ Sync
Select
CLOCK
TRIGGER
SYNC
FrontPanel
P0 Source
P2 Source
LoClock
LoOsc
Control
P2
VME
P2_CLKIN
P2_SYNCIN
P2_TRIGIN
P2_TRIGOUT
P2_STAT1OUT
P2_STAT2OUT
+5V
+3.3V
Configuration Data & Control
XCF08PV048C PROM
JTAG Port

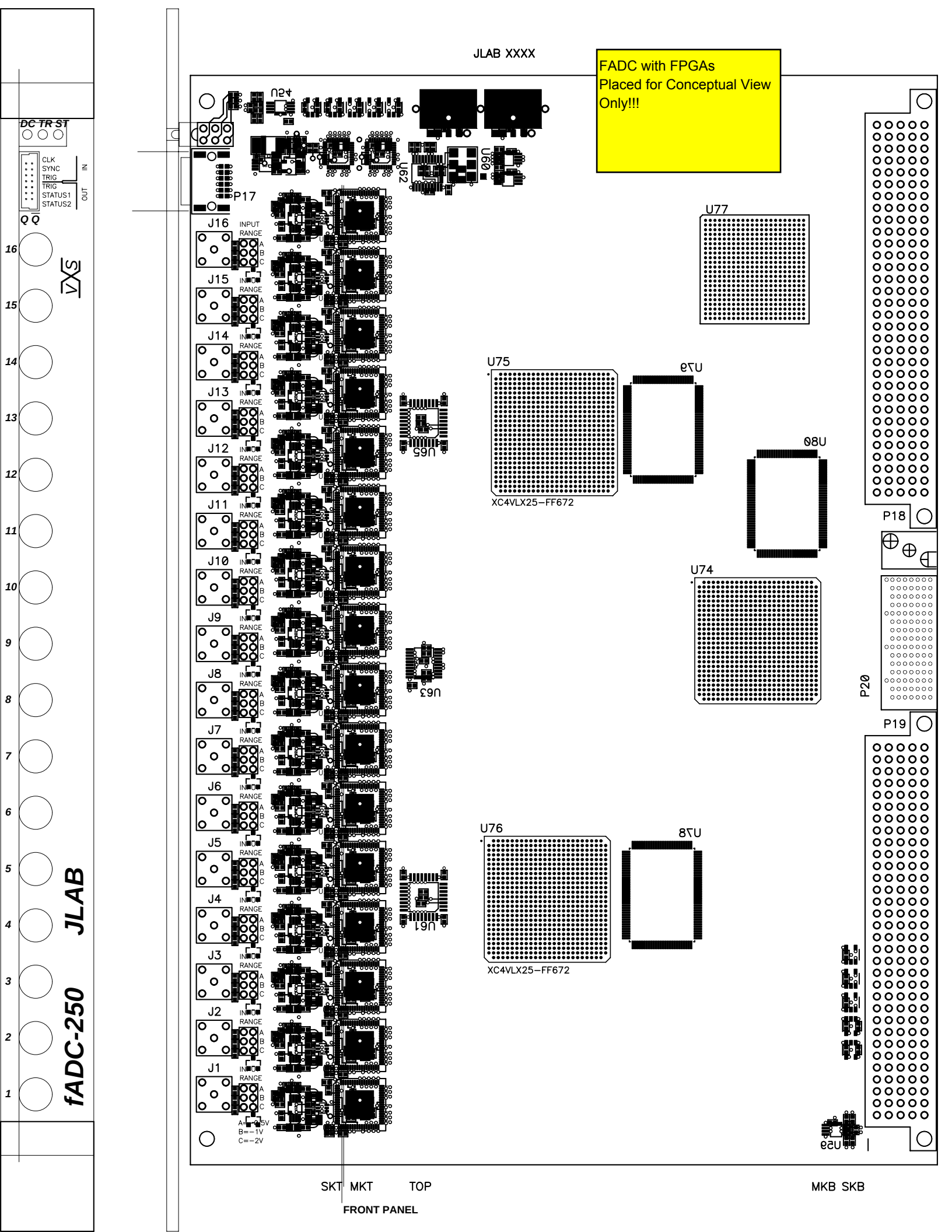


fADC250

VME64x Flash ADC Module Specifications

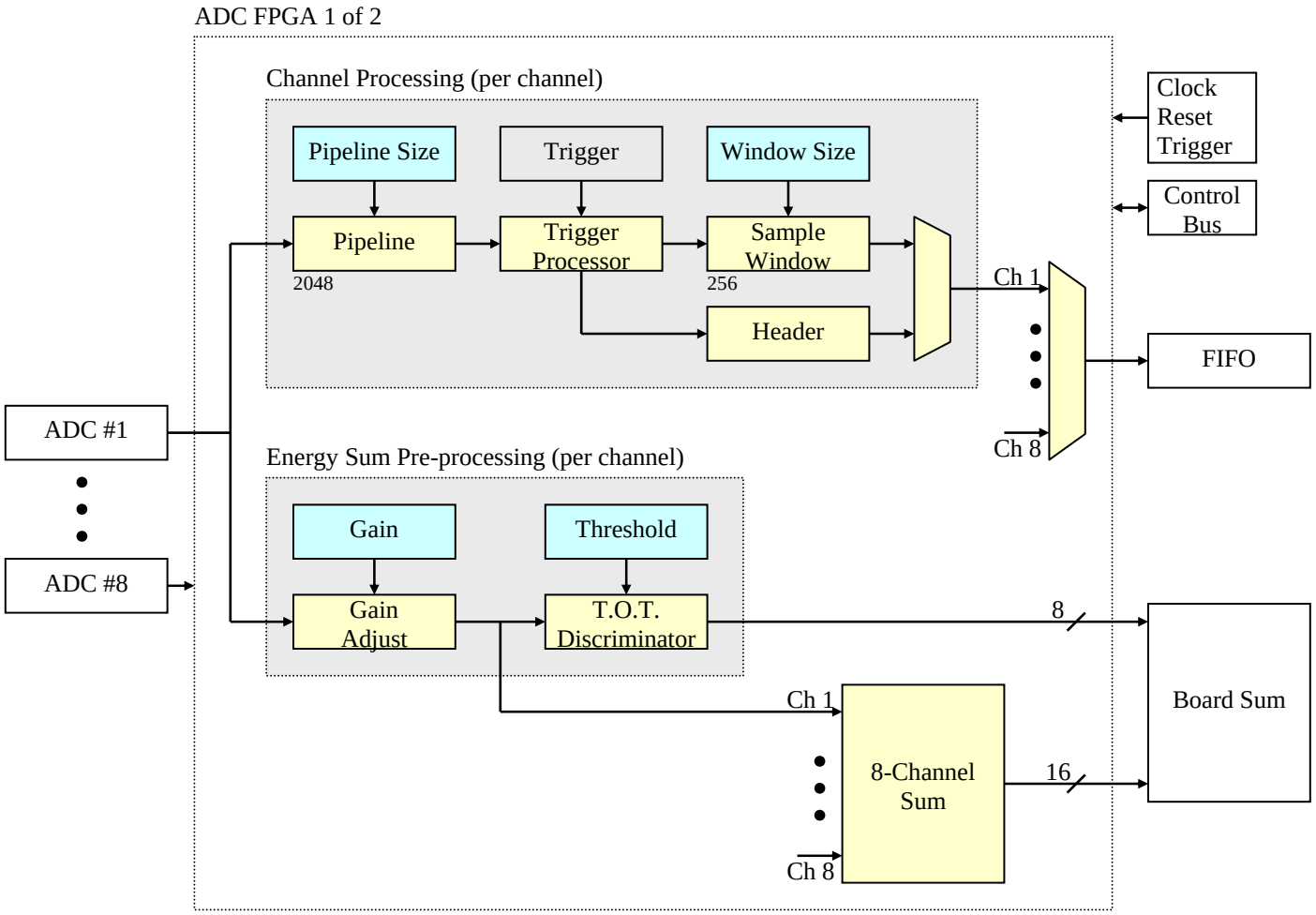
Signal Inputs	Number	16 S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable
	Offset	±10% FS per channel via DACs
Clock	Sampling	250 MSPS, Differential
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)
	Source	Internal and External
Control Inputs/Outputs	Clock	IN – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)
	INL	± 0.8 LSB
	DNL	± 0.5 LSB
	SNR	56.8 dB @ 100 MHz Input
	Data Latency	32 nS
Trigger Latency	8 μS	
Data Memory	8 μS	
Data Processing	Sparcification Windowing Charge, Pedestal, Peak Time (Over Threshold, Relative to trigger) Output (Backplane, VXS)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0	
Packaging	6U VME64x	
Power	+3.3V, +5V, +12V, -12V	


DC TR ST
CLK
SYNC
TRIG
TRIG
STATUS1
STATUS2
IN
OUT
Q Q
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
fADC-250
JLAB
VXS
INPUT RANGE
A
B
C
A=−0.5V
B=−1V
C=−2V
SKT
TOP
FRONT PANEL


JLAB XXXX
FADC with FPGAs
Placed for Conceptual View
Only!!!
DC TR ST
CLK
SYNC
TRIG
TRIG
STATUS1
STATUS2
IN
OUT
Q Q
fADC-250
JLAB
P17
J16
J15
J14
J13
J12
J11
J10
J9
J8
J7
J6
J5
J4
J3
J2
J1
INPUT RANGE
A
B
C
A=+0.5V
B=−1V
C=−2V
U24
U62
U60
U77
U75
U79
XC4VLX25−FF672
U80
U74
U76
U78
XC4VLX25−FF672
U65
U63
U61
U59
P18
P19
P20
SKT MKT TOP
FRONT PANEL
MKB SKB

FADC Preliminary Logic – Raw Data Transfer

J. Proffitt March 30, 2006



Blue : Control registers
Yellow : Processing elements
Clear : External devices

General:

- 8 ADC channels per FPGA
- Pipeline, gain adjust, discriminator, and energy sum run continuously at sample rate
- Pipeline size = 2048 samples max.
- Sample window size = 256 samples max.
- All functions operate at >250MHz

Raw Data Transfer:

- When a trigger is received, data are moved from the pipeline to the sample window (all channels simultaneously)
- After the sample window is filled, the header + window are sent to the external FIFO (all channels sequentially)
- Triggers are ignored during data transfer and if external FIFO is full
- Headers contain channel ID and trigger number

Flash ADC Status – Prototype
Discussion

- We have made several decisions at Jlab that impact the cost and development time required for the prototype.
  1. Initial idea was to use Altera Fpga with 4 ADC per chip. Alteral chip was not adequate for all of the differential input pins. The Xilinx part will manage I/O from 8 ADC and James Proffitt has simulated the initial raw data 'processing' and the results show that the logic will operate at 4nS
  2. No mezzanine – Initial idea behind the mezzanine was to push 'high level' processing functions to Fpgas on the mezzanine card. The base board would be used for applications that did not require the summing function or other requirements for data processing.
  3. Include 'trigger processing' on board using the resources on the MGT-Fpga for board level logic functions. Time-Over-Threshold 'HitBits' will be used for "local" trigger output.

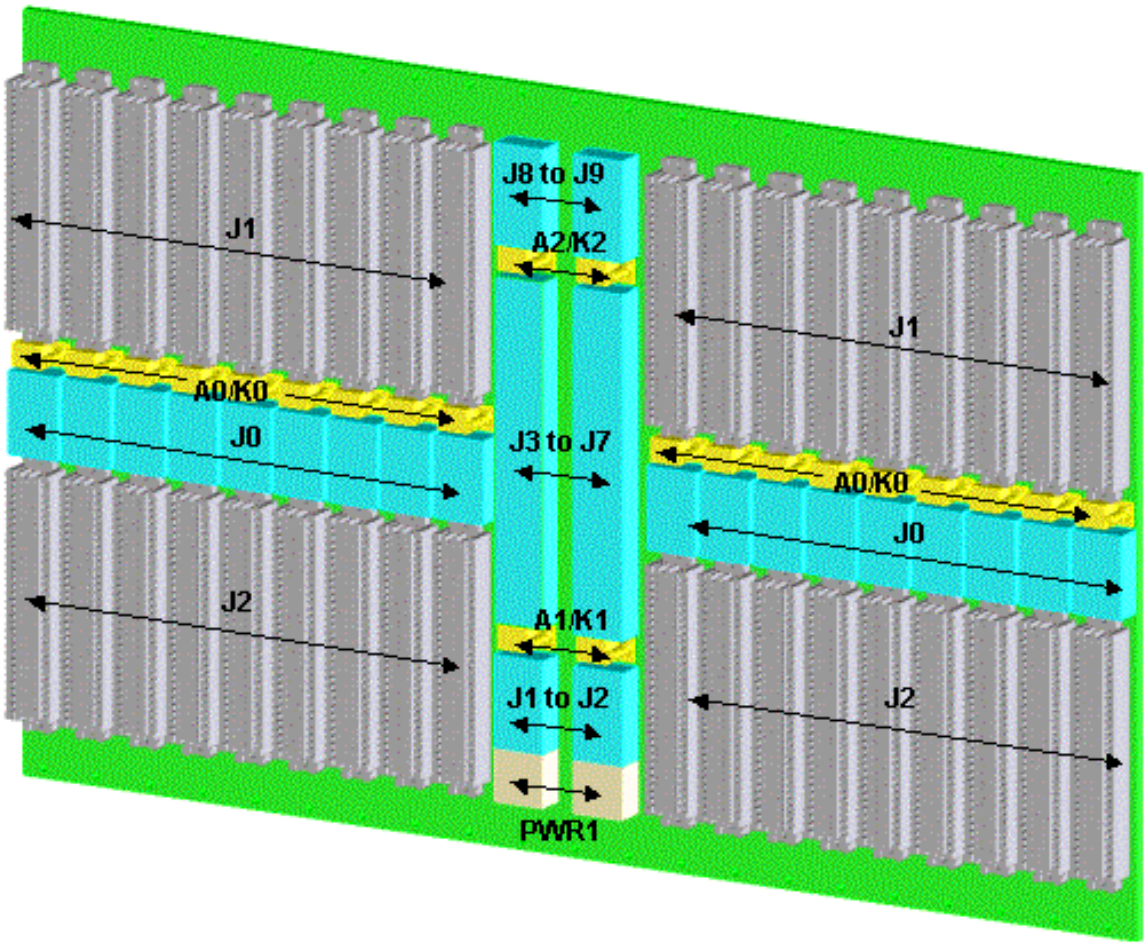
Flash ADC Status – Prototype
VXS Development

- A ‘payload’ and ‘switch’ module have been designed that are simple modules built to measure the skew from each payload slot to the center switch slot.

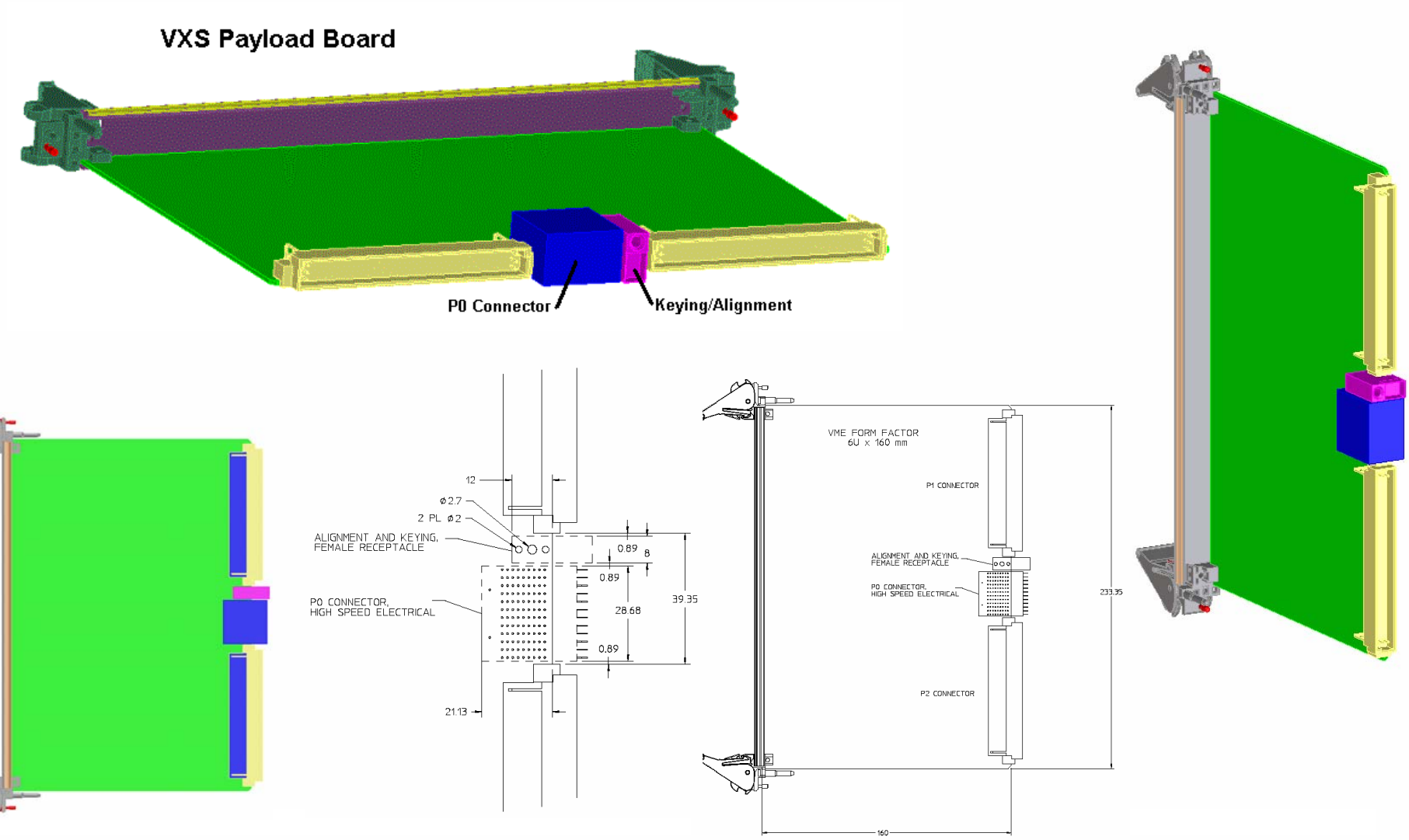
- These boards were designed to drive LVPECL signals on all of the differential pairs and single ended lines from the payload VXS connector to the switch slot VXS connector.

- We have been successful with creating the new MGT connectors and understand the connection technique used on the backplane to support all the pairs that eventually route to the central switch slot. This was by no means trivial, and the skew measurements may be very useful when testing the high speed serial data transfer from each fADC slot.

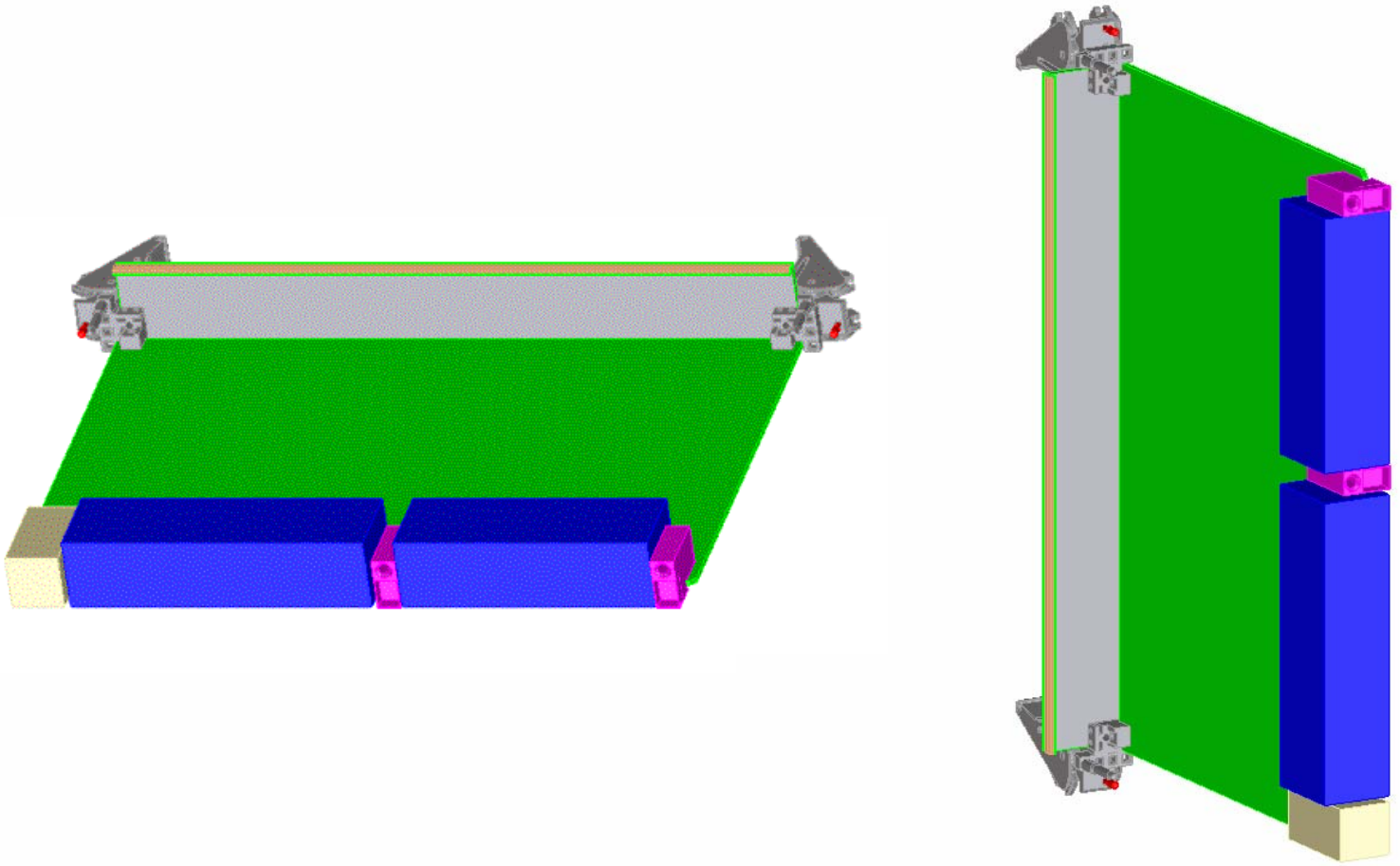
Example of a VXS Backplane

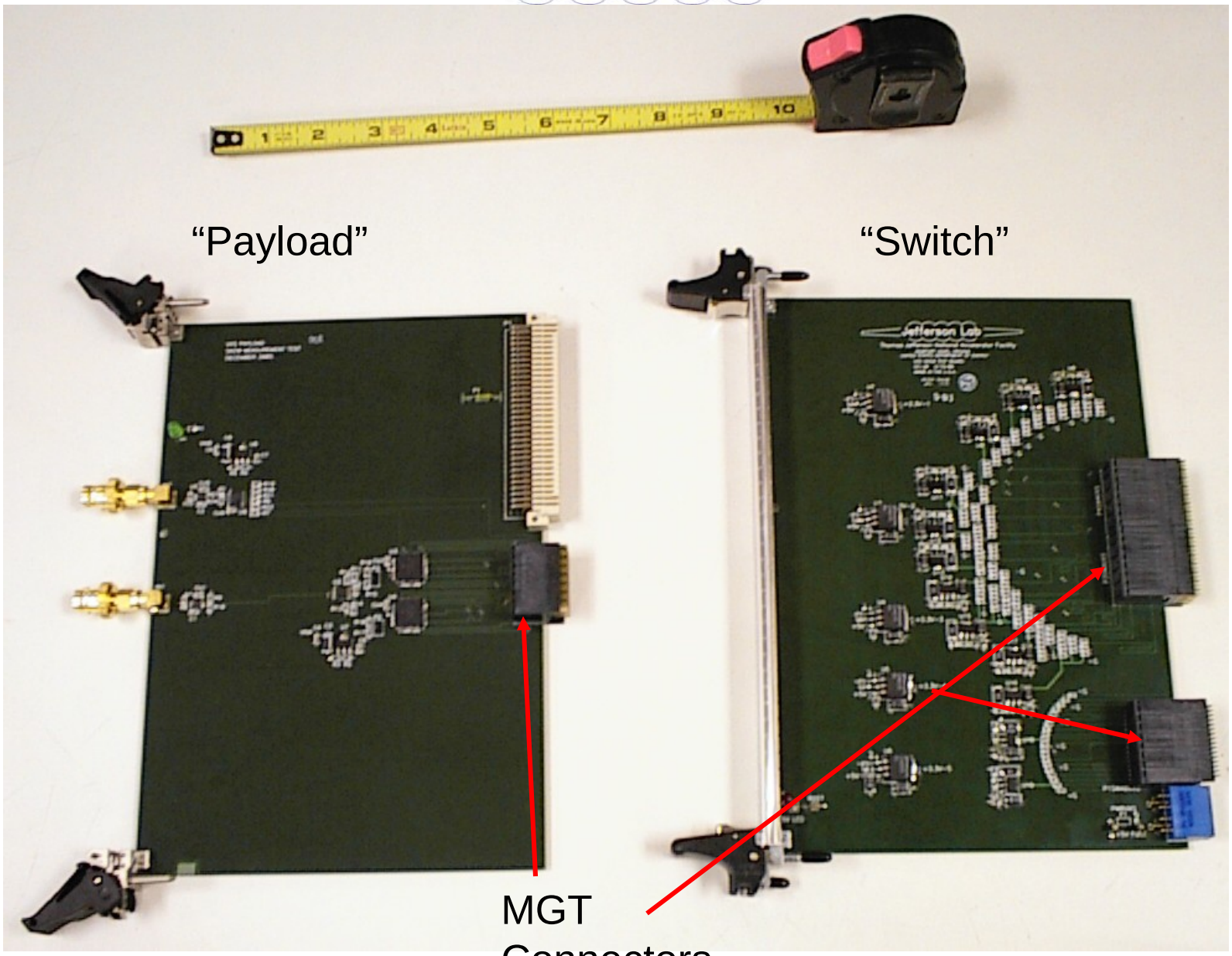


Example of a VXS Payload Board



Example of a VXS Switch Card



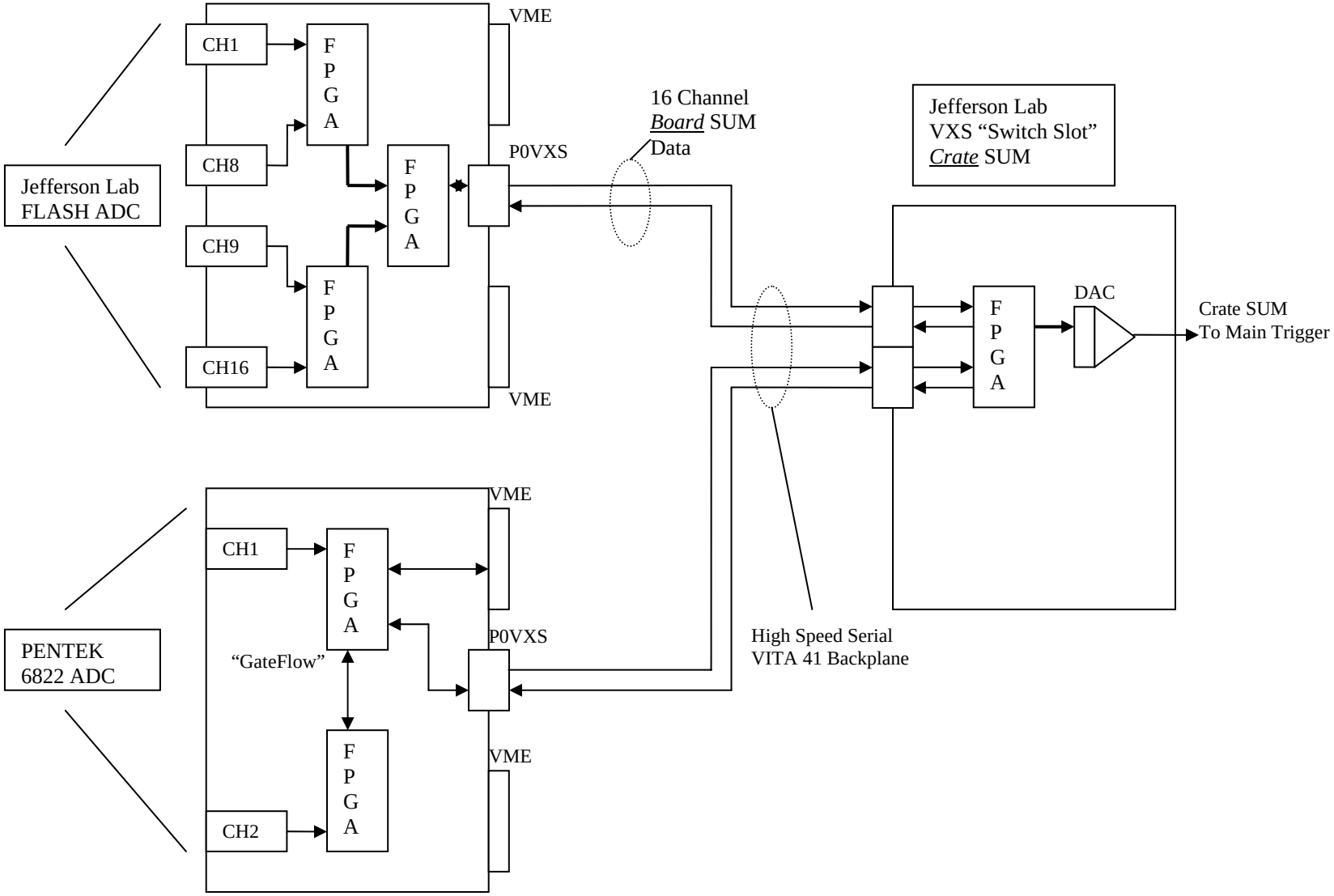

“Payload”
“Switch”
MGT
Connectors

Flash ADC Status – Prototype

VXS Development

- Additional engineering resources added to the design 'team'. These engineers are only part-time and presently work in the Accelerator Division. The engineers will focus their work on the MGT devices and provide simulation and verification of the HDL code needed for the high speed serial SUM data transfer from each fADC card to the central switch card.

- We have purchased a commercial ADC module that uses the VXS data path. This module will be used to test the switch slot prototype and can be used to simulate data from a 2nd fADC module. Block diagram on following page for discussion.


Jefferson Lab
FLASH ADC
CH1
CH8
CH9
CH16
F
P
G
A
VME
P0VXS
VME
16 Channel
Board SUM
Data
Jefferson Lab
VXS “Switch Slot”
Crate SUM
DAC
Crate SUM
To Main Trigger
PENTEK
6822 ADC
CH1
CH2
“GateFlow”
VME
P0VXS
VME
High Speed Serial
VITA 41 Backplane

FADC Module
Cost Estimate

- Cost estimate is contingent on the number of Field Programmable Gate Arrays per ADC channel
- Consider 8 ADCs per FPGA
- 16 channel design
- VME interface FPGA and peripheral logic
- Trigger Processing & VXS FPGA
- Front panel, I/O connectors, other components.
- Circuit board manufacturing, assembly, manufacturing QA

FADC Module
Cost Estimate

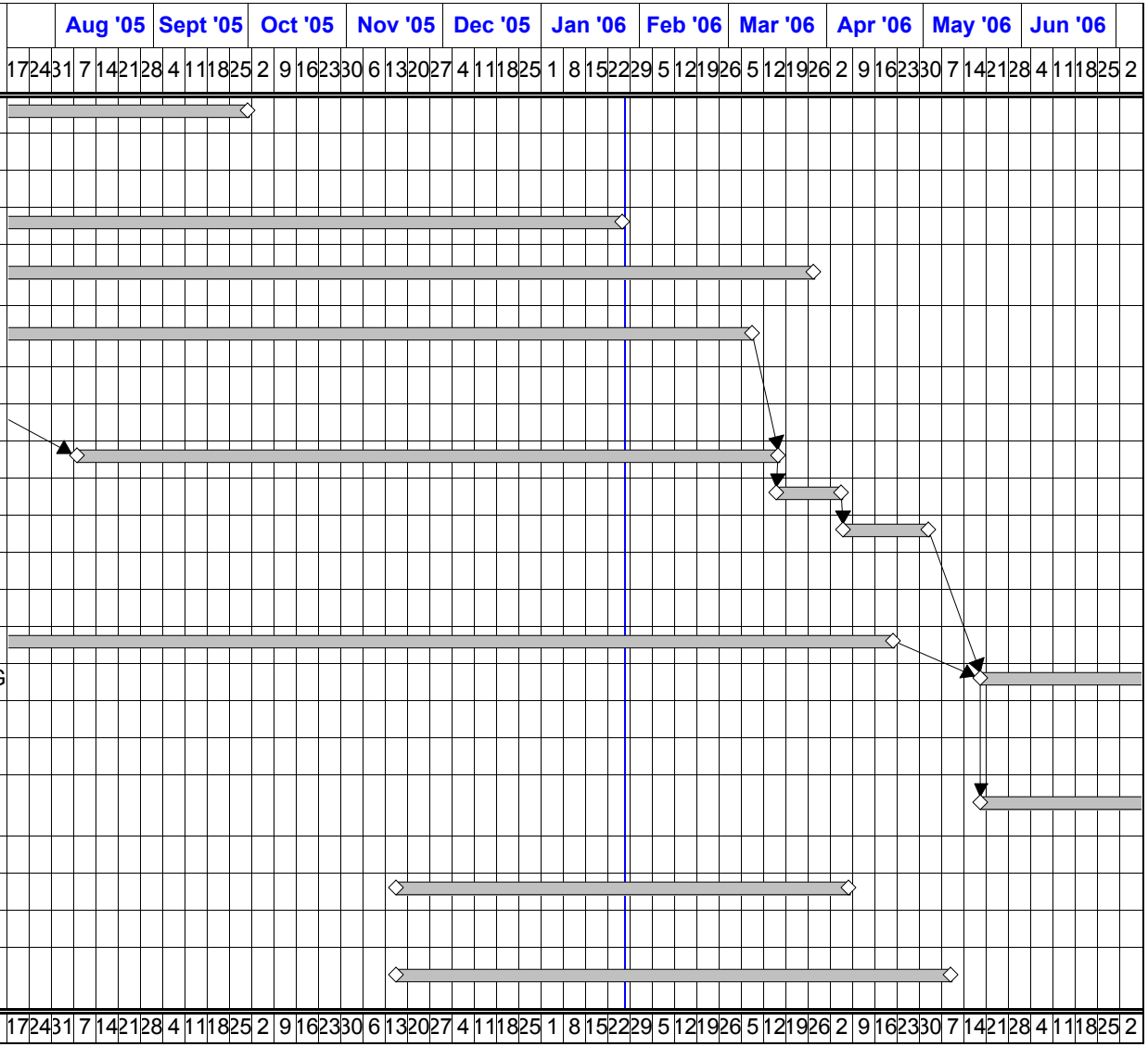
Item	Quantity	Price	Extended Price	Description
ADC	16	$50	$800	10 bit 250Mhz
FPGA-ADC	2	$300	$600	8 ADC per Fpga
FPGA-MGT	1	$235	$235	XC4VFX20
FPGA-VME	1	$250	$250	Altera
Board	1	$450	$450	Multilayer PCB
Front Panel & Connectors	**	$350	$350	MGT-VME-Lemo Engraving Etc
Assembly	1	$150	$150	Soldering-Xray- Etc
Other Misc	**		$500	FiFoS-Discreets-Etc
Total			$3335	

Jefferson Lab
THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY

Schedule

Flash ADC Schedule - Preliminary

	Activity Name	Start Date	Finish Date	Resources
1	**System Definition**	3/24/05	9/30/05	
2				
3	**Design**			
4	**Front-End**	3/24/05	1/26/06	FJB
5	**Data Processor**	3/24/05	3/27/06	JP
6	**Data & Interface Back-End**	3/23/05	3/8/06	EJ,JP
7				
8	**PCB**			
9	***PCB Layout***	8/8/05	3/16/06	FJB,JP,EJ,JW
10	***PCB Fabrication***	3/16/06	4/5/06	External
11	***Assembly***	4/6/06	5/2/06	External
12				
13	**Test**			
14	**LabView Dev.**	3/7/05	4/21/06	CC
15	***Lab Tests***	5/19/06	8/21/06	FJB,JP,EJ,MT,WG
16	***User Tests***	8/21/06	10/27/06	
17				
18	**Driver/Library Development**	5/19/06	11/16/06	DA,EJ
19				
20	**User's Manual**	11/16/05	4/7/06	CC
21				
22	**System Clock Distribution**	11/16/05	5/9/06	?????



Jan 27, 2006

C:\PCAD\Projects\Flash_ADC\FADC250-1.fts

“Roll the Credits:”

Fernando Barbosa	-- Front End Design; Project Engineer
James Proffitt	-- ADC-FPGA Data processing
Ed Jastrzembski	-- VME interface FPGA
Hai Dong*	-- Trigger Processing/MGT FPGA
Doug Curry*	-- MGT FPGA & Switch Slot Prototype
Jeff Wilson	-- Circuit board designer
Mark Taylor	-- Circuit board designer

* Part-Time from Accelerator Div.