# GlueX Electronics for DAQ

### Overview

The GlueX data acquisition electronics plan encompasses both analog and digital requirements and will, in general, be responsible for discriminating, and digitizing raw detector signals storing them for later readout at level 1 trigger rates of 200 kHz without incurring deadtime. The GlueX detector includes approximately 18,600 ADC channels and 4,300 TDC channels. This represents upwards of 70-80 front-end crates of electronics. Additional DAQ related electronics must be developed for collecting energy sums and track counts from a subset of these crates in order to process a L1 trigger decision. One then needs to distribute this trigger information at the 200 KHz rate to all of the crates.

Other electronics requirements including preamps and other detector specific needs are not covered in this document.

A pipelined approach at the front-end will be required to support the high trigger rate. The digitized charge and time information must be stored for several $\mu s$ while the level 1 trigger is formed and then distributed. Multiple events must be buffered within the digitizer modules and then readout or transmitted while the front ends continue to acquire new events. The aggregate raw data rate from the GlueX detector is expected to reach about 1 Gbyte/second. A sophisticated timing system is required to synchronize the pipelines of all front-end modules in all crates.

In parallel, formed energy sums from the calorimeter crates as well as track counts from the barrel and TOF systems must be collected and clocked back to a Master L1 trigger module (or crate) where all the data and logic that compromise the level 1 trigger can be processed.

In the following sections we describe the DAQ electronics plan. It can be generally broken down into two stages. The first stage attempts to bring together a complete set of digitizing and trigger distribution hardware to provide a platform that fully supports pipelining and event blocking. This hardware can then be used by both the existing 6 GeV program as well as R&D efforts of GlueX and the 12 GeV program. The second stage will attempt to fully integrate the Level 1 trigger processing and the a new global trigger distribution system. This stage depends on newer commercial technology (VXS and high speed serial transport) that must be developed and better understood.

### Stage One R&D

There are a number of board development projects which must progress (in parallel) over the next 3+ years both to support existing DAQ requirements and to provide R&D for the future 12 GeV program. In total, to date, eight board designs have been identified (Fig. 1) and are listed below in rough order of development: (NOTE: Boards are identified by version numbers and whether they support VME or VXS form-factors. A VME/VXS designation indicates a single board that can be used in both types of crates.)

- 250 MHz 16 Channel Flash ADC (Version 1 VME/VXS) FY06 FY07 (D,L)
- VME Trigger Interface (Version 3a VME) FY06 (T)
- Backplane Distribution Card (Version 2 VME only) FY06 (T)
- Crate Energy Sum/Trigger Process (Version 1 VXS) FY06 FY07 FY08 (L)
- F1TDC 64/32 Channel (Version 2 VME/VXS) FY07 FY08 (D)
- VXS Trigger/Clock Interface (Version 3b VXS) FY07 FY08 (T)
- Trigger Supervisor Board (Version 1 VME/VXS) FY07 FY08 FY09 (T)
- Master L1 Trigger Processor (Version 1 VME/VXS) FY08 FY09 (L)

The DAQ group is involved jointly with the JLAB electronics group in the development of all of the above designs. These boards can be roughly catagorized into three different subsystems: Digitizing(D), L1 Trigger Processing(L), and Trigger/Clock Distribution(T). However, they all must provide cross support for communication between subsystems. All experimental halls in the 12 GeV upgrade plan are expected to use modules in both the Digitizing and Trigger/Clock Distribution Systems. Therefore these boards are going to be developed without requiring the VXS backplane support.

With the design for the 250 MHz FADC currently underway, simultanious development must be done on a new VME Trigger Interface (TI Board Version 3). The current JLAB trigger interface card (Version 2) is a critical hardware component used to support many aspects of the CODA data acquisition system, specifically in the front-end, but it also provides data to the backend for event-building. It is used in both single and multi-crate systems and provides both trigger information and general I/O to the CODA readout controller (ROC) software component.

As the CODA DAQ system evolves to support higher rate experiments, pipelined front-ends, and soft real-time systems via embedded Linux (see the Gluex DAQ Plan document for more details), the capabilities of this module must evolve as well. Ideally this board becomes a bridge between support for existing and newer CODA systems. Below are outlined the general features of the version 3 trigger interface that are required.

- Software and hardware compatibility with TI version 2. Must work with the existing Trigger supervisor preferably with minimal modification of existing software.
- Include remote VME Reset capability currently provided by separate microcontroller card.
- Support trigger buffering locally. Record high resolution time stamp with each accepted trigger. Creation of a trigger event bank in RAM as events are accepted.
- VME slave must support block readout of trigger event bank information. Can be used with F1TDC and FADC in chained block reads.
- Onboard scalers available, trigger count and connected to user inputs.
- VME Master capability. For example upon receiving a trigger the card would have the ability to go on the bus and read module status or latched scaler and buffer this info in the trigger event bank.
- Clock/Trigger source for F1TDC and/or FADC - linked to time stamp. Lines to P2 for input to the backplane distribution card.
- User ability to program local FPGA. Appropriate code should be loadable over VME and then be able to downloadable into the FPGA. This code should then be selectable to be executed over the standard trigger processing code. This effectively becomes the "primary" user readout list for the crate.

The addition of updated versions of the Backplane Distribution Card and F1TDC Board will complete an initial phase of electronics development in that a consistant DAQ system that supports pipelining, and event blocking will be available. It will also be supported by the existing JLAB Trigger Distribution System (Trigger Supervisor) and be useable by all existing 6 GeV experiments. Most of the GlueX detector development DAQ can also be supported by this hardware.

Ideally this stage of development could be completed by the end of FY07.

**Stage Two R&D**

Traditional DAQ systems typically split detector signals and send one set for discrimination and L1 trigger processing, and the other set for digitization. With the availability of pipeline electronics and high speed flash ADCs one now has the ability for the digitizers to do both, requiring only a single input from the detector and consequently no delay cabling.

We plan to use a commerically supported extension to VME called VXS (VME Switched Serial) which provides a full 8 lane crossbar fabric interconnecting 18 VME payload slots in a crate with two specialized switched slots. These data lanes currently support 3 Gbit/s transfers and are expected to increase to 10 GBit/s. Using this technology we intend to design two additional switch slot crate level boards. One, the Crate Enery Sum/Trigger Processor, will collect partial sums from all FADCs in a crate and perform additional sums and trigger processing. This board would also be responsible for sending trigger data to a final Master Trigger board via a high-speed serial link fiber elsewhere in the GlueX experimental Hall. The second board would be a revision "3b" of the Trigger Interface card. The primary difference between this board and its 3a version would be that it resides in a switch slot so as not to take up a payload slot. In addition the trigger and clock signals would be distributed to all payload boards via the VXS backplane. No backplane distribution card should be necessary in this configuration.

The two final subsystems that must be developed (in parallel with the VXS crate cards) are the Master L1 Trigger Subsystem and the Trigger/Clock Distribution System (Trigger Supervisor replacement). The design of these boards

cannot be fully specified at this time. Much of their will depend on the R&D being done with VXS. The form factor necessary to collect signals from a large number of crates (around 20-30) and process that data within a few microsecs is not known. The Trigger/Clock distribution board however is expected to fit in a 6 or 9U VME form factor as it should be available for use by all experimental halls regardless if they intend to use the Master L1 trigger processor or not. There is no reason to expect to have to design two different Trigger Distribution Boards, so consideration should be given to the design to allow a compatable interface between it and the output of Master L1 Trigger board.

**Goals and Milestones**

The high speed FADC is expected to be in prototype by the summer or early fall of 2006, The new VME trigger interface (Version 3) capable of supporting both the old trigger supervisor as well as the new pipelined front-end should be prototyped in the same timeframe. This board along with the backplane distribution card must be designed to fully support and work cooperatvely with the FADC. Once these systems have been sufficiently prototyped, version two for the F1TDC can be specified and designed.

By early 2007 there should be enough hardware and software development to support small detector system prototyping, and beam tests that would encompass the core functionality of the GlueX DAQ system. By the end of FY07 we should have available a complete set of hardware to support fully pipelined high-rate systems at least at the single crate level.

VXS R&D should be sufficiently advanced by the summer of 2007 to begin protoyping the Crate Sum and the VXS Trigger Interface cards. Prototypes could be available in 2008. Final specifications and development for the Master L1 Trigger and Trigger Distribution subsystems could get underway during 2008.

**Personnel**

Personnel working on these projects include the JLAB electronics group, Ed Jastrzembski of the JLAB DAQ Group, and Dave Doughty from CNU. Currently there are three design engineers working on these projects - all part time. The JLAB DAQ and Electronics groups have additional responsibilities involving maintence and support of the running 6 GeV program. To maintain the proposed development schedule it has been determined that a 4th design engineer will be needed to sufficently cover the overlaping requirements of all these designs. In addition, as prototyping moves to production, more help will be needed in the form of an electrical tech who will be able to support testing, debuging and repair. Support for all these designs will be ongoing as they are built and put into production. It is important that the proper expertise in these various new technologies be maintained in house, and that it stay.

Software support for these boards must also be developed as these designs are built. This effort falls under the responsibility of the DAQ group. This code must be integrated with the general CODA software toolkit.

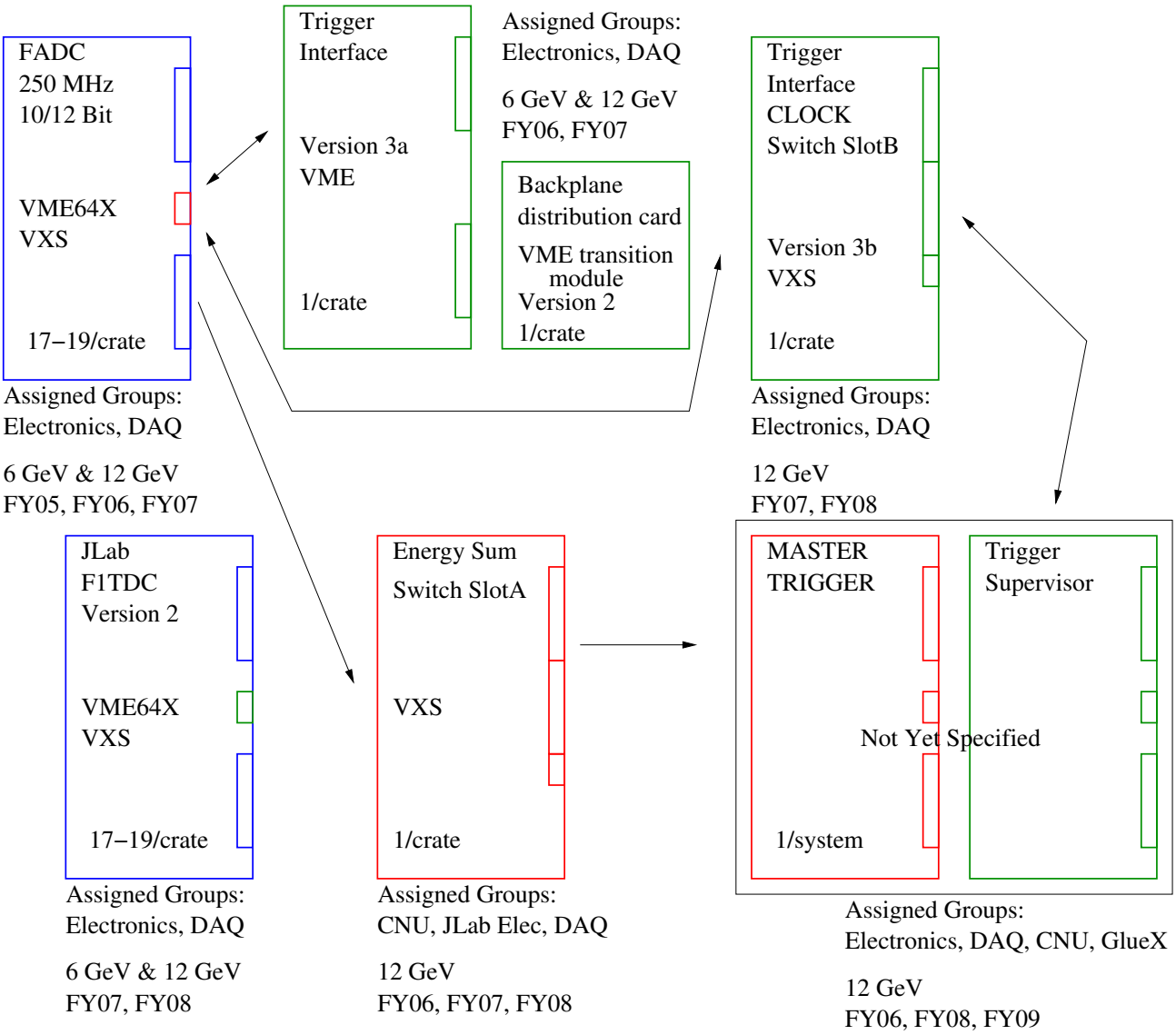


Figure 1: Schematic of the electronic boards that are required to support the plans for GlueX pipeline electronics and data acquisition. Indicated are the module classifications, responsible groups, expected use in the 6 or 12GeV program, and estimate of time frame for design and prototyping.