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P. Smith, scribe

Minutes of GlueX electronics meeting in Bloomington, Indiana; April 6 & 7, 2006

Participants:

At IU: Dave Rust, Mike McCracken, Simon Taylor, Paul Smith, Jim Pinfold, Scott Teige, Curtis Meyer, Matt Shepherd, Alex Dzierba, Chris Cuevas, Ryan Mitchell, Eric Scott, Gerard Visser

Videoconferenced from JLab: David Lawrence, Elliott Wolin, Ed Jastrzembski, Elton Smith, Dave Abbott, Dave Doughty

Videoconferenced from UConn: Richard Jones Videoconfereced from UPenn: Mitch Newcomer

By phone from UTenn: Steve Berridge By phone from Alberta: George Lolos, Zisis Papandreou, Mauricio Barbi

April 6:

Paul Smith gave a brief introduction and welcome. Slides are on the GlueX portal as doc-605. There was a discussion of the need to "re-baseline" the detector design in order to include the latest channel counts and to substitute the DIRC for the gas cerenkov currently in the design. Elton pointed out that there was an imposed requirement to stay within a fixed cost envelope. One ongoing problem is delays in procurement; the Struck fADCs needed for drift chamber testing have not yet been ordered for example.

Chris Cuevas reported on the status of various modules being developed at JLab. Slides are on the portal as doc-603. Chris has also written a planning summary of his group's efforts for migrating the existing 6 GeV experiments and the 12 GeV program to the new electronics modules; this is available as doc-614. A big motivation for current work by the JLab fast electronics group is to replace aging FASTBUS modules in the existing halls as well as providing new modules for hall D. For the 250 Msps FADC project, a first prototype should be available in the summer of 2006. Xilinx and Maxim parts are in hand. The prototype will copy 1 μs time windows from the 8 μs pipeline into up to 8 processing units; this has been simulated and uses about 40% of the front-end FPGA resources. The prototype will not implement a leading-edge time-fitting algorithm. Two engineers from the accelerator division have been helping with the VHDL design and modeling of the high-speed serial VXS links that will carry the GlueX calorimeter energy sum trigger information. These links can also be used to form other types of triggering functions for the other halls. Two test boards have been constructed to measure timing delays and skews on a VXS backplane. A Pentek flash ADC which includes a Xilinx V2pro chip has also been purchased in order to begin exercising VXS backplanes. All work to date has been funding with "6 GeV" money. Requests for "12 GeV" funding have been submitted, but not yet approved.

Dave Doughty reported on the status of the energy sum trigger high-speed serial links. Slides are in GlueX-doc-608. The JLab FADC board will include a Xilinx XC4VFX20 which has 8 multi-gigabit transceivers; these will connect to the 8 VXS backplane signal pairs. The GlueX calorimeter energy sum is expected to use 4 bonded lanes. The Xilinx Aurora protocol has been selected due to it's low latency and low overhead. An "Active VHDL" simulation is working. Two evaluation boards have been requested which would allow further development and testing. A forward error correction algorithm needs to be developed, and there are details of framing and synchronization to be worked out.

Scott Teige showed results of a simulation of an algorithm for extracting timing information from a fit to the leading edge of pulses from the FCAL PMTs. Scott's slides are in doc-607; the algorithm is further described in doc-426, while a note about the FCAL timing is in doc-427. The algorithm uses all integer math, achieves a resolution of 1/25 of the time bin size, and could be implemented in either a single 24 bit lookup, or a series of three 16 bit lookups. Further studies are needed to evaluate how well this algorithm works for small pulse heights. It is not clear at this time where best to implement this time fit; it could be part of the FADC, the crate level CPU, the level 3 processor farm, or part of the event analysis. It may be desirable to use this or a similar algorithm to reduce the TDC channel count for the BCAL. It should also be applicable to the Pair Spectrometer and the Upstream Photon Veto.

Mike McCracken presented an update on the CDC status. He has redesigned the HV distribution board due to several problems with the first version. This is being fabricated from RO-4003 material to eliminate outgassing since it is inside the gas plenum. He has some JLab transimpedance amplifiers to try as well as a HV distribution and preamp board from CLEO. Slides from this talk are on the portal as doc-604.

Simon Taylor showed his latest results from the FDC prototype. See GlueX-doc-602 for slides. He can image the anode wires using the cathode strips with about 200 μm resolution. He has tried several algorithms for fitting the cathode pulse leading edge to extract a time; his best result so far is about 4.2 ns with a 105 Msps Struck fADC. The Struck full scale range has been reduced from the original 5 volts, but more gain would be useful. Simon also needs to try extracting timing from the anode signals.

Jim Pinfold gave an update on the chamber preamp project (GlueX-doc-609). There is a 3 stage plan covering 2 years. UPenn has an 8 phase plan for designing the chips based on the existing ATLAS ASD. For GlueX, the chips will likely be made in a 0.25 μm TSMC CMOS process by MOSIS. For phase I, 40 chips will be fabricated and placed on 16 channel boards (probably two 8 channel chips). These boards should be available for chamber and bench tests in the fall of 2006. Phase II (testing) should be done by late 2006 or early 2007. For phase III, 500 chips will be fabricated and about 1000 chamber channels instrumented. The time scale for phase III is expected to be around fall of 2007.

Mitch Newcomer joined the meeting by video link. He will be sending 2 ASDQ boards for us to try on the prototype chambers. He expects to be ready to submit a design to MOSIS for fabrication by September of 2006. There are several specifications he needs from GlueX:

1) Input protection needs?
2) maximum chamber current
3) maximum drift time
4) output current requirements

He would also like to see a "gallery" of typical signals from the prototype chambers. There was some discussion of exactly when the U Alberta preamp development contract would be in place since his students can't get started before then. This contract must be signed by Allison Lung at JLab – the hope is this contract will be in place by the end of April.

Gerard Visser described his planned adaptor which will interface the existing and planned preamps to a Struck flash ADC - basically it is a differential-to-single ended convertor. There will be 2 op-amps per channel available for prototyping and testing various shaping options. Once we are confident that we understand the required sampling rate, Gerard will begin work on a prototype chamber ADC board. This will likely be a 64 channel board sampling at 100 to 125 Msps. Gerard showed a preliminary layout and a summary of currently available multi-channel chips. The plan is to use round cables with 20 twisted pairs to connect the preamps to the ADC board. Each cable would service 16 detector channels leaving 8 wires to supply preamp power as well as any control or test signals. Clocking and other control lines would be through the VME P2 connector allowing 20 of these modules in a VME64X crate.

There was a general discussion of GlueX tracking. There are currently no plans to test either the CDC or FDC in a magnetic field. There is a plan to have a beam test of at least the FDC at TRIUMF in 2007.

There is also the issue of testing the dE/dX capability of the chambers. Curtis thought that the large range of angles which tracks pass through the CDC is a much larger effect than dE/dX; the plan is to test the prototype with cosmic rays and to have the ability to rotate the chamber to various angles.

We also began a discussion of manpower issues. There are currently 3 engineers working on various GlueX electronics projects at JLab, but all have other responsibilities as well. At least one additional engineer and one senior level technician are needed at JLab to work on the flash ADC as well as various trigger cards, distribution cards, a new trigger supervisor, etc. This is spelled out in GlueX-doc-614. It was the conclusion of the meeting participants that at least one full time person is needed at the lab to work on "slow control" issues, i.e. temperature monitors, power supply monitors, etc. There should be an effort to standardize this type of electronics on a lab-wide basis. In addition, there should be an engineer dedicated to the mechanical/electronic integration of the GlueX detector. For example, where do the FDC preamps sit inside the magnet, how are they cooled, how do the cables exit, etc. GlueX cabling in general has not been well thought out, and the design report specifies the ability to operate the various subdetectors in an extracted position without uncabling. The routing, support, and management of the detector cables needs a complete and detailed design which allows for subdetector movement.

April 7:

The manpower discussion was continued from the previous day. The consensus was that 4 full time people are needed at JLab. These are:

1) Fast electronics/DAQ engineer
2) One senior technician

These two positions are requested in GlueX-doc-614

3) One mechanical engineer to work on cabling, cooling, and general detector integration issues.

4) One lab-wide slow controls coordinator/integrator

It was thought that currently there is adequate technical manpower at the various universities working on GlueX electronics. Alberta has 2 engineers available to work on preamp integration. UPenn has Mitch Newcomer who is supervising the preamp chip design. UTenn has one engineer working on DIRC electronics. The BCal SiPM electronics will be purchased as an integrated system. FIU has responsibility for calibration and test pulsers. For the FCal, Indiana will need a technician to work on testing the Cockcroft-Walton PMT bases, although it is likely that SiPMs will be a reasonable alternative. It was agreed that Elton Smith, Chris Cuevas, and Paul Smith will continue to work on spelling out a complete list of all GlueX electronics and the manpower needs. A good start on this is GlueX-doc-614. An updated version of GlueX-doc-524 will be available soon and will include manpower information. Alex pointed out that JLab contracts with universities and IUCF should be written as long term agreements in such a way as to be independent of specific engineers, allowing for personnel changes while still maintaining institutional responsibilities. Standardizing electronics amongst the various JLab experiments is also important from the standpoint of maximizing the use of limited engineering manpower.

Steve Berridge phoned in from UTenn and gave a nice presentation on work there related to the DIRC. They are examining uniformity issues for the proposed multi-anode PMT, the Hamamatsu H-8500 and are looking at a preamp from the BABAR DIRC on loan from SLAC. The op-amps used at SLAC are no longer available, so this will need to be redesigned. Chris Cuevas mentioned a similar board being used at JLab and will loan a copy to UTenn. Steve's slides are on the GlueX portal as doc-616.

Richard Jones joined the meeting by video and gave an update on the Tagger, Pair Spectrometer, and Pair Polarimeter. His slides are in GlueX-doc-615. The tagger "microscope" will be read out by silicon PMs. If currently available SiPMs are used it will be necessary to construct stabilized, regulated, adjustable power supplies of about 48 volts; this would be designed and built at UConn. The SensL SiPMs will

likely be complete “modules” which include this power supply. The tagger “fixed” array will use conventional 1 inch PMTs and commercial bases. Catholic U is responsible for this part of the tagger. It may be possible to use current integrating ADCs to save money over flash ADCs, but this increases the number of module types and should be carefully considered. The tagger “OR” will be formed with commercial NIM logic with the result being sent via fiber optic cable to the GlueX trigger. Other fibers will carry the clocking and trigger signals upstream to the separate tagger building. Scalers will also be needed on the tagger channels.

Richard also mentioned two other detectors. The Pair Spectrometer is in the current baseline detector and consists of 32 channels of scintillator paddles viewed by conventional PMTs and read by flash ADCs. The silicon microstrip based Pair Polarimeter is not in the current baseline design. This is in some sense a separate experiment; the rates are low, the time resolution needed is only 10 ns, and the readout can be done with buffered latches. A similar detector system currently exists in hall B.

Mauricio Barbi, George Lolos, and Zisis Papandreou phoned in from Regina with an update on the silicon photomultiplier R&D being done by SensL in Ireland. They expect to have 1 mm^2 SiPMs available soon with a dark rate of ~200 Hz/pixel, a rise-time of 1-2 ns, and a fall time of 20-40 ns. The “phase 1” SiPMs for the BCal should be ready for acceptance testing this summer. These will have an active area of 1.3 cm^2, 10^4 pixels, and a variable gain amplifier. There is still a lot of uncertainty in the BCal channel count. Current estimates are about 2000 FADC channels and 1000 TDC channels. Simulations are in progress to optimize these numbers. Slides are in GlueX-doc-617.

Scott Teige spoke about the electronics implications of upcoming beam tests of detector prototypes at JLab. The BCal test in the fall of 2006 will use conventional FASTBUS ADCs and TDCs and read the hall B tagger with the existing FASTBUS TDC readout system. For the summer of 2007 FCal tests, the detector itself is fairly well understood from previous runs at BNL and JLab, so the main thrust of the running will be to use “real” GlueX electronics including F1 TDC readout of the hall B tagger, FADC readout of the FCAL, and an energy sum trigger using the FADC data. There will be 2 VME/VXS crates with a prototype clock distribution system and the new JLab trigger interface and supervisor modules. We also want to test the derivation of ADC and TDC clocks from the accelerator master oscillator. Scott’s slides are in doc-606.

There was a lively discussion of what needs to happen at JLab to be ready for the summer 2007 test run. The main issues are finishing the FADC design and testing of the prototypes, the implementation of the energy sum trigger, clock distribution, and the new trigger interface card. Additional manpower is needed essentially now if we are to make this deadline.

Elton Smith showed a nice slide (GlueX-doc-611) of livetime vs processing time and buffering, and there was considerable discussion of what is meant by a deadtimeless front end electronics system in GlueX. The F1 TDC, for example, has 4 trigger buffers so that multiple triggers in a short time window can be handled. A counter increments on each trigger. The processing time varies depending on the number of edges in the time window being considered. If the short term rate is too high triggers may be lost, but the count will still be correct. The JLab FADC prototype will not implement multiple buffers, but this is planned for subsequent versions with enough FPGA resources being allocated. The philosophy for GlueX front-end electronics is to handle variations in trigger rate with buffering; if all buffers get used up a flag will be set indicating a trigger was received but no data can be provided. For the expected maximum level 1 trigger rate of 200 kHz and sub-microsecond processing times, the live time will be essentially 100%.

Dave Rust attended this electronics meeting as an observer and his comments are available in GlueX-doc-618.