High Density 125 MSPS Differential Input ADC Module Specifications – for GlueX Drift Chamber Application

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This document sets forth the specifications required of the GlueX drift chamber ADC board to be designed and constructed by IUCF.

Requirements

The following specifications are required. Every effort shall be made to have the prototype meet or exceed these specifications. Deficiencies shall be addressed in a revision of the design. Workarounds shall be implemented if feasible, to allow for FDC and CDC prototype activities. These specifications will be tested thoroughly before the prototype moves into production.

Signal inputs	Number of channels	72
	Connector type	3M #10250-1210PE "Mini-D-Ribbon", for use with 25 pair double density cable
	Channels per connector	24
	Signal range full scale	+/- 164 mV differential @ 100 kHz. Gain may be altered with choice of resistor values.
	Programmable signal range	No – set by choice of resistor values
	Programmable DC offset	+/- 55% of full scale range, common DAC setting for groups of 12 channels, >12 bit resolution
	Termination	100 Ω differential, high-Z common mode
	Common mode rejection	>66 dB @ 0 to 10 MHz over specified range
	Common mode range	-1.75 V to 4.25 V
	Frequency response	Includes cable equalization and 5^{th} order lowpass shaping/anti-alias filter; *response details to be optimized in studies with real cable & preamp*
Conversion characteristics	Bit resolution	12 bit
	Sample clock rate	10 to 125 MHz; tolerant of higher clock input frequency but functionality not guaranteed

	Sample clock source, ext	Differential input >200 mV @ >5 V/ns differential slew rate, 3.3V CML common mode range; see “Fast control inputs/outputs” for connection details.
	Sample clock source, int	Fixed 125 MHz +/- 50 ppm oscillator, <1 ps RMS jitter over 10 kHz to 20 MHz offset from carrier
	Sample clock distribution tree additive jitter, ext input to effective sampling apertures	<50 ps RMS jitter over 10 kHz to 20 MHz offset from carrier, measured with FS 10 MHz sinewave on one channel, FS white noise on all other channels, random readout triggers at max rate, >50% VME bus activity with MBLT
	INL	<0.1%, measured with 1 kHz ramp
	DNL	<1 ADC bin, measured with 10 MHz sinewave
	SNR	>67 dB with 10 MHz FS sinewave on one channel, FS white noise on all other channels, random readout triggers at max rate, >50% VME bus activity with MBLT
Preamp test pulser	Number of channels	3
	Output interface	Current-mode drive onto 25th pair of signal cable
	Signal range full scale	+/- 10 mA differential
	Waveform	TBD – step, pseudo-log, or arbitrary/DAC
	Timing/triggering	TBD – Through fast control input (a trigger/command word format must be defined to support this).
	Rate	<1 kHz
Fast control inputs/outputs	External sample clock input	Differential CML or LVPECL input from P2 or VXS P0 (selectable)
	Trigger/command input	3 bits, differential CML or LVPECL or LVDS, input from P2 or VXS P0 (selectable, follows ext sample clock), synchronous to P2 sample clock. Low-rate asynchronous trigger option is selected if internal clock is used, has trigger jitter +/-2 sample periods.

	Trigger/command word format	Serial word presented in “nibbles” of up to 3 bits, length TBD, possibly only 1 bit per existing JLab standards.
	Trigger/command bit setup/hold time requirement	1 ns / 1 ns
	Sync input	This is just a special case of trigger/command
	Spare input	If used, this is just a special case of trigger/command
	Busy output	P2, active low open-collector output, maskable. Also P0, LVDS output, maskable.
System timing and rates	Trigger latency (max allowable)	13.5 μs
	Variable (event-event) trigger latency	Allowed, if trigger/command word format is defined to support this. If not, trigger latency is a programmable constant.
	Trigger input deadtime	Fixed value, depends of course on format / word length of trigger/command input. With standard “1 bit” trigger/command word, deadtime is 2 cycles (16 ns @ max sample rate).
	Trigger action FIFO depth	>8
	Busy assertion	On programmable almost-full condition of trigger action FIFO
	Trigger (readout) handling time	Depends on programmed data window size; example ~ 375 ns for 40 point window
	Action on attempted readout too late (acquisition overrun)	Skip whole event data but insert error flag into datastream instead
	Action in case of back-end data FIFO almost full condition	Next readout suspended until the almost full is relieved (in consequence of back-end readout). This may cause “late readout” errors (event skips) if trigger rate is high. Optionally, data FIFO almost full may assert busy output, to prevent this.
	Final output data FIFO size	1 MB

On-board data processing	Zero suppression	Starting from fetch window (start: defined by trigger time and trigger latency value, length: a programmable constant), programmable lookahead (0-31 points) of programmable ZS threshold crossing defines start of sample window; channels never crossing ZS threshold during fetch window are completely suppressed from datastream.
	Window extension ("reverse zero suppression")	Optionally, sample window can be extended if signal continues above some other programmable threshold at "nominal" end of fetch window. (Would allow nominal window to be set narrower).
	DSP	FPGA-based DSP can be performed on the sample window (zero suppressed) data, or the sample data can be read out raw.
	Examples of supportable DSP	Integration; peak finding, edge timing, or time over threshold @ raw sample resolution; short FIR filtering; interpolation/upsampling and peak finding or edge timing @ upsampled resolution; correlation/matched filtering; …
	Header insertion	Each channel not suppressed gets at least a sample window start timestamp, sample length count (if raw samples are output), and channel number (and optional module number) inserted. Each event gets some header words including trigger scaler, trigger time, error flags, and optionally checksum words (trailer words if desired).
	Hit limit	Entire event data dropped if a programmable hit count limit is exceeded. Error flag word inserted into datastream instead.
Datastream readout	Interface	VME64x 2eSST, also supports 2eVME, MBLT, BLT32, A32:D32 single accesses. Up to ~320 MB/s for 2eSST (in practice, expect about 160 MB/s).
	Interface – addressing	Main output data FIFO multiply mapped to 1 MB, to allow for block transfers. But it is a FIFO – random access is not supported, you always get the next word.
	Protocol	Read a register to get number of bytes in some preset number of events, e.g., 200. Then read that many bytes from output FIFO.

	CBLT	Supported, details TBD.
	Event size	Padded to a multiple of 4 bytes if needed.
	Block transfer padding	Last word to transfer is padded up to 8 or 16 bytes if needed, according to transfer type.
Scalers	Level crossing scalers	Each channel has 3 (TBD) programmable level crossing scalers
	Scaler capture	Simultaneous capture of all the scalers to readout registers, triggered by TBD (here again, would like more than a 1-bit trigger command)
	Scaler readout	Can be inserted into datastream (preferred) or read individually by VME
Infrastructure	Mechanical	6U VME64x compliant, constructed as a main board including 36 ADC channels and a mezzanine board with 36 more channels
	Power	<75 W; +5 V @ <13.5 A, +3.3 V @ <15 A, +12 V @ <1.5 A, -12 V @ <1.5 A, i.e., within ratings of Wiener 6021/23 VME64x crate at connector ambient temperature <50 °C. ***Full crate will require 230 A supply option on +5 V.***
	Thermal	Forced air cooling is required. ***May require bottom airflow fan tray.*** Overtemperature shutdown will be implemented if needed to prevent damage in case of airflow failure. It will not be implemented to maintain calibration in case of airflow failure.
	Housekeeping monitors	Board temperature(s) will be readable via VME. Supply currents or regulator control voltages, if available, will be readable via VME.
	FPGA Clear & Configure	Shall occur on power-up or assertion of VME SYSRESET#
	FPGA Configuration Memory Update	Downloadable through VME with no physical access (jumpers, switches, JTAG cables) required. JTAG download also supported for debugging & initial boot.

Other expected characteristics

The following are either anticipated improvements of performance stated above, loosening of external requirements stated above, additional anticipated characteristics, or ancillary information not really relevant as a specification. These are expected to be met, but subject to change. Testing these additional characteristics will not be a priority.

Conversion characteristics	Bit resolution	12 bit (10 bit or 14 bit build option using pin-compatible alternate ADC chips). First couple of boards will be 14 bits.
	Sample clock source, ext	required input >1 V/ns differential slew rate should be sufficient
	Channel-channel skew of effective sampling apertures	<2 ns
	Temperature coefficient of effective sampling aperture delay relative to ext input	Within +/- 10 ps/K
	INL	<0.1%, measured with 10 MHz sinewave
System timing and rates	Acquisition buffer depth	2048 points (16.4 μs @ max sample rate)
	Rate capability	>200 kHz Poisson trigger rate with <0.1% deadtime if VME readout is maintained at average >10 Mbytes/s (per module), and assuming "typical" event data sizes (needs discussion of course)
	Data latency (sampling to acquisition buffer)	8 cycles (64 ns @ max sample rate)
Infrastructure	Mechanical	Constructed as a main board including 36 ADC channels and a mezzanine board with 36 more channels
	Power	Expect 60 – 65 W actually. Probably about 10 A load on +5 V supply. ***Full crate will require 230 A supply option on +5 V.***
	ADC chip power (for reference, gives an idea of the power floor)	41 W @ max sample rate, including 80% supply efficiency factor.
	VME transceivers	SN74VMEH22501 (except IRQn#)
	SYSRESET# action	Force clear all FPGA configurations, flush all FIFO's

Front panel LED's	• VME activity • Trigger • Busy out • Input signal activity • Sample clock valid

Revision history (of this document)

3/3/2008

1. Input signal characteristics, in particular the input impedance and signal range, revised to reflect test results with GAS-1 preamp.
2. Fast control inputs and busy output now selectable P2 or VXS P0. (If special CBLT is required, CBLT lines will also be optionally P2 or VXS P0. This has not been written in yet.)
3. Clarified pulser trigger source, it is just a special case of fast control input.
4. Some cleanup of text/style.