Bench Measurements of the Gas – 1 ASIC
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Introduction: We report on bench measurements of transient and direct current behavior of the GAS-1 ASIC made using the built test board and 64-lead chip socket for the GAS-1 ASIC. This ASIC appears to be fully functional with somewhat higher power consumption and higher gain than expected from simulations. Note that the transient results reported have been measured with a 34.5 ohm resistance across the outputs instead of the 124 ohm design load. The current based output easily accommodates different loads at the expense of voltage gain.

1. Transient Behavior

Detailed examination of the behavior of GAS-1 ASIC chip no. 1 indicates a linear gain response to impulses within the range of 10 to 300 fC. Reducing the output current offset (the current differential (AOUT_X – BOUT_X)) improves linearity but reduces the range of linear behavior for large impulse charges. Analysis of a ten-chip sample of the GAS-1 ASIC yielded 80 out of 80 working channels, with an average gain of 3.5 mV/fC across 124Ω for an unaltered chip running with a 2.52-V power supply.

1.1 Charge Injection Circuit

To create a charge impulse in the fC range, a LeCroy 9210 pulse generator outputs a 2.0 KHz square-wave signal to the short-pulse charge injector illustrated below. The BNC cable from the LeCroy is 50Ω-terminated at the injector. The charge injector connects to AIN or BIN pins of the test socket, depending on the polarity of the incoming signal.

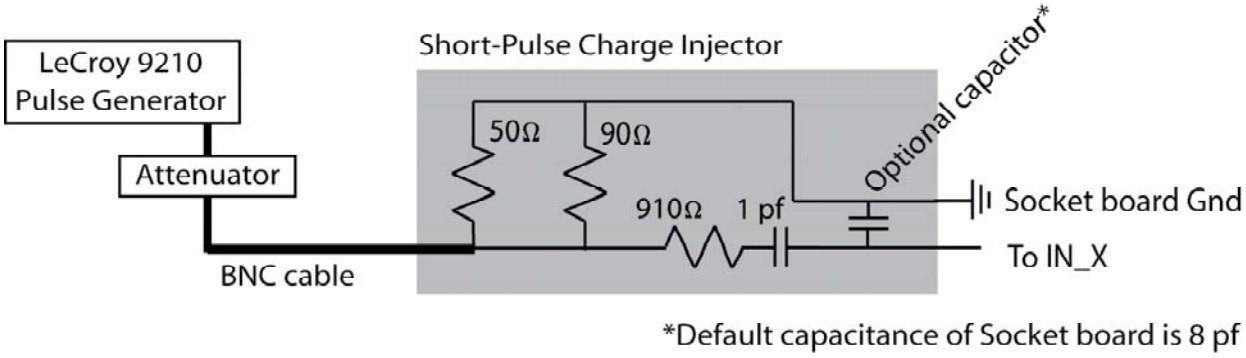


Figure 1: Charge Injection Circuit with Short-Pulse Charge Injector

In other chip tests, a similar charge injector imitates the ion tail from a CF_4 straw. Again, the LeCroy pulse generator sends a square-wave signal through the charge injector circuitry to the chip input. Below are LeCroy oscilloscope images of a positive impulse from both Short-Pulse and CF_4 Ion Tail charge injectors. (NOTE: All LeCroy images are taken across an effective resistance of 50Ω in the case of direct measurement of signals, or 34.5Ω in the case of output offset measurements.)

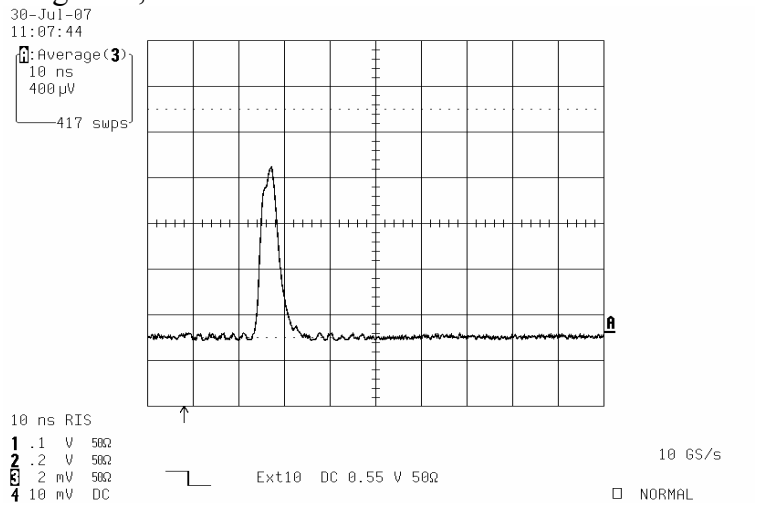


Image 1: Short-Pulse Injector Charge, measured with LeCroy Oscilloscope

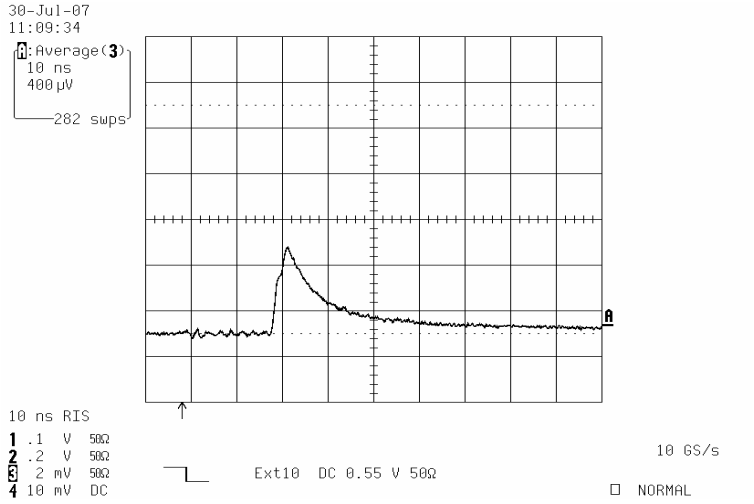


Image 2: CF_4 Ion Tail Injector Charge, measured with LeCroy Oscilloscope

1.2 Transient Readout Technique

A Mini Circuits T1-6 transformer reads the voltage differential (AOUT_X – BOUT_X) across the 124-Ω reference bus. Due to an internal parallel resistance of ~1kΩ between AOUT_X and AIN_X, the effective resistance across A and B is 112Ω. The transformer is connected by BNC cable to a LeCroy 9354A 500MHz oscilloscope and DC 50Ω-coupled. The LeCroy pulse generator externally triggers the oscilloscope.

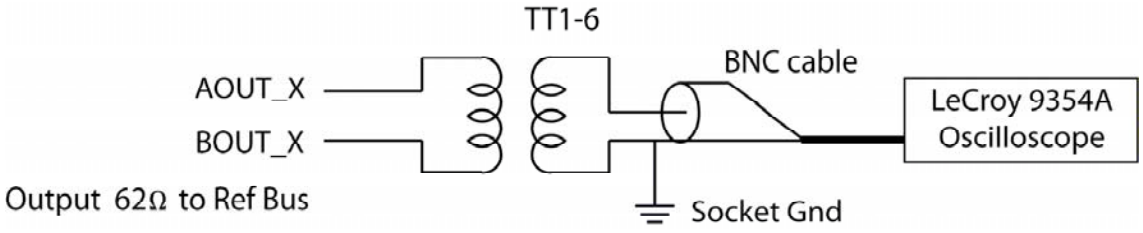


Figure 2: Transient Readout Schematic

Because the measurements from the oscilloscope were performed across 50Ω || 112Ω = 34.5Ω, and not across 124Ω, the output response is attenuated by a factor of 3.6. The data and graphs below are labeled according to their termination.

1.3 Bench Measurement Test Operation

The GAS-1 ASIC is designed to operate using a 2.5-Volt power supply; however, we also ran tests with 2.4 Volts delivered to the chip to observe lower-power behavior. Using a 100-KΩ potentiometer connected from AIN_X to ground we were able to vary the output offset (AOUT_X – BOUT_X) to determine its effects on output response to an impulse. We tested chips using both the short-pulse charge injector and the CF_4 ion tail injector. Unless otherwise noted, all measurements were performed using the default switch settings of the chip. All settings are properly labeled with respect to termination, power supply and nature of input charge.

1.4 Transient Behavior Measurements and Results

1.4.1 Response to the Short-Pulse Charge Injector

Below are voltage response waveforms from input charges of -10, -20 and -51 fC, using the short-pulse charge injector. The waveforms show adequate tail cancellation and a rise time of less than 10 ns for charges smaller than ~300 fC.

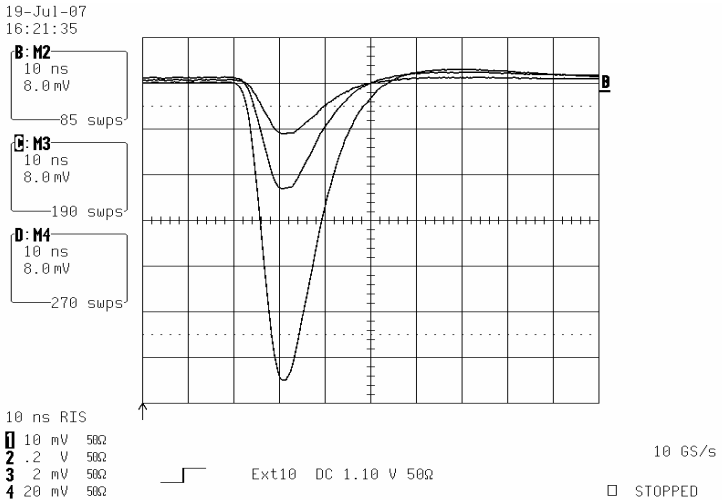
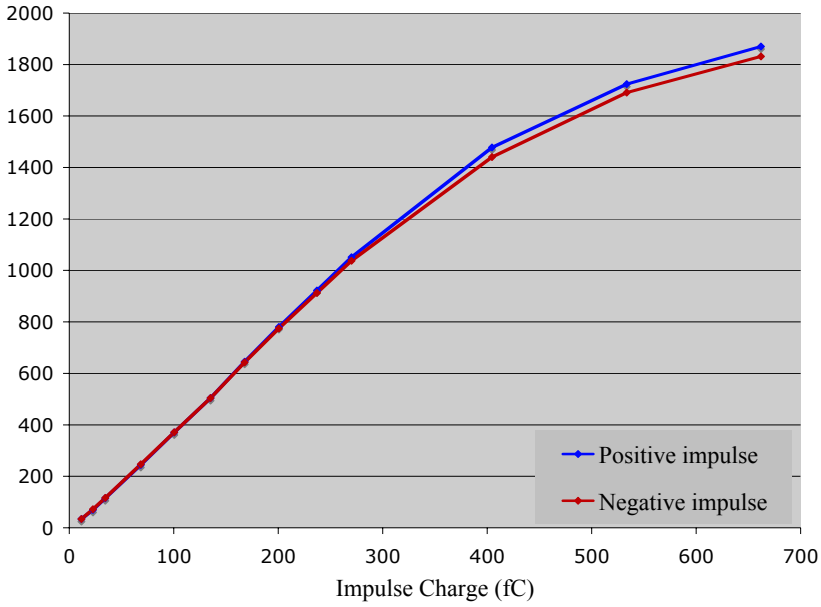


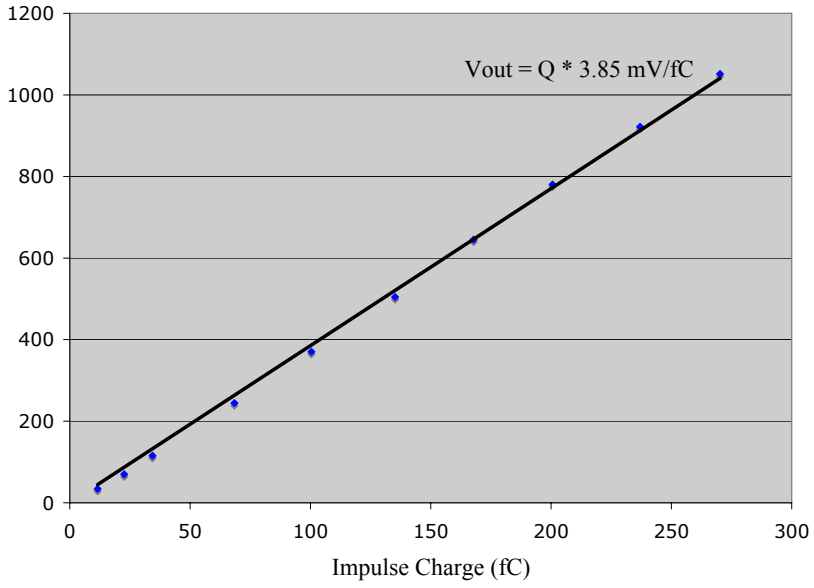
Image 3: Output Responses to varied input charges (from top to bottom): -10, -20, -51 fC

Measurements across a wide range of input charges show that the response to short-pulse charges is approximately linear between about 10 and 300 fC, with a gain of about 4 mV/fC (across 124Ω) using the hand-wired test socket. Beyond a 300 fC input charge, the output response becomes attenuated and linearity breaks down. Additionally, we found that both positive and negative impulses into BIN_X and AIN_X (respectively) behaved almost identically. Below is a graph comparing the positive and negative responses of an unaltered chip powered at 2.52 Volts.



Graph 1: Output Response to Short-Pulse Charge; Chip 1, Channel 1

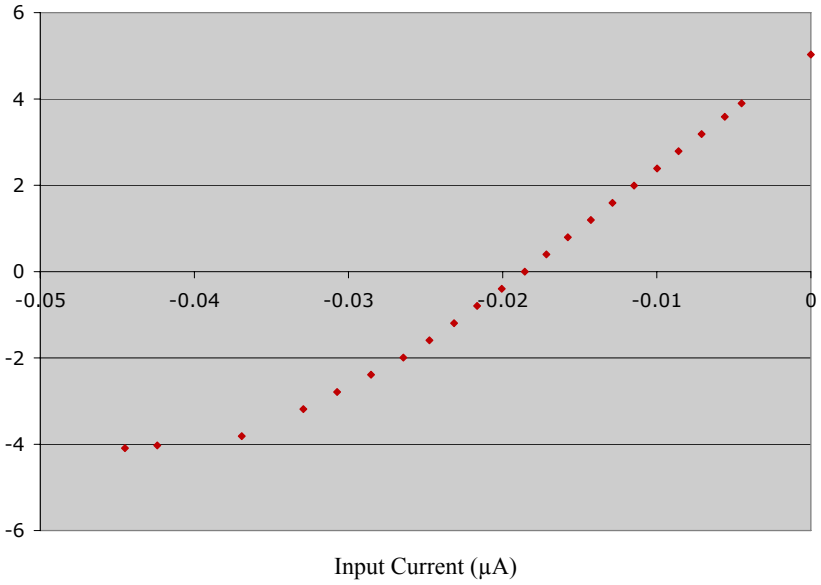
Below is a graph of output response to low-range charge impulses (below 300 fC). The response is nearly linear, with a gain of 3.85 mV/fC (measured over 124Ω):



Graph 2: Low-Range Output Response to Short-Pulse Charge; Chip 1, Channel 1

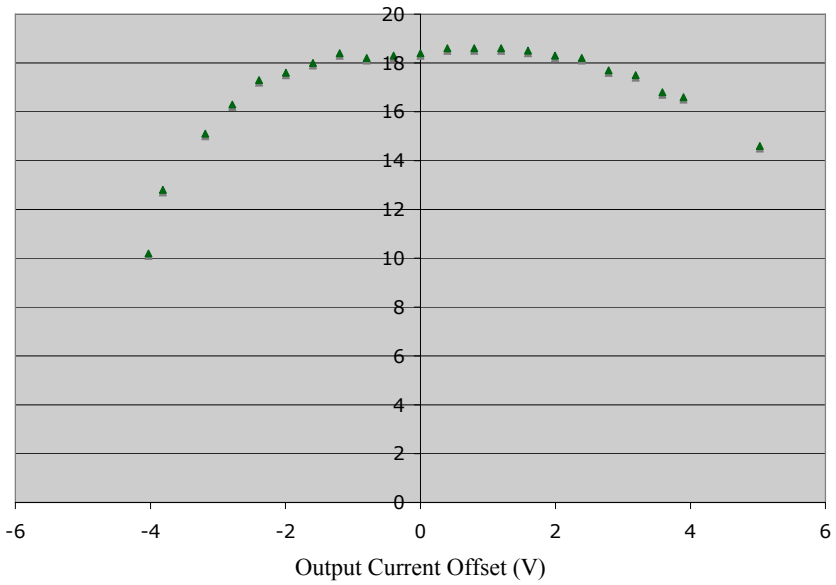
1.4.2 Output Performance with Varied Output Current Offset

By placing the 100-KΩ potentiometer between AIN_X and ground, we varied the output offset to explore its effects on output response behavior. Below is a graph of the relationship between the input and output offset current, varied by using the potentiometer.



Graph 3: Output Current Offset Response to Input Current

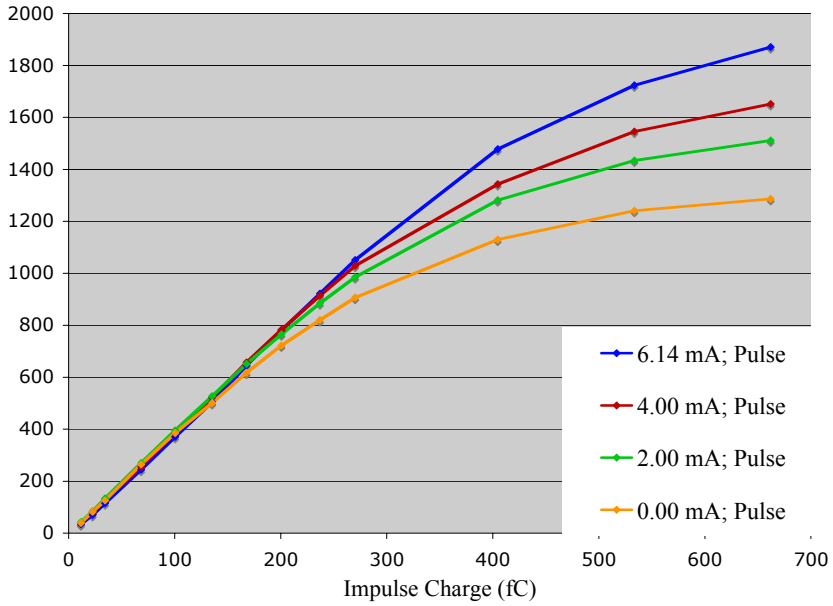
Using the potentiometer, we varied the output current offset and studied the output response to a short-pulse +20 fC charge with varied output current offsets. We are primarily concerned with the range of zero to maximum output current offset.



Graph 4: Output Response to a ~20 fC charge for varied Output Current Offset

The maximum output response occurs for output offsets between -1.0 and +2.5 mA. 5However, a wide-range input charge analysis of response at varying output offsets shows that the maximum current offset has the widest dynamic range. Decreasing the offset causes the output response to attenuate at charge sizes less than 300 fC, significantly decreasing its linear dynamic range. A decreased offset does improve the linearity of lower-range results, but the effect is minimal and only noteworthy in cases where precise linearity is required. Varying the output offset does not

significantly change the shape of the resulting waveform. Below is a graph comparing output response to a normal impulse at output offsets of 0.0, 2.0, 4.0 and 6.15 (output default) mA for a chip powered with 2.52 Volts:



Graph 5: Output Response to Short-Pulse Impulse for varied Output Offsets

Similar tests run with the chip powered at 2.4 Volts showed similar results with respect to output offset. Decreasing the chip power from 2.52 to 2.40 Volts decreases output response by a factor greater than 2.52 / 2.4, but not by a significantly greater amount.

1.4.3 Response to the CF_4 Ion Tail Charge Injector

Waveforms of the response to the CF_4 ion tail charge injector indicated that the tail cancellation processes were not completely effective in eliminating the tail signature. However, the GAS-1 ASIC can still be effective in this instance; a recorded event effectively spans fewer than 60 ns. Below is a sample waveform resulting from a 100-fC input charge from the CF_4 ion tail injector; it exhibits a rise time of ~15 ns.

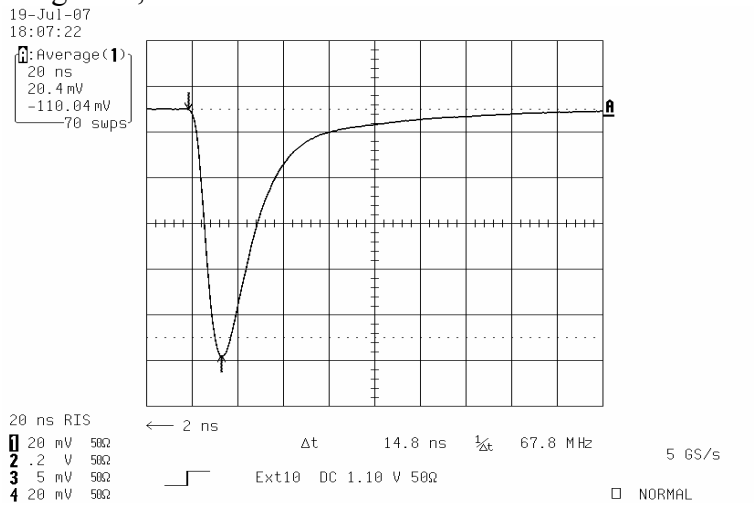
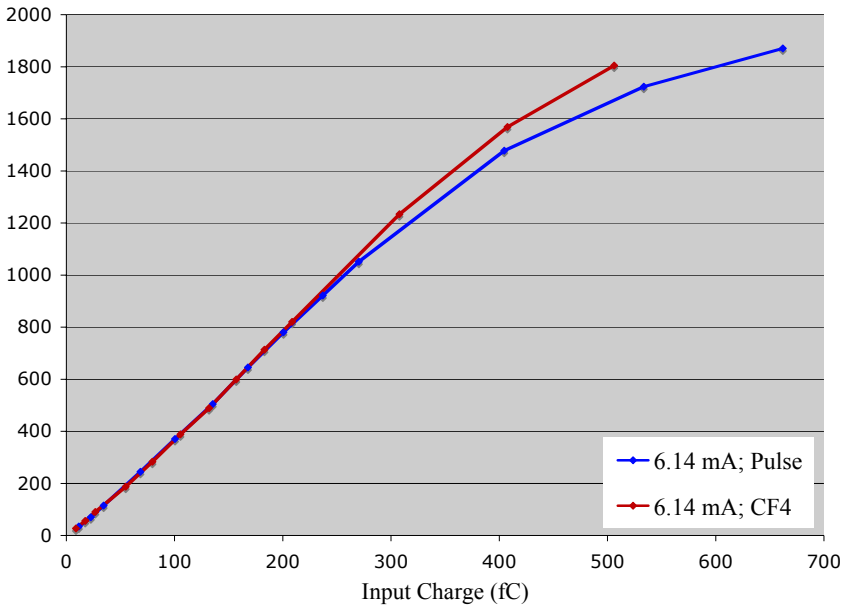


Image 4: Response to 100 fC Charge from CF4 Ion Tail Injector

Measured across 34.5Ω

Despite the imperfect shaping performance with respect to tail cancellation, the gain and dynamic range of output response to CF_4 closely matches that of the short-pulse impulse charge. CF_4 response is also affected similarly by changes in output offset and chip power supply. Below is a graph comparing the dynamic ranges of responses to CF_4 and short-pulse impulses:



Graph 6: Comparison of Responses to CF4 and Short-Pulse impulse input charges

1.4.4 Response to Varied Input Capacitance

The hand-wired test socket has an internal input capacitance of 8 pF; increasing this capacitance up to ~70 pF contributes to minor attenuation and delay effects on the resulting waveform's peak and rise time. Below is a graphic comparing the responses to 20-fC short-pulse impulses for input capacitances of 8 (internal capacitance), 18, 33 and 64 pF:

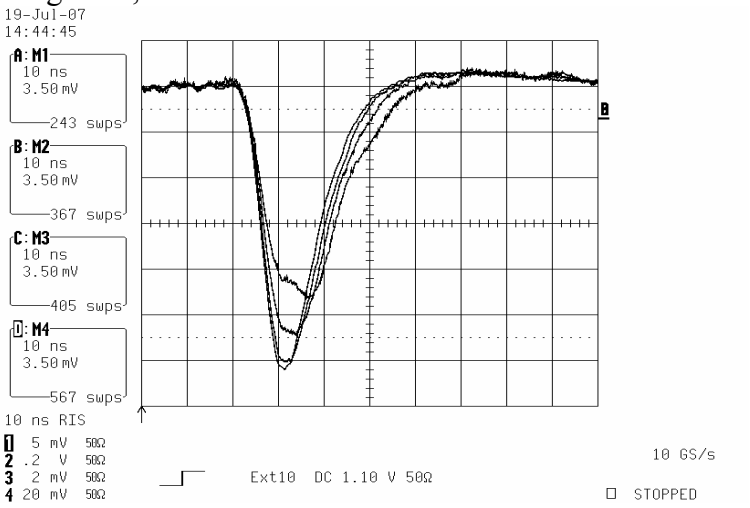
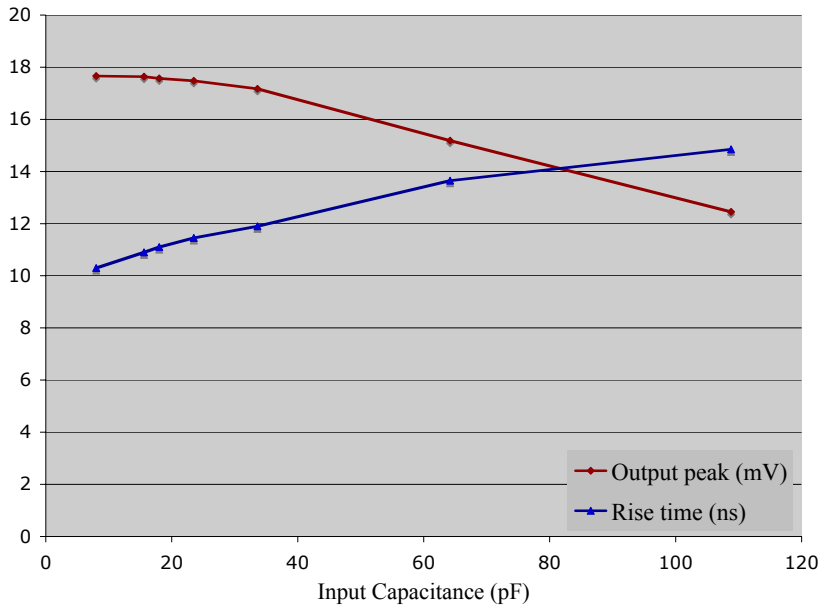


Image 5: Response to Increased Input Capacitance for a 20-fC Short-Pulse Impulse

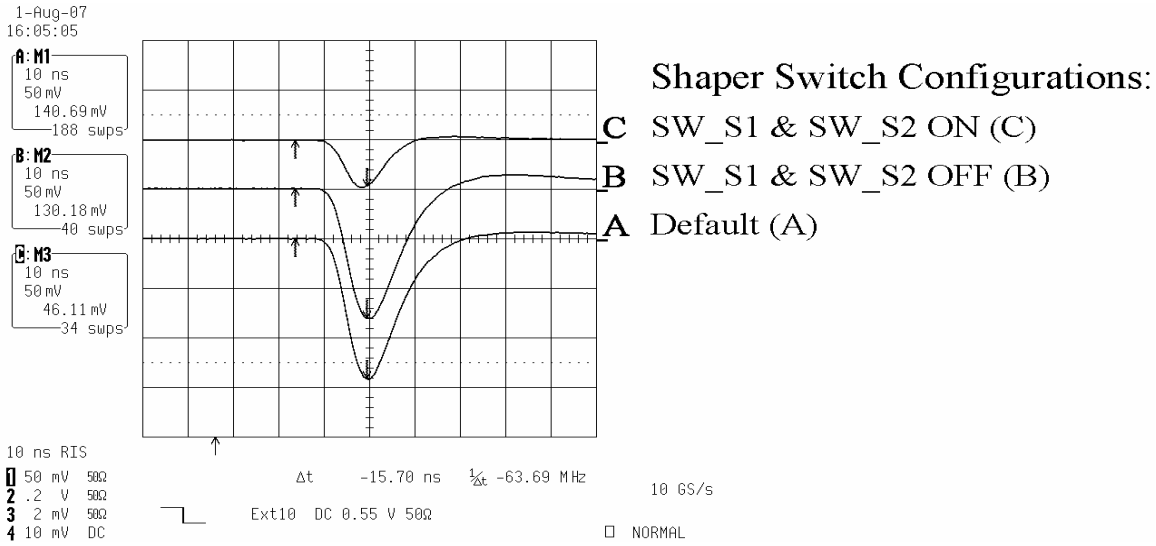
Below is a graph comparing output response to a ~20 fC short-pulse impulse for input capacitances varying between 8 and 108 pF (responses are measured over 34.5Ω). Response amplitude is attenuated by approximately .06 mV / pF (measured across 34.5Ω).

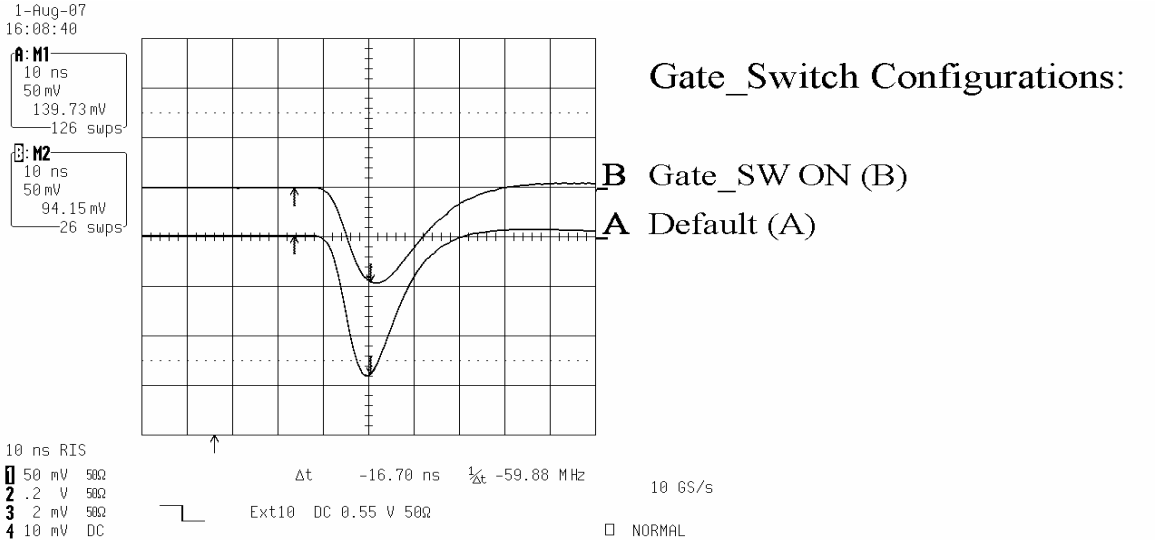


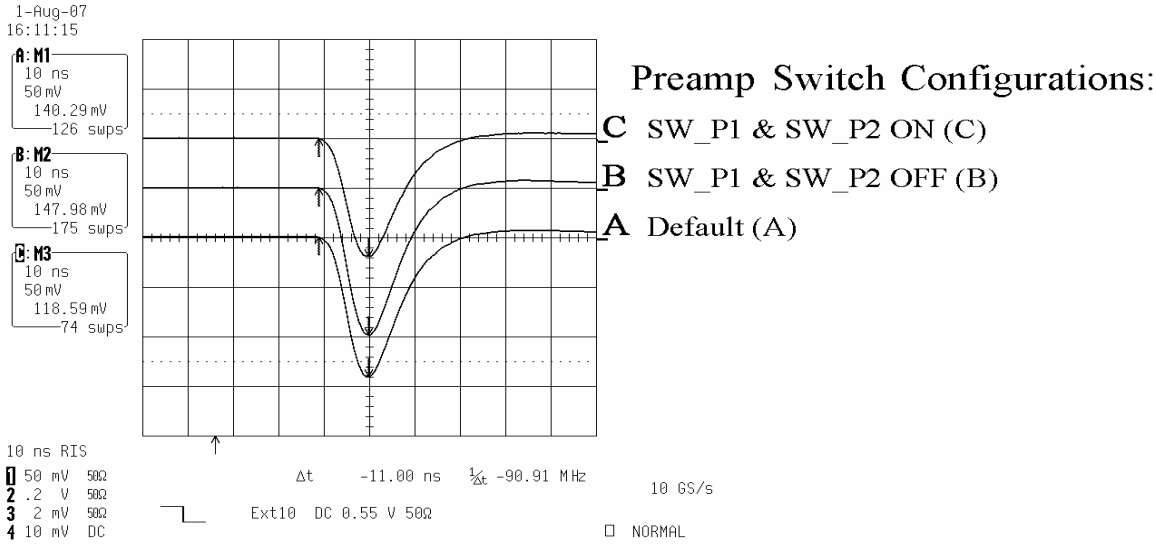
Graph 7: Output Response to -20.6 fC Short-Pulse Charge for Varied Input Capacitance

1.4.5 Switch Behavior

Below are comparisons of chip response to various switch configurations. Measurements were performed on chip no. 1, which was powered using 2.52 Volts. A +135-fC pulse was sent to BIN_1 using the short-pulse charge injector. Unspecified switch positions are assumed to be in the default position.


1-Aug-07
16:05:05
A:M1
10 ns
50 mV
140.69 mV
188 swps
B:M2
10 ns
50 mV
130.18 mV
40 swps
C:M3
10 ns
50 mV
46.11 mV
34 swps
10 ns RIS
1 50 mV 50Ω
2 .2 V 50Ω
3 2 mV 50Ω
4 10 mV DC
Δt -15.70 ns 1/Δt -63.69 MHz
Ext10 DC 0.55 V 50Ω
10 GS/s
NORMAL
Shaper Switch Configurations:
C SW_S1 & SW_S2 ON (C)
B SW_S1 & SW_S2 OFF (B)
A Default (A)


1-Aug-07
16:08:40
A:M1
10 ns
50 mV
139.73 mV
126 swps
B:M2
10 ns
50 mV
94.15 mV
26 swps
10 ns RIS
1 50 mV 50Ω
2 .2 V 50Ω
3 2 mV 50Ω
4 10 mV DC
Δt -16.70 ns 1/Δt -59.88 MHz
Ext10 DC 0.55 V 50Ω
10 GS/s
NORMAL
Gate_Switch Configurations:
B Gate_SW ON (B)
A Default (A)


1-Aug-07
16:11:15
A:M1
10 ns
50 mV
140.29 mV
126 swps
B:M2
10 ns
50 mV
147.98 mV
175 swps
C:M3
10 ns
50 mV
118.59 mV
74 swps
10 ns RIS
1 50 mV 50Ω
2 .2 V 50Ω
3 2 mV 50Ω
4 10 mV DC
Δt -11.00 ns 1/Δt -90.91 MHz
Ext10 DC 0.55 V 50Ω
10 GS/s
NORMAL
Preamp Switch Configurations:
C SW_P1 & SW_P2 ON (C)
B SW_P1 & SW_P2 OFF (B)
A Default (A)

Significant attenuation affects are registered in the configuration in which both shaper switches are on. This effect was previously unaccounted for in simulations; however, the issue could be related to the specific bench configuration and test socket. Further analysis and simulation would be required to better understand the behavior of shaper switch 1.

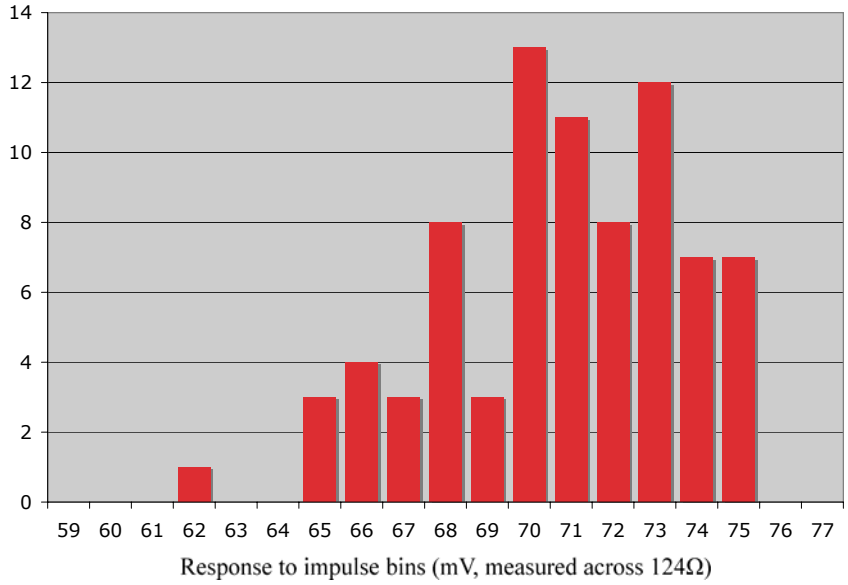
Turning both shaper switches off results in greater tail cancellation than that of default, as exhibited in the image. The gate switch serves to attenuate the signal to 2/3 its original size, as well as delay the rise time of the waveform. Preamp switches increase the magnitude of the signal when off, and increase it when both are turned on (without producing significant effects to waveform shape).

1.4.6 Chip Response Yield and average Measured Gain

After testing 80 channels on 10 GAS-1 ASIC chips for performance in response to a -20-fC short-pulse charge, we found an average gain of 3.5 mV/fC (measured over 124Ω). Below is a table and a histogram outlining our results on a chip-by-chip basis.

Table 1: Response (measured across 124Ω) to a -20 fC short-pulse charge; 10-chip sample

	Response to 20fC pulse (mV)		Gain (mV/fC)	
Chip no.	Mean	Std	Mean	Std
1	70.13	1.36	3.51	0.07
2	73.01	1.32	3.65	0.07
3	72.47	1.51	3.62	0.08
4	73.4	0.83	3.67	0.04
5	72.60	1.29	3.63	0.06
6	65.46	1.95	3.27	0.10
7	69.01	1.05	3.45	0.05
8	69.46	2.02	3.47	0.10
9	68.92	1.69	3.45	0.08
10	68.20	1.96	3.41	0.10
10-Chip Sample	70.27	2.85	3.51	0.14



Graph 8: Histogram of Output Response to a -20 fC impulse - 10-chip sample

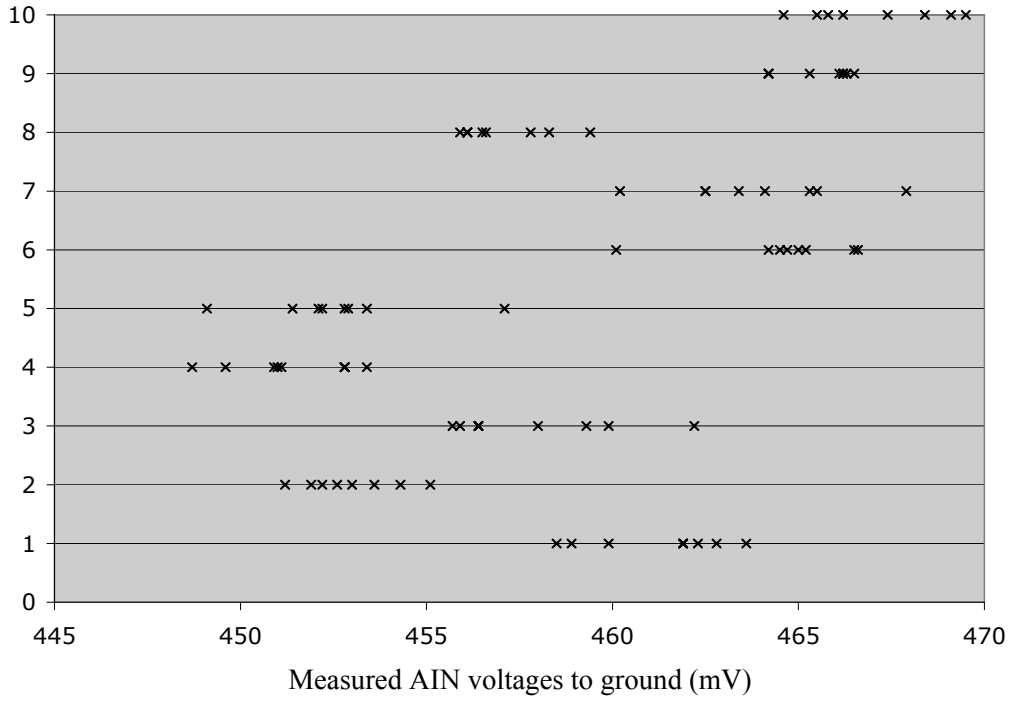
2. Direct Current Measurements and Chip Yield

2.1 DC Measurements of Input and Output Offsets

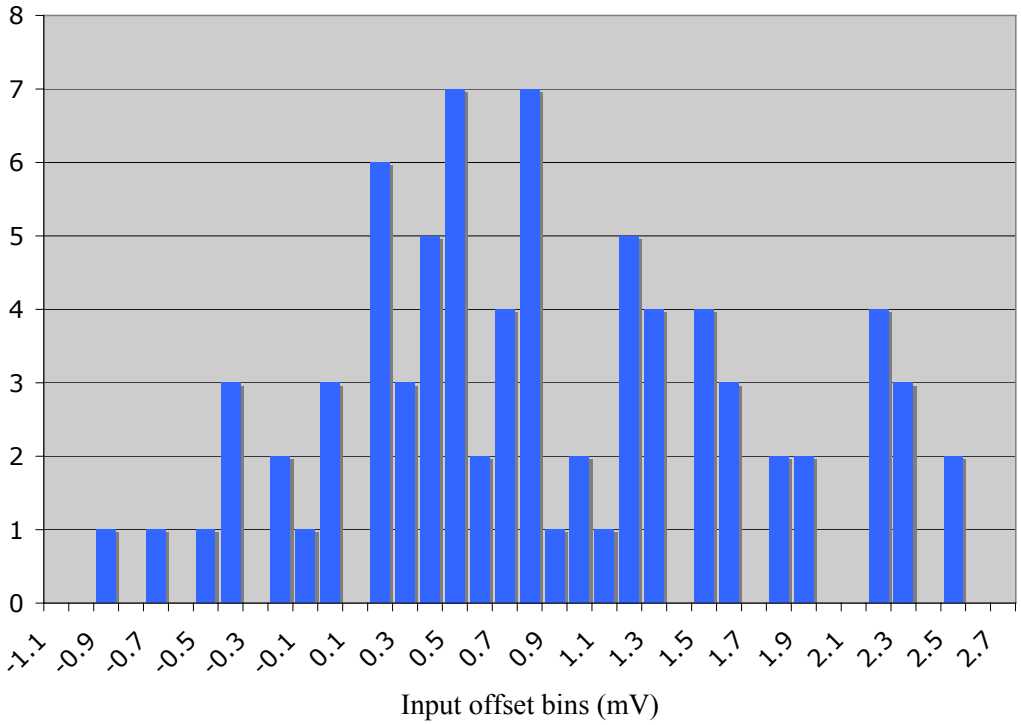
Using the LeCroy pulse generator and a Fluke 179 Multimeter for DC measurements, we tested channels from 10 chips for DC characteristics of channels. All 80 channels tested functioned properly; cross-chip channel statistics and histogram analyses for chips powered with 2.52 Volts are included below.

Table 2: DC Input and Output Offsets for a 10-chip sample

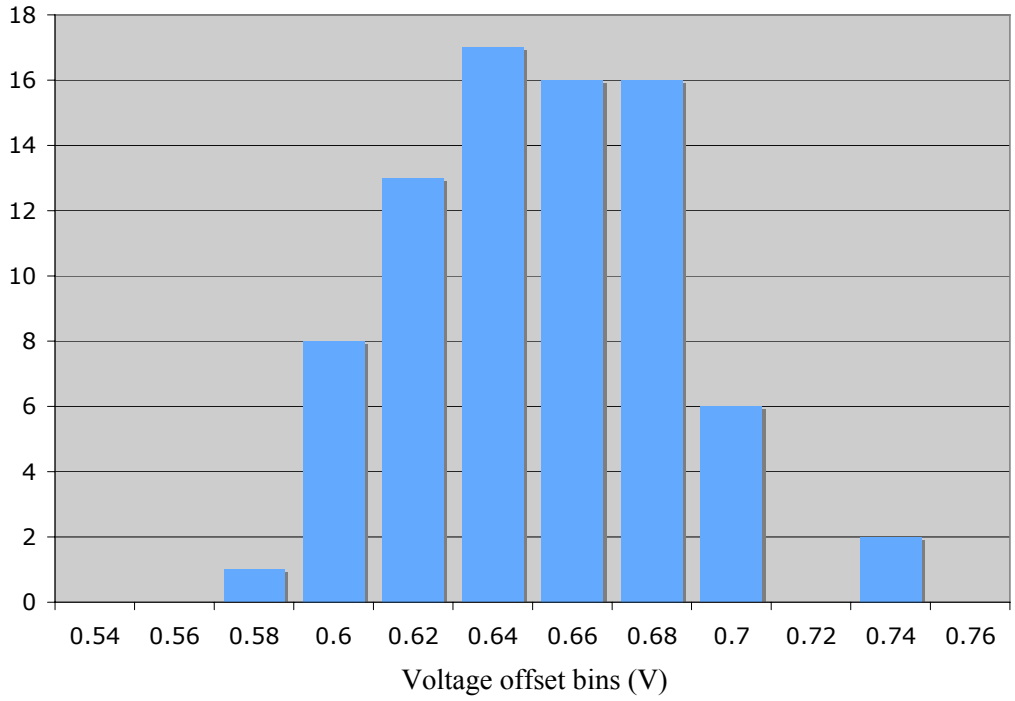
	AIN to gnd (mV)		(A-B)IN (mV)		(A-B)OUT (V)	
Chip no.	Mean	Std	Mean	Std	Mean	Std
1	461.23	1.88	1.70	0.33	0.65	0.02
2	452.99	1.29	1.53	0.34	0.64	0.04
3	457.98	2.32	0.15	0.33	0.64	0.04
4	451.29	1.64	-0.40	0.30	0.61	0.02
5	452.63	2.24	0.39	0.23	0.61	0.02
6	464.60	2.02	1.00	0.30	0.66	0.04
7	463.93	2.34	0.61	0.35	0.65	0.02
8	457.09	1.27	2.26	0.19	0.66	0.03
9	465.63	0.95	0.78	0.30	0.66	0.03
10	467.06	1.81	0.60	0.36	0.65	0.02
Over 10 chips	459.44	5.85	0.86	0.81	0.64	0.03



Graph 9: AIN Voltages to Ground, Chip-by-Chip (10-Chip sample)



Graph 10: Histogram of Input Offsets; 10-chip sample



Graph 11: Histogram of Output Offsets, measured across a 62Ω Load – 10-chip sample

2.2 GAS-1 ASIC Power Consumption

Below is a 10-chip analysis of the average total current and power per channel. This data was taken while the outputs of each channel were connected through 62Ω to reference bus; removing the reference bus decreases the power per channel by about 10 mW. Additionally, adjusting the output current offset (A-B)OUT to 0 does not change the power dissipation of the chip.

Table 3: Average Current and Power Loss in a 10-chip sample – 2.521-Volt supply

	Total Current (mA)	Power per Channel (mW)
10-chip Mean	157.98	49.37
10-chip Std	4.31	1.35

Below are the results from testing various switch combinations for their effects on power draw for Chip number 1. The power per channel remains between 44 and 60 mW.

Table 4: Preamp Switches' effect on Power Consumption, 2.521-Volt supply

Column labels: [P1] [P2]

0=default, 1=non-default	0 0	1 0	0 1	1 1
Total Current (mA)	156.56	166.02	151.20	163.02
Total P /chan (mW)	48.93	51.88	47.25	50.94

Table 5: Shaper Switches' effect on Power Consumption, 2.521-Volt supply

Column labels: [S1] [S2]

0=default, 1=non-default	0 0	1 0	0 1	1 1
Total Current (mA)	156.56	190.68	143.06	178.82
Total P /chan (mW)	48.93	59.59	44.71	55.88

Table 6: Gate Switch's effect on Power Consumption, 2.521-Volt supply

Column label: [Gate_SW]

0=default, 1=non-default	0	1
Total Current (mA)	157.16	157.16
Total P /chan (mW)	49.11	49.11

The GAS-1 ASIC is designed to operate between 2 and 3 Volts; however output response performance varies significantly within this range. Below are the response levels

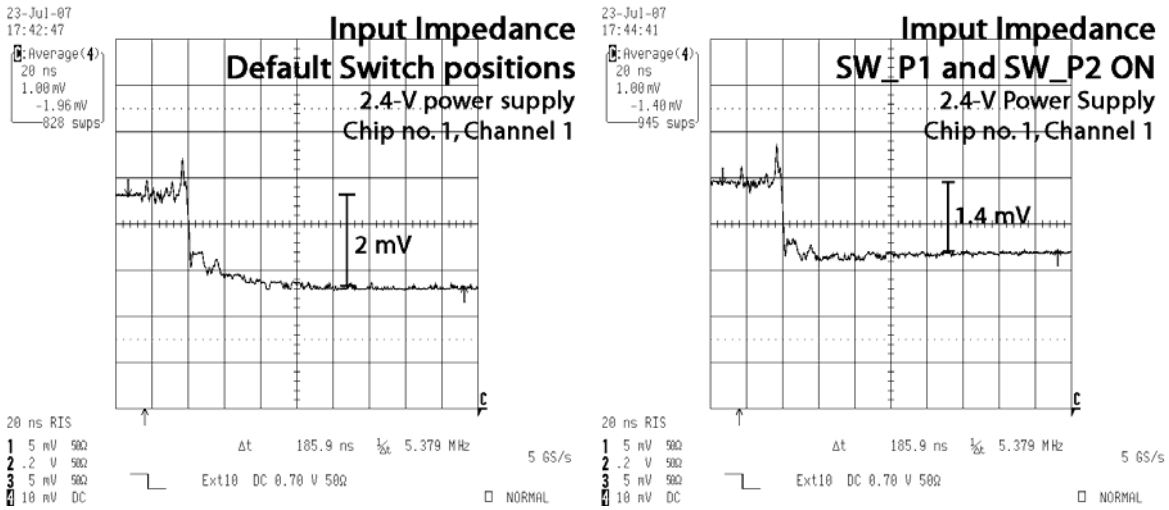
2.3 Input Impedance

Using the LeCroy pulse generator to send a 200-mV signal though a 10KΩ resistor in series with the input to ground, we were able to determine the input impedance. Impedance tests were run from channel 1 of chip number 1 with the power supply set at 2.4 and 2.521 Volts. The preamp switch settings ([P1] [P2]) were also varied.

Table 7: Input Impedance with varying preamp and power chip configurations

Chip Voltage supply	Preamp Setting	Input Impedance (Ω)
2.400	Default	101.52
2.400	OFF OFF	73.54
2.400	ON ON	277.49
2.521	Default	72.015
2.521	OFF OFF	66.95
2.521	ON ON	154.35

Below are time-dependent impedance graphs for a 2.4-V power supplied chip and varied preamp switch configurations:



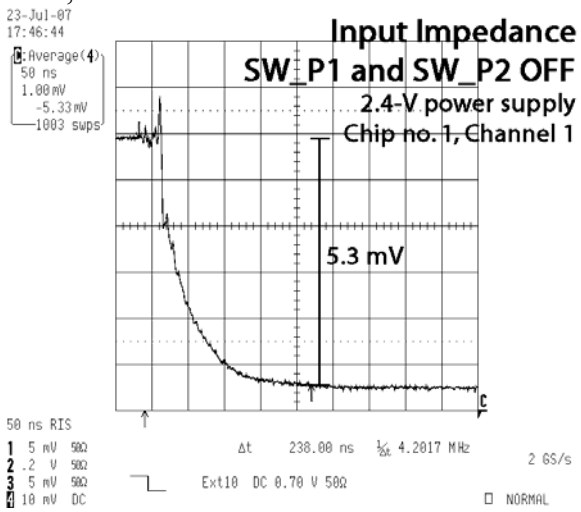


Image 6: Input Impedance for varied Preamp Switch Configurations

3. Input and Output Protection

To test the efficacy of the input protection measures, we used the setup outlined below to inject high amounts of charge into one of the inputs.

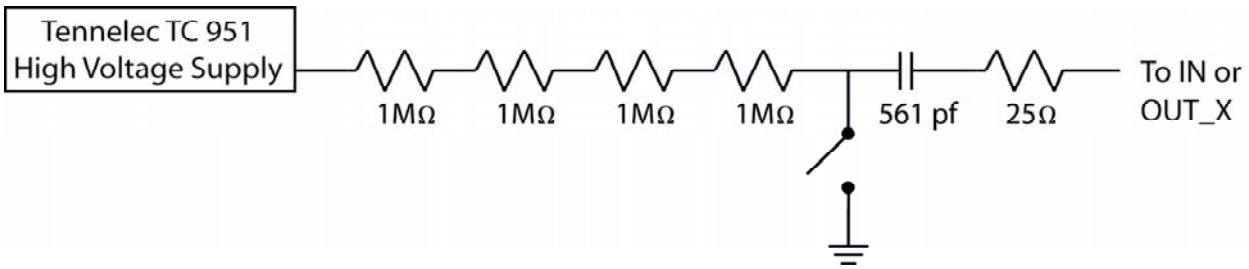
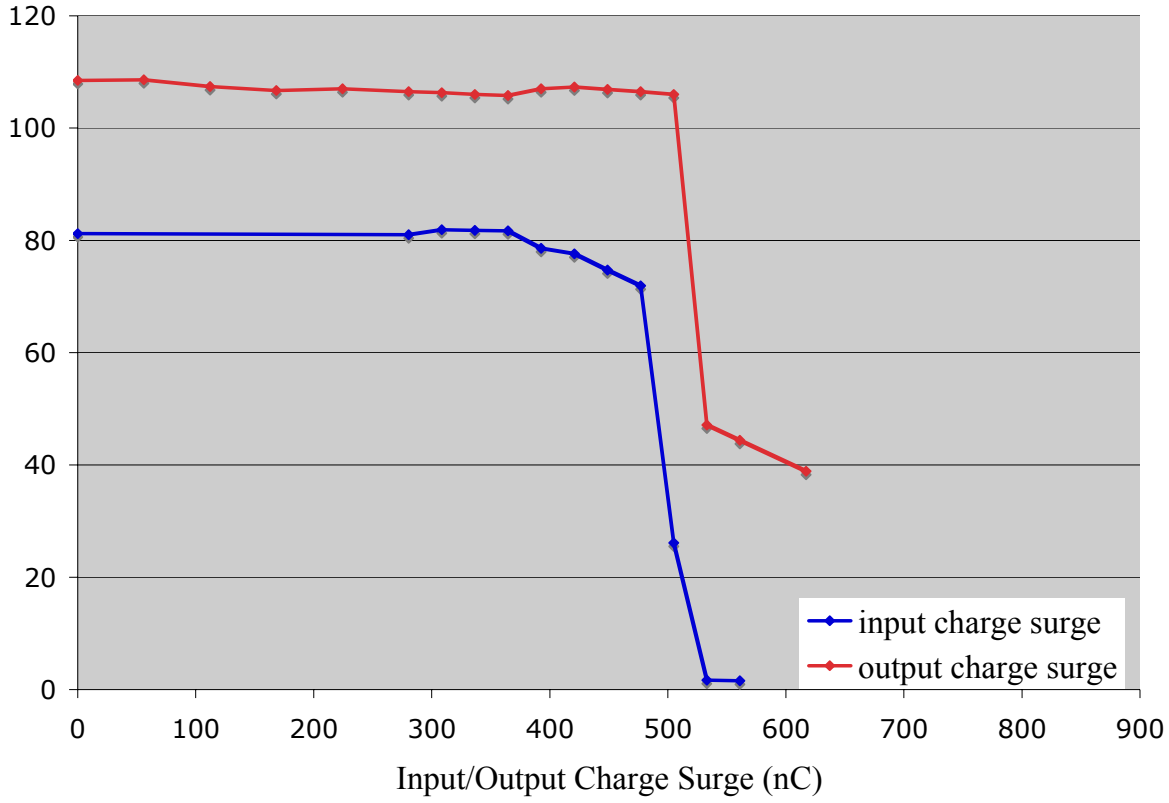


Figure 3: Test setup for input and output protection measurments

Input and output protection tests were performed on chip 11. With four channels having been broken, the remaining four non-damaged channels continued to function. Only after the fifth channel was destroyed did the chip cease to function completely. Channels 8, 7, 6, 5, and 1 were broken in succession during the test.

Below are our results; we found that channels functioned properly up to input charge surges of 475 nC (850 V from the power supply), and output charge surges of 450 nC (800 V supplied).

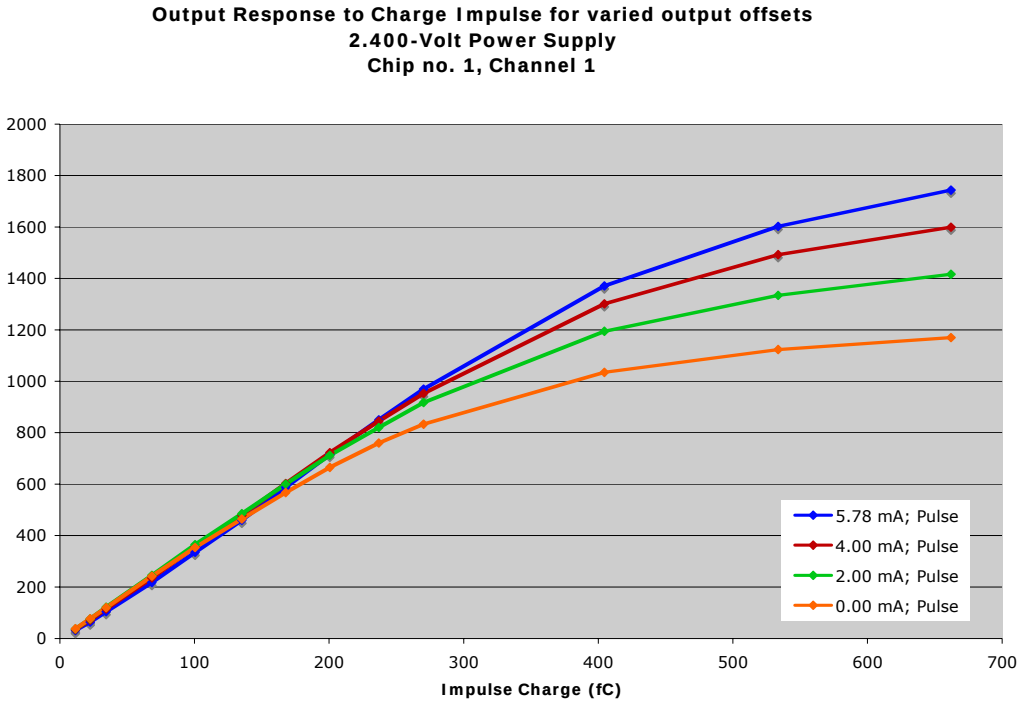


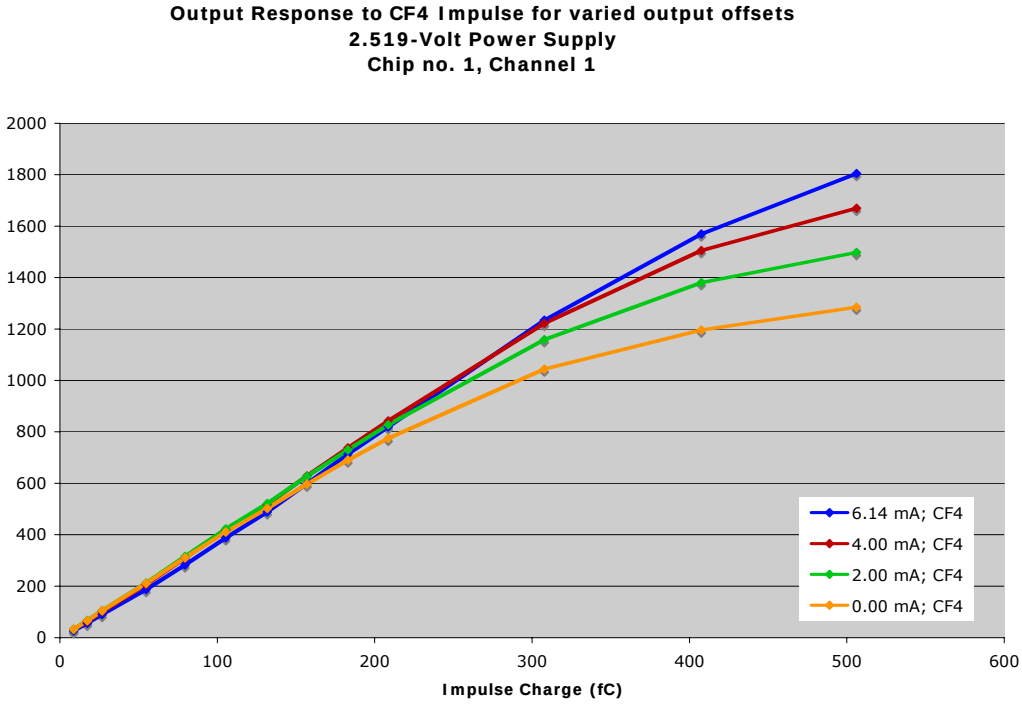
Graph 2: Output Response to input and output charge surges

In this instance, the input and output charge surge data was collected on the same chip, with the input data recorded first. Therefore. the discrepancy between normal output responses (~80 fC in the case of input protection and ~110 fC in the case of output protection) may have been caused by a redistribution of power (~400 mW) to fewer than 8 working channels. In any case, the data still suggests that channel input and output will be protected up to ~500 nC.

4. Reference Section

Below are other graphs containing reference plots for various power supply and pulser-type configurations.





Output Response to CF4 Impulse for varied output offsets
2.400-Volt Power Supply
Chip no. 1, Channel 1