March 18, 2008

GLueX Front End Analog Signal Processing ASIC

This report describes an eight channel ASIC being designed to meet the front end signal processing requirements for several types of gas proportional detector sub-systems in the Jefferson Laboratory GlueX detector. These include both cathode readout strips and wire anode pickups. The primary use of the ASIC will be to provide a high density, low noise, on detector sensor readout suitable for driving a differential analog signal to an off detector shaper and ADC board being developed at Indiana University. The analog outputs will provide both timing and de/dx energy loss measurements. A further objective will be to add a selectable timing comparator output for the 2304 wires of the CTC. This report will cover the ASIC design and submissions in two parts: First the design and submission of the GAS-1 ASIC with amplifier, shaper and line driver blocks, and second the revised design (in progress) with improvements based on measurements of the GAS-1 and a selectable timing comparator option.

I. GAS-1 ASIC

Channel Blocks –

The GAS-1 design is modeled on several successful earlier designs by our group: The ASDQ [1]currently in use at Fermi National Laboratory in the CDF experiment and the ASDBLR [2] used in the CERN ATLAS TRT tracker.
The basic blocks are shown in Figure 1.

Input Protection-

The Negative (anode) input protection is formed using 4 custom designed P-N diodes with 3 positive and two negative 50um X 6um terminals in $60um^2$ N-Well tubs. Poly resistance in series with these diodes helps encourage current sharing and avoid thermal runaway in any one diode.
(See Appendix A) of about 10 ohms.

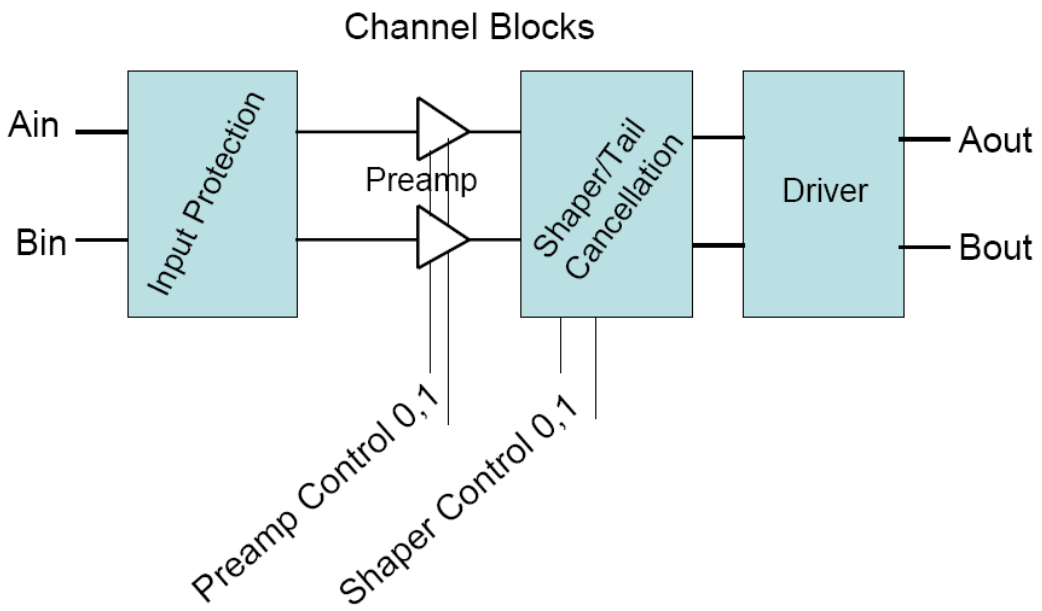


Figure 1 Basic Channel blocks of the fabricated GAS – 1 ASIC.

Preamp - We have chosen to use dual preamps for each channel to accommodate positive and negative inputs, provide excellent DC balance for the differential stages that follow and to allow the rejection of pickup by implementing common mode techniques. The additional intrinsic noise will vary depending on the implementation of the hookup and in any case should be no worse than 40% higher than with a single ended input in the case of equal capacitive loading at the inputs. The preamp circuit configuration is a cascoded common source. For good low noise performance the input transistor is operated in moderate inversion. Its dimensions are 3900um X 380nm and current is approximately 1mA. Current is supplied to the amplifying node (drain) of the NMOS cascode by a fixed PMOS current source. An 18K ohm resistor to ground at this node is used to reduce the variation in impedance at this node due to the relatively unpredictable range of output impedances of the MOSFETs. The feedback network consists of a 8k resistor in parallel with a 1.2pF capacitor driven by a source follower attached to the cascode drain. The dual preamps are intermingled in the layout to help improve DC balance and common mode rejection. The peaking time of the preamp (with layout parasitics) is 2.2ns and the dynamic range is in excess of 1pC. (See basic schematic in Appendix B)

Shaper – The Dual preamps set the input bias for the differential shaper. In this design one preamp is used for negative (wire anode) signals and the other is used for positive (cathode) signals. With this arrangement the signal in the shaper always has the same polarity. In order to maintain a large fraction of the available dynamic range, an offset is added to the first shaping stage using a PMOS current mirror. A dummy PMOS device of the same size balances the load on the on the other first stage output. This offset increases the available dynamic range by about 30% from the zero offset case. The shaper consists of 4

shaping poles and a pole zero doublet to cancel the ion tail associated with the repulsion of the positive gas ions away from the wire after avalanche multiplication. The basic schematic in shown in Appendix C.

Line Driver - The shaper output is a differential current derived from the drains of an NMOS differential pair. Matched PMOS current mirror masters receive the current and provide reference for independent positive and negative mirror copies. These are connected such that the net current in each of the differential outputs is nearly zero for a zero offset input. An internal resistance of 500 ohms equivalent to Vdd/2 assures that the small mismatch currents do not pull the outputs to the supply rails. (See basic schematic in Appendix D)
The design goals have evolved somewhat over the two years that the ASIC has been in development. Most notably a 5X gain stage has been added to accommodate the lower induced charge collected on the cathode strip pickups.

Table 1 Initial Gas-1 Design Objectives

Input Capacitance	Up to 100pC
Input Impedance	~75 ohms
Signal Range[1]	0-350 fC
Analog Output Gain	2-3mV/fC
Peaking time	~12ns
Rate	< 300KHz
Noise	< 1fC
Power	40mW/ch
Input Protection	> .1mJ

Technology - Sub-Micron CMOS technology was chosen as a target technology due to it's availability and low cost, compared to available Bipolar and BICMOS processes. Noise performance which would be better using a bipolar technology for the relatively fast shaping time of 10ns was not considered to be a primary concern due to the relatively large signal size. The GAS-1 ASIC was originally targeted for the IBM CMOS 6SF Process. Unfortunately Multi-Project Wafer (MPW) runs through CERN have been very limited since the completion of most of the LHC experiment designs and MOSIS discouraged the use of this technology through their services. At the recommendation of MOSIS we chose to use TSMC's 0.25um triple well CMOS process. For our first run we took advantage of the deep N-Well to surround the large input transistors but left the remaining NMOS transistors in their native substrate bulk. Subsequent examination of our design led us to realize that additional linearity would be possible by using NMOS differential pairs and source followers with independent deep NWELL tubs. This is being implemented in our next design.

[1] Impulse Response of 350fC is very conservative since ionizing tracks will leave a trail of ionizations that drift in over several hundred ns.

Our first submission, design #77419, was delivered to MOSIS on April 4, 2007. We received parts back in June and reported measurement results in early August, 2007. (See Support Document GAS_1_Bench_Measurements) The measured gain (80 channel, 10 ASIC sample) was 3.5mV per fC with a standard deviation of .14fC. The response to a charge injector designed to mimic a gas proportional tube with an ion tail (t_0=1ns) showed a slight under compensation consistent with the design. The input impedance with default preamp current settings was measured to be ~100 ohms.

Table 2 GAS-1 Bench Measurement summary

Input Cap range tested	20 – 120pF
Input Impedance	72 ohms @2.5V Vdd
Signal Range	>300 fC (+ and – inputs)
Analog Output Gain	3.5 mV/fC
Peaking time 20pF / 120pFCin	10ns/15ns
Rate	Pulse shape OK
Measured Noise	158 e/pf +3000 e
Power	49mW/ch
Input Protection	> .18mJ pos, > .4mJ neg

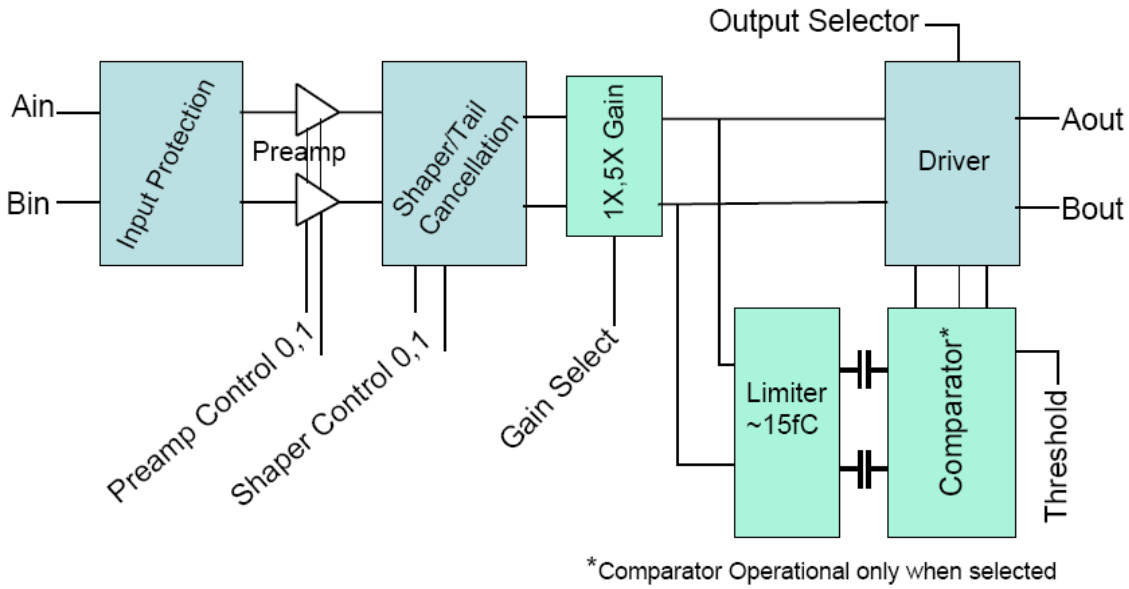
The GAS – 1 ASIC has been tested on the bench and attached to several prototype detectors. There are no known deficiencies. Design enhancements recommended by users concern reduction of power: 1) eliminate extra ASIC borne power dissipation in Thevenin equivalent circuit on each output: 1K Ohms to VDD and GND to make Vdd/2 independently for each channel. Replace with an additional ASIC pad for an on chip VDD/2 bus. Each output will have a 500 Ohm resistor to the Vdd/2 bus. 2) Identify source of extra 9mW of power dissipation observed in fabricated devices.
Transient performance has been validated by all tests to date on the ASIC.

II. GAS-2

The GAS-2 ASIC is presently under development. Objectives for this second ASIC are as follows:

1.) Reduce 1/f noise component in PMOS and NMOS current sources.
2.) Add a 1X, 5X logic level selectable Gain stage to accommodate lower gain cathode strip readout.
3.) Add a selectable timing comparator. Minimum Sensitivity 2fC.

A channel block diagram is shown below. Note that additional detail concerning the GAS – 2 ASIC is available as a support document. See "GAS_ASIC_Status.pdf"



igure 2 GAS-2 Channel Blocks **F**

The 1X - 5X gain Stage - The charge induced on the cathode pad readouts is about 5X smaller than at the wire (anode). In order to minimize noise pickup in the signal transfer between the GAS ASIC and shaper it was decided to increase the gain in the front end readout. To preserve the shaping, achieve the higher gain and retain a wide dynamic range, we chose to use a current mirror transfer between two stages at a cost of about 3mW. See Appendix E for the circuit schematic.

Limiter and Timing Comparator - The 2304 wire anodes of the CTC will bused for tracking. The closest point of approach of ionizing tracks will be determined by using the time of arrival of the avalanche signal from the first track primaries at the wire. Position information will be inferred using the positive ion velocity.

The GAS – 2 chip will have a switch selectable comparator that outputs a current pulse to the line driver output suitable for low level logic switching. DC offsets accumulated in the preamp and shaper stages will be eliminated using capacitive coupling. A 10pF series coupling capacitor and 3k resistor to Vdd/2 (1.25V) on each line will provide a 30ns time constant and turn the unipolar shaper stage output into a bipolar shape with an amplitude loss of ~25%. To prevent a long dead time for large signals the capacitive coupling will be preceded by a limiter stage that will provide some additional gain and limit the linear signal size to about 15fC, (30-50 mV). The comparator is a two stage design with a non linear impedance formed by a crossed transistor mirror pair load to provide DC hysteresis.

The first stage input transistors and resistor bias network to set the voltage of the capacitively coupled inputs are arranged to minimize offsets due to process variations to about 2mV. Capacitively coupled positive feedback from the output to the input stage cascode transistors provides sufficient charge when the output

triggers to maintain a stable comparator output for ~10ns. The basic schematic of limiter and comparator stages are shown in Appendix F.
The output transient response is shown in Figure 3 for a ¼ fC step ramp in the SPICE simulation of the limiter/comparator circuit with a 1.5fC threshold setting is shown in the figure below. The width of the signal is seen to be nearly constant even for at threshold signals.

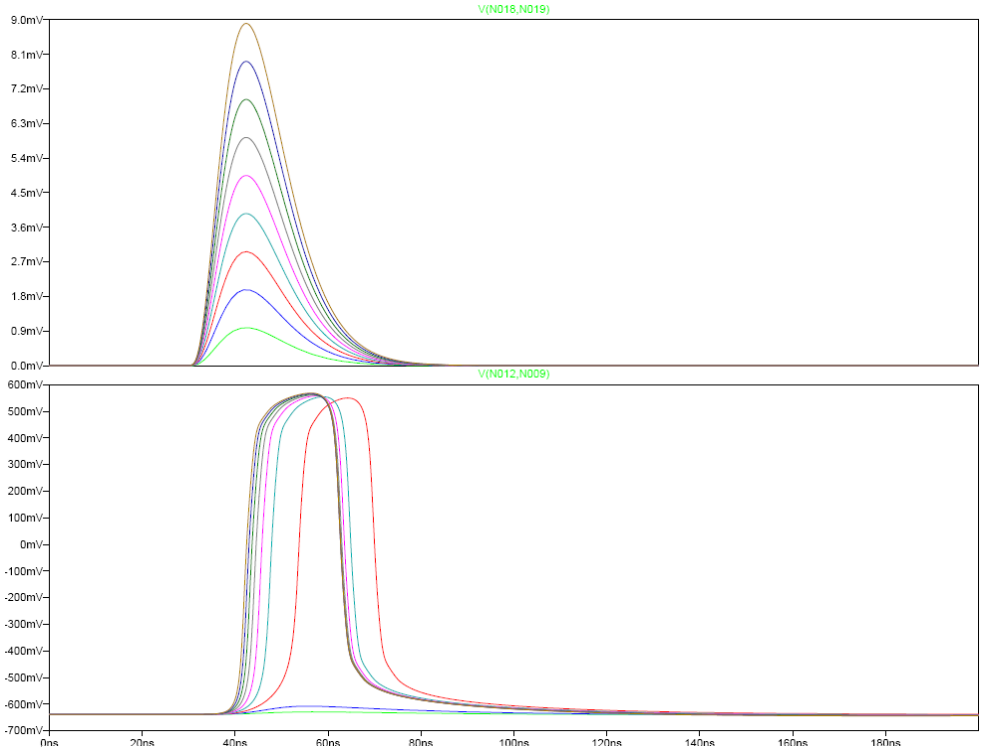


Figure 3 The transient response of the limiter and comparator circuit.

Gas – 2 Status and Work Plan –

What is Done:

1. The current mirrors for the amplifier and shaper have been redesigned to reduce 1/f noise sensitivity.
2. Most of the NMOS transistors have been placed in Deep N wells so that bulk modulation effects can be minimized by connection of the bulk and source.
3. The layout of the 1x, 5X gain stage layout is complete. We have a nearly complete, layout to schematic verification of the single channel layout.
4. Initial design of the comparator section is underway. Schematic design is nearly complete with process variation checks underway.

What Remains:

1. Layout of the Limiter and Comparator section. This will involve stretching the length of the GAS-1 channel layout. (3-4 weeks)
2. Single channel Layout verification and simulations. (2 weeks)
3. Arraying the design and lengthening the ASIC foot print. (2 weeks)

4. Submit GAS – 2 ASIC (1-2 weeks till submission meets all requirements.)

This design will be submitted to MOSIS for fabrication in the TSMC .25um process. We expect to be ready for a May 5 submission. Should that be missed the next proposed submission date is June 30.
The fabricated ASICS will be packaged by MOSIS and characterized in bench tests at Penn and JLAB. Once performance qualified packaged parts should be available for on detector testing. The choice to immediately proceed to a full production run will depend on the success of the design.
We expect that all processing, including production will be through the MOSIS service. Testing and characterization of final production parts is planned to be done at the Penn IMS automated ASIC test facility.

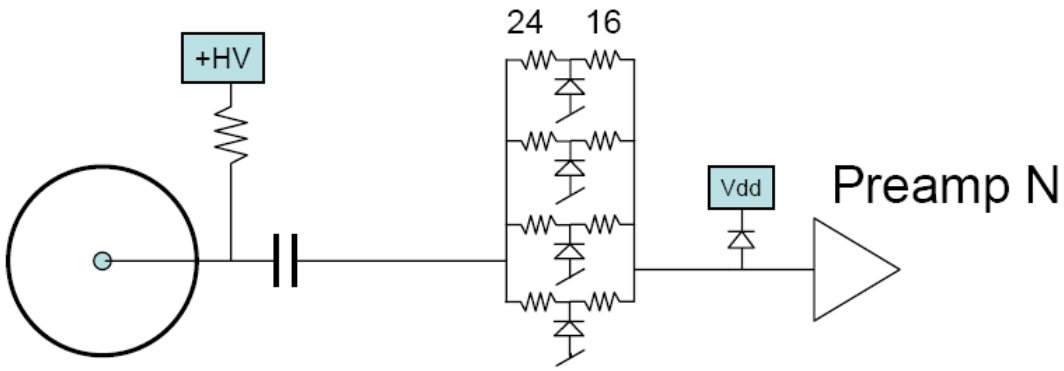
References:

1. Bokhari, W.M., Heinrich, J.G., Lockyer, N.S., Newcomer, F.M.,
Nucl. Sci, 1998. Conference Record. 1998 IEEE
V1, pg. 445-446
2. B. Bevensee, F.M. Newcomer, R.P. Van Berg, H.H. Williams, IEEE
Trans. Nucl. Sci. NS-43 (1996) 1725.

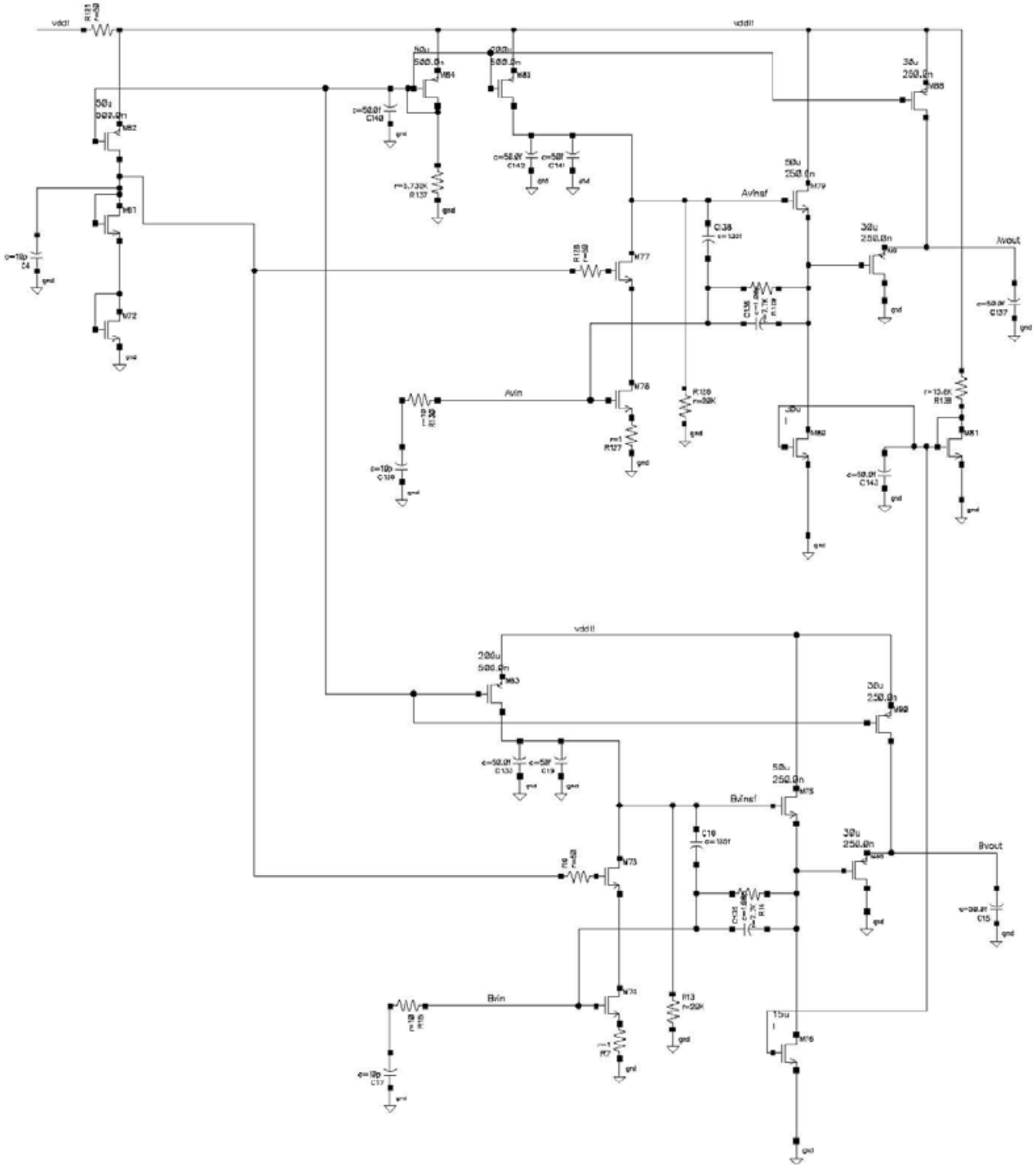
Note Many additional references are available for both ASDQ and the ASDBLR ASICS, through Google.

Appendix A

GAS-1 Negative input protection schematic for Anode input shown with expected straw tube attachment through a series HV blocking capacitor on the left. Additional protection will be provided by a board level diode on each channel Positive input protection (wired with opposite polarity) is provided on the P input with 30% of the N input diode area.

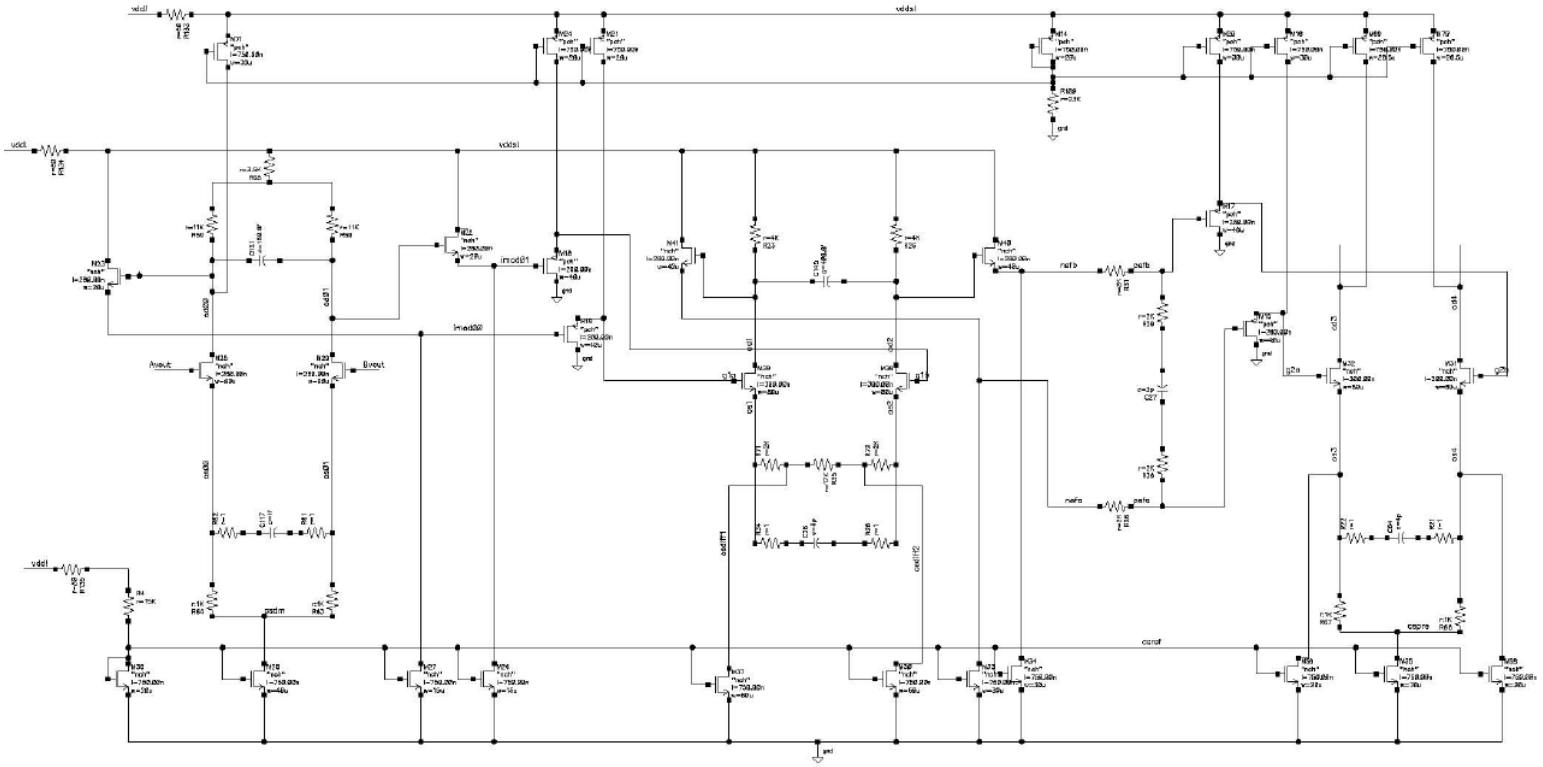


Appendix B Dual Preamp Schematic



Note that capacitive parasitics are included on important nodes.

Appendix C Shaper Schematic



FIRST STAGE:

GAIN & BIAS

SECOND STAGE:

TAIL CANCELLATION

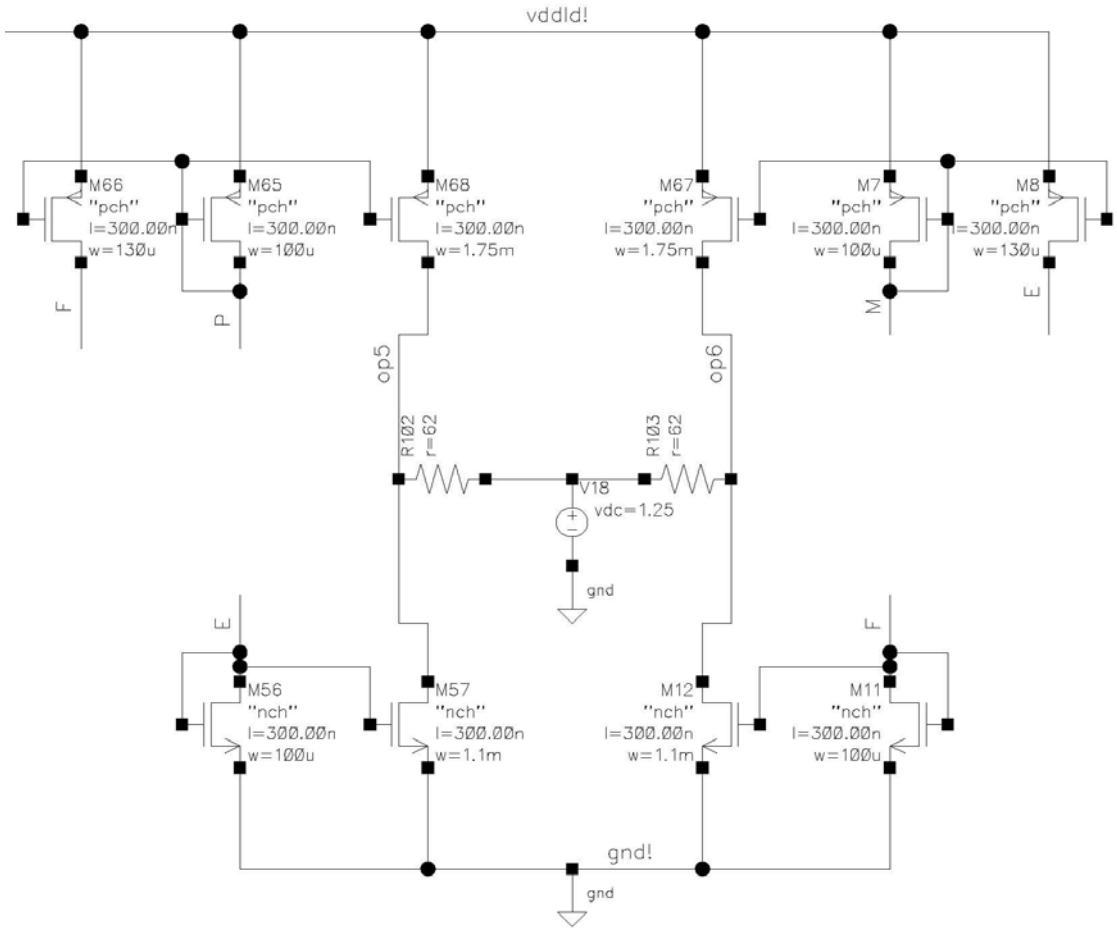
DOMINANT DIFFERENTIATOR

DOMINANT INTEGRATOR

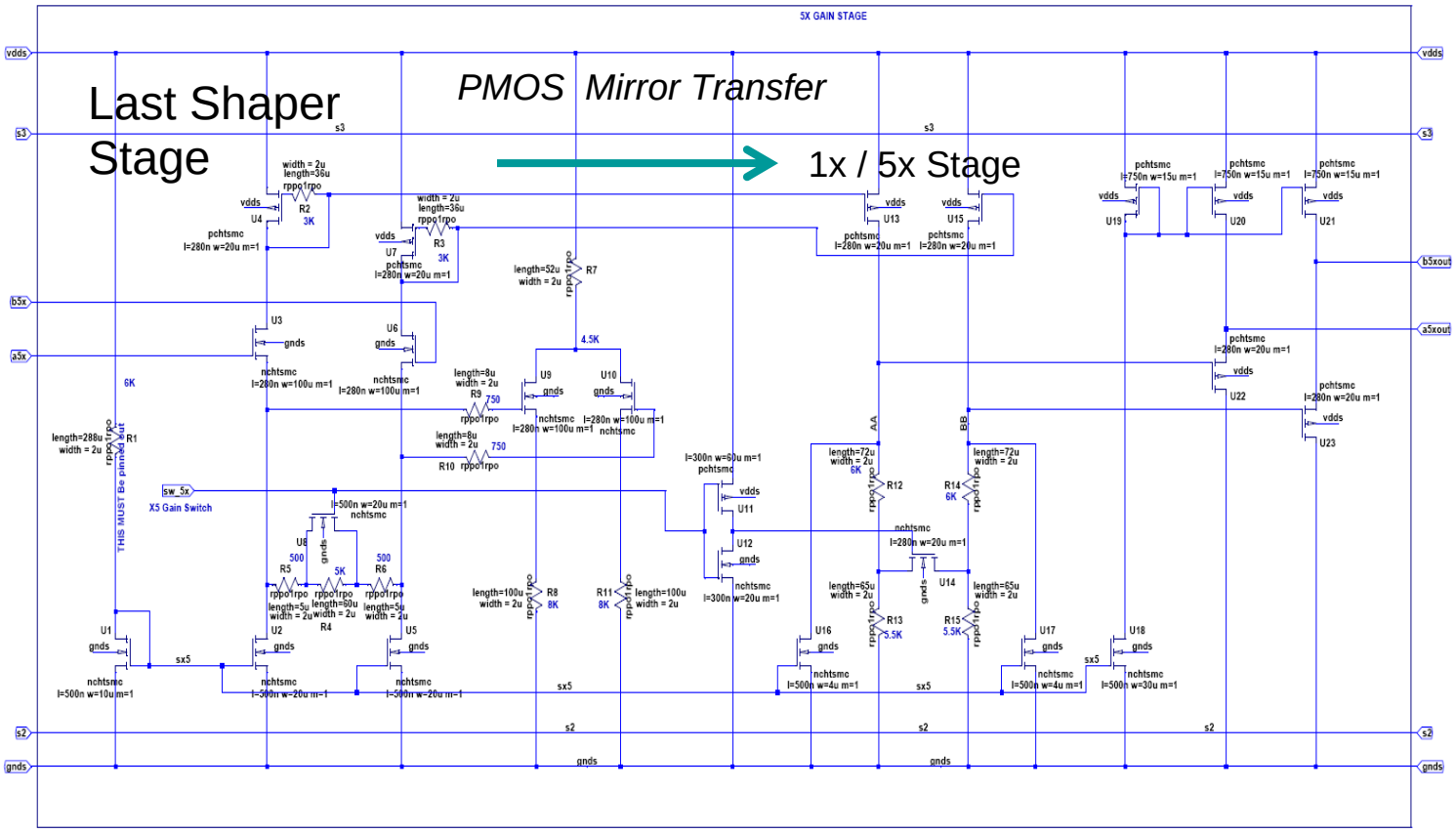
FINAL STAGE:

PREAMP TAIL CANCELLATION

Appendix D Line Driver Schematic

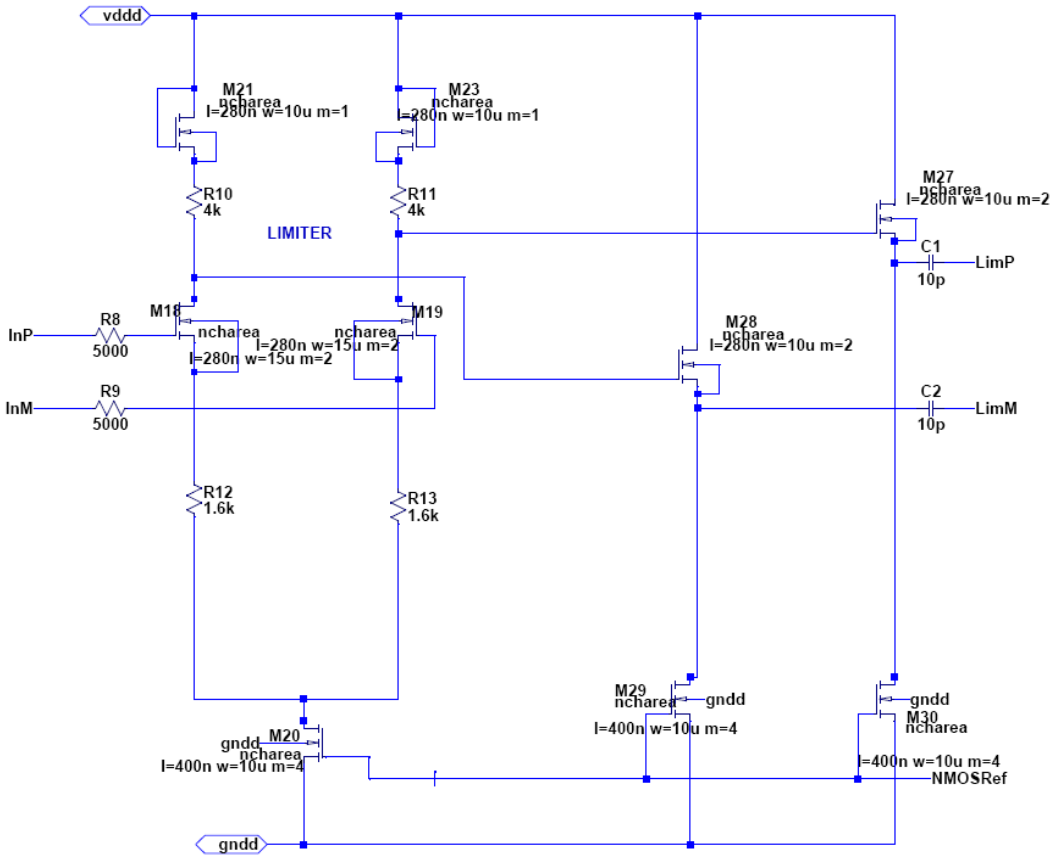


Appendix E GAS-2 Gain Select stage: 1X, 5X



Appendix F GAS – 2 Limiter and Shaper Schematics

Limiter Circuit



Appendix F GAS – 2 Comparator Circuit