A VME64x, 16-Channel, Pipelined, 250 MSPS Flash ADC With Switched Serial (VXS) Extension

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I. Introduction

We have designed a 250 MSPS pipelined flash ADC (Analog-to-Digital Converter) which will be employed at the Jefferson Lab's four experimental physics halls and will support 8-, 10- or 12-bit resolution. This high speed and high density flash ADC conforms to VITA-41 VME64x switched serial (VXS) standard.

The trigger information output from each of the modules on a VXS crate is routed via the backplane to a switch slot. A total of 18 flash ADCs per crate feed serial data to the switch slot at an aggregate rate of 6 Gb/s which is then sent to the experiment global VXS trigger crate.

II. VME64x with VXS

The Switched Serial Extension (VXS) backplane is a redundant Star configuration, figure 1.

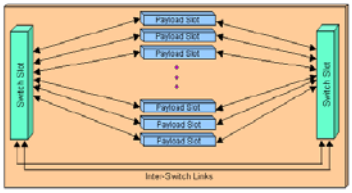

Figure 1 – VXS Redundant Star Configuration

III. Module Architecture

Figure 2 shows a simplified block diagram for one of the channels of the JLab 250 MSPS flash ADC (aka, fADC-250).

The topology of the fADC-250 module and its photograph are shown in figures 3 and 4, respectively.

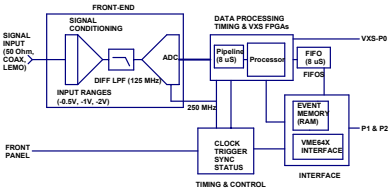

Figure 2 – Simplified Block Diagram (One Channel)

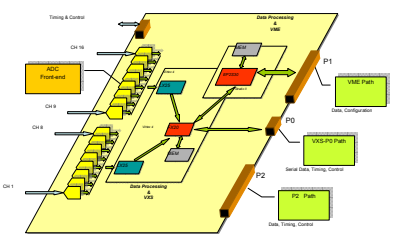

Figure 3 – Topology of the fADC-250

IV. Results

The front-end response of the ADC was characterized for bandwidth (110 MHz) and signal response, as shown in figure 5. The top scope traces show the differential input to the ADC; the bottom trace is the math sum of the differential signals.

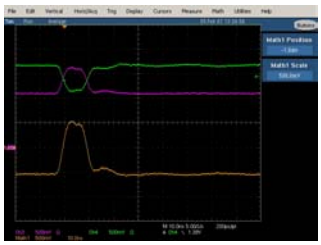

Figure 5 – Front-end Pulse Response

Figures 6 shows the resolution measured on a 10-bit module.

We obtained nominal resolutions of 0.59 LSB (ENOB = 10-bits) and 1.43 LSB (ENOB =11.48 bits) for the 10- and 12-bit ADCs, respectively

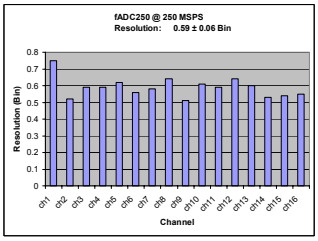

Figure 6 – Front-end Pulse Response

Figure 4 – Photograph of the fADC-250

Figures 7 and 8 show a ramp and fast pulses waveforms respectively.

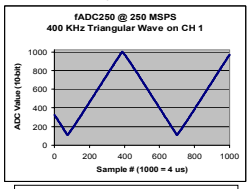

Figure 7 – Ramp on 10-bit ADC

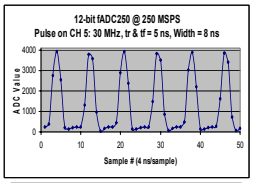

Figure 8 – Pulses on 12-bit ADC

Figure 9 shows that the cross-talk from channel 8 into channel 9 on a 12-bit module is negligible and within the background noise of +4/-5 bins (σ = 1.55 bins) determined from a pedestal run.

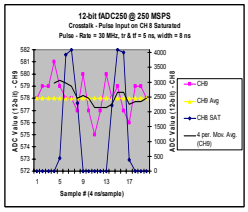

Figure 9 – Cross - talk

V. Conclusion

We have designed a 16-channel, pipelined flash ADC that can support applications requiring 8-, 10- and 12-bit ADCs and operating at 250 MSPS.Our tests indicate that we are meeting our specification goals, shown below in figure 10.

Besides measuring the integrity of the front-end design through our tests, we have also verified data processing algorithms for sparcification and windowing. Additionally, energy sum outputs through the VXS backplane have also been verified.

We plan to fully test our design and qualify these flash ADCs for production within the next year.

VI. Acknowledgements

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fADC-250 Specifications
VME64x with VXS, Pipelined 250 MSPS Flash ADC Module

Signal Inputs	Number	16 S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable
	Offset	±10% FS per channel via DACs
Clock	Sampling	250 MSPS, Differential
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)
	Source	Internal and External
Control Inputs/Outputs	Clock	N – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger	SW Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)
	INL	± 0.8 LSB
	DNL	± 0.5 LSB
	SNR	56.8 dB @ 100 MHz Input
	Data Latency	32 nS
Trigger Latency	8 µS	
Data Memory	8 µS	
Data Processing	Sparcification Windowing Charge, Pedestal, Peak, Energy Sum on VXS for Trigger Time (Over Threshold, Relative to trigger) Output (Backplane, VXS)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0	
Packaging	6U VME64x	
Power	+3.3V, +5V, +12V, -12V	

Figure 10 – Specifications of fADC-250