GlueX Collaboration Meeting

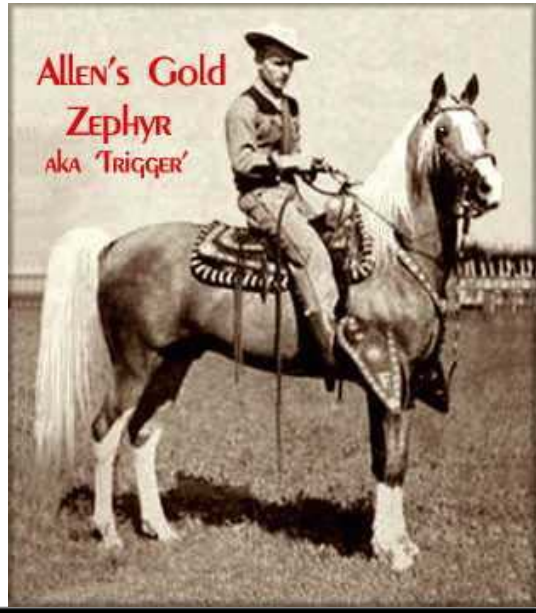
12GeV Trigger Electronics

9 September 2009

R. Chris Cuevas

1. Trigger Workshop Summary
   - New requirements
2. Hardware status
   - Module description review
   - Test results
3. FY10 Goals

Every new system needs a cool ‘icon’



Trigger Workshop Summary

- 2nd annual 12GeV trigger workshop held on July 8th, 2009 at Christopher Newport University.

- Good attendance and folks from all four experimental halls were represented.

- Four sessions included:
  Trigger module descriptions - C. Cuevas
  DAQ System – D. Abbott, E. Jastrzembski
  Global Trigger requirements – A. Somov
  On-line and run control – E. Wolin

Hall D Requirement Review

- 200kHz average L1 Trigger Rate, Dead-timeless, Pipelined, 2ns bunch crossing (CW Beam)
- Level 1 trigger system supports streaming subsystem hit patterns and energy summing with low threshold suppression
- Scalable trigger distribution scheme (GlueX: ~30 L1 crates, ~50 total readout crates)
- Low cost front-end & trigger electronics solution
- Reconfigurable firmware – Provides different programmable features required by other halls. (CLAS12 calorimeter for example)

New Trigger Requirements From Trigger Workshop

- Summary

1. Use the two trigger signals, Trig1 and Trig2 to change the mode of the flash board readout. Presently the readout mode is selected when the User programs the module before starting a 'run'. Presently the mode does not change during a 'run'. Using the two Trigger bits, the trigger supervisor can issue a specific readout mode for a given trigger event type. (e.g. Change mode to initiate a scaler readout event)

2. Dedicate a VXS differential pair from the TI to CTP and from the TI to the SD. Keep the I^2C link, but a differential pair will be needed to transfer data from the two switch cards at a higher rate than the I^2C allows. (The dedicated pair is not required to be a gigabit serial link.)

3. Add input/output signaling capabilities to the CTP and TI front panels. The number and type of signaling levels were not defined, but I/O signals will be required and allow for a number of useful features

4. Global Trigger -- Implement multiple trigger partitioning "sessions". Ed and David A. outlined a simple idea for up to 4 concurrent trigger sessions using CODA3.

5. Global Trigger – The Trigger Supervisor will need to manage external signals for calibration systems. Presently the TS is specified to connect directly to the Global Trigger Processor(s) and the additional inputs/outputs to pulsers or other hardware will need to be managed.

Module Definitions From CD3 Review

- ***Decision to use VXS (VITA 41) high speed serial backplanes***
- **F**lash **ADC** 250Msps (**FADC250**)
  - ✓ This is where the trigger 'data' begins

- **C**rate **T**rigger **P**rocessor (**CTP**)
  - ✓ Collects trigger data (SUM) from 16 FADC250 modules within one crate
  - ✓ Transports trigger data over fiber to Global Trigger crate
    - 10Gbps capability (8Gbps successfully tested)

- **S**ignal **D**istribution (**SD**)
  - ✓ Precision low jitter fanout of ADC clock, trigger and synch signals over VXS backplane to FADC250 modules

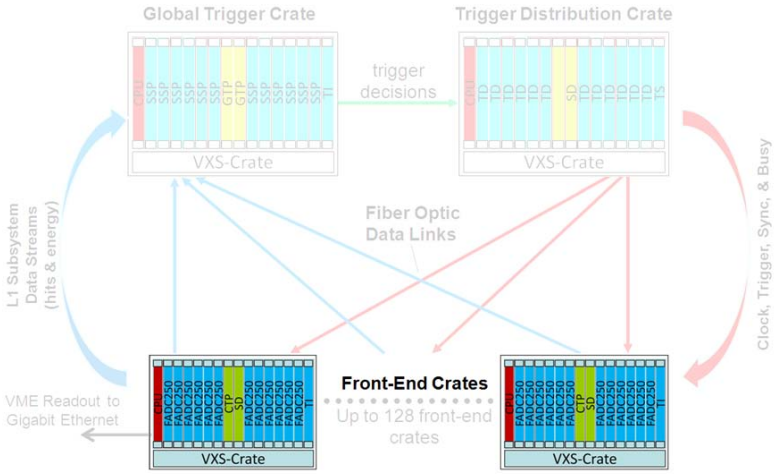
- **T**rigger **I**nterface (**TI**)
  - ✓ Direct link to Trigger Supervisor crate
  - ✓ Distributes precision clock, triggers, and sync to crate SD
  - ✓ Manages crate triggers and ReadOut Controller events

Module Definitions From CD3 Review

- **S**ub-**S**ystem **P**rocessor (**SSP**)
  - ✓ Direct fiber optic link to Crate Trigger Processor output
  - ✓ Supports up to 8 CTP modules
  - ✓ VITA 41 ‘Payload” format
- **G**lobal **T**rigger **P**rocessor (**GTP**)
  - ✓ Collects trigger data information from up to 16 SSP modules within the global trigger crate.
  - ✓ Trigger data from SSP modules is transported via VXS backplane
    - GTP modules are VITA 41 “Switch” format
    - Global Trigger equations are downloaded via VME or Ethernet
    - GTP Output wired to Trigger Supervisor
- **T**rigger **D**istribution (**TD**)
  - ✓ Precision low jitter fanout of ADC clock, trigger and synch signals plus trigger ‘link’ information over fiber.
  - ✓ VITA 41 ‘Payload’ format supports up to 8 TI fiber links
- **T**rigger **S**upervisor (**TS**)
  - ✓ Direct link to Global Trigger Processor output
  - ✓ Distributes precision clock, triggers, and sync to TD modules
  - ✓ Manages system trigger configuration and Read-Out Controller(ROC) events
  - ✓ Handles multiple trigger ‘sessions’ and calibration trigger requirements

Front-End Electronics: FADC250

- 16 Channel 12bit, 250Msps Flash ADC
- 8μs raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- ***Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size***
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- VXS P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)
- 9 prototype modules assembled and in use for several years.
- Used in existing 6GeV program and Hall D detector tests:
  - Hall A BigBite
  - Upgraded Hall A Moller Polarimeter
  - FDC and FCAL



JLab-FADC250:

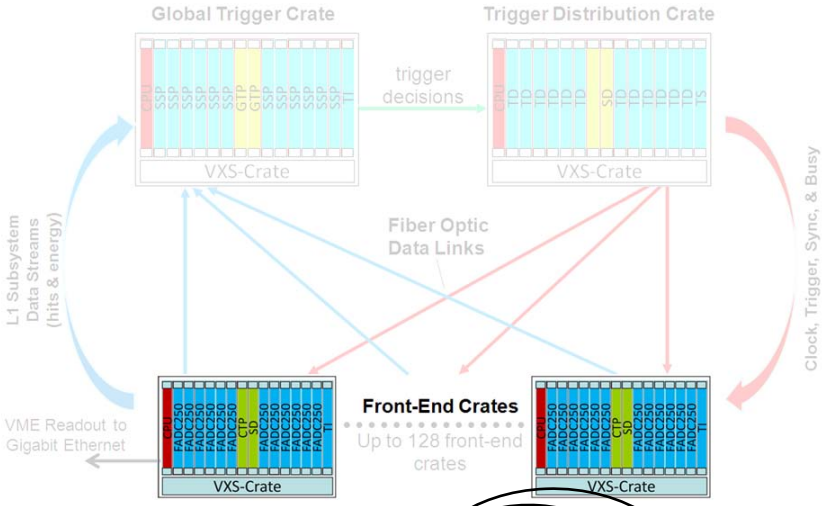
F. Barbosa
H. Dong
E. Jastrzembski
J. Wilson
C. Cuevas
B. Raydo

Crate Trigger Processor (CTP)

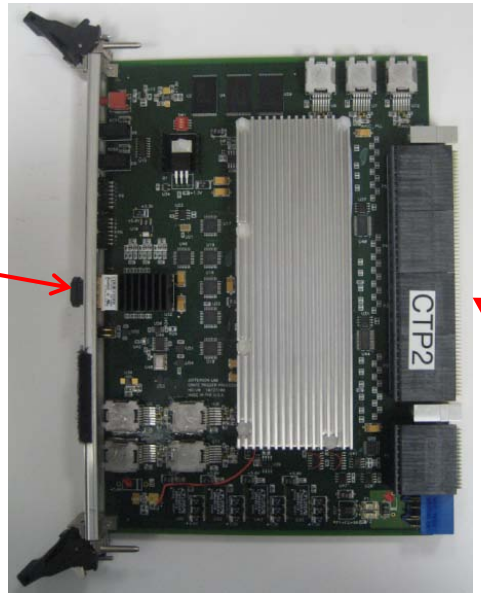
- Each FADC250 stream L1 board energy sum/hit to Crate Trigger Processor (CTP) residing in VXS switch slot A. Two modules assembled and tested.

- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)

- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



CTP Prototype:

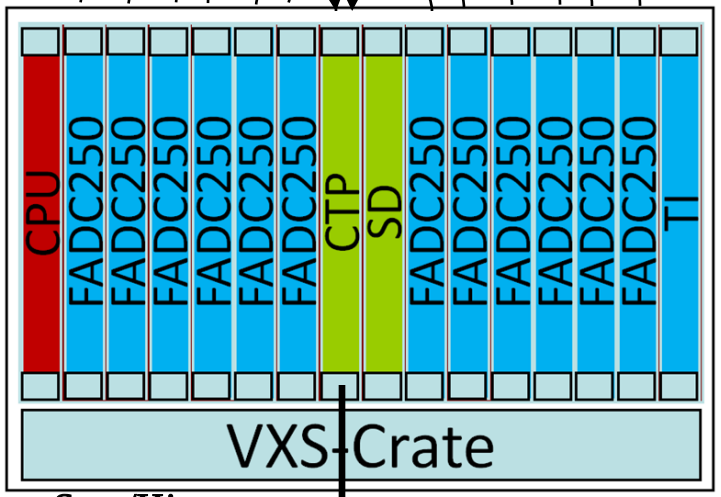


Fiber Optics Transceiver

VXS Switch Connector

H. Dong
J. Wilson

Board Energy/Hits 5Gbps to CTP



Crate Sum/Hits 10Gbps Fiber to Global Trigger Crate

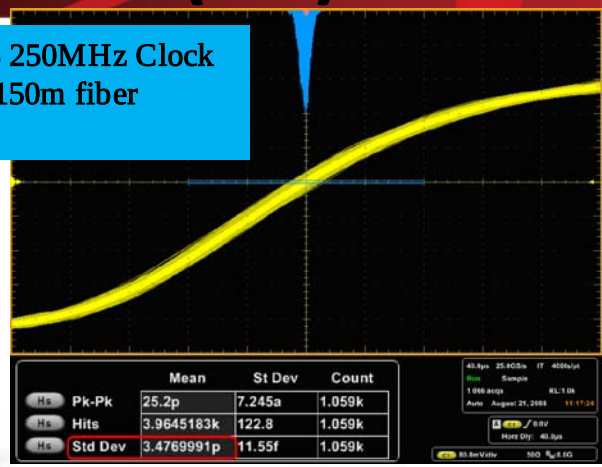
Crate Level – Signal Distribution (SD)

- VME64x backplane w/VXS (VITA 41 Standard) provides high speed serial connections from payload slots to switch slots (Dual Star)

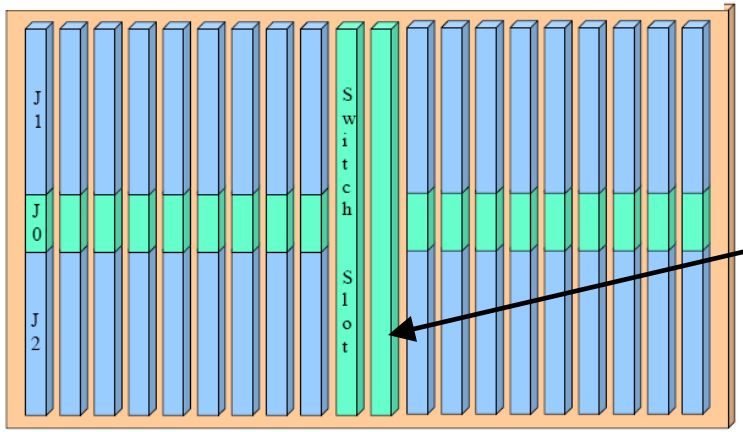
- Supports 18 Payload slots with precision clock, synchronization, and trigger signal distribution.

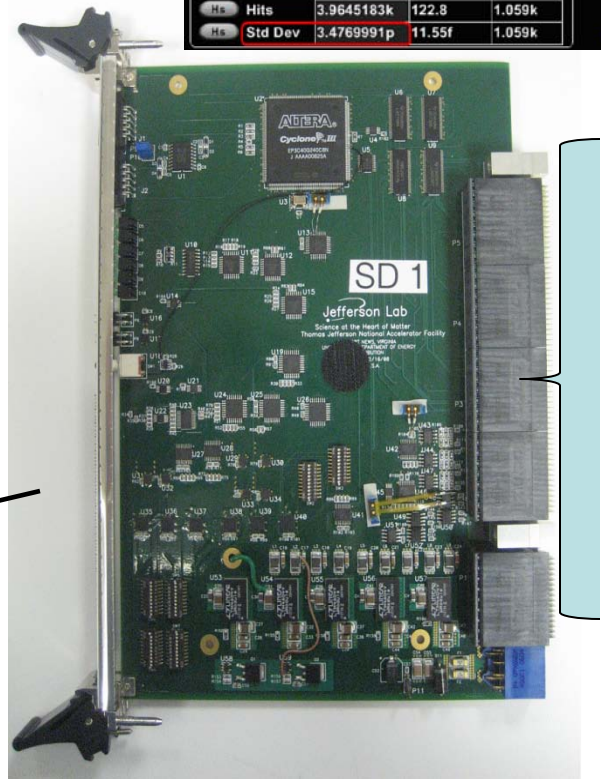
- Receives signals from TI and distributes common signals to each payload module (i.e. FADC250, FADC125, F1TDC)

3.47ps RMS 250MHz Clock Jitter after 150m fiber distribution



VXS (VITA 41 standard)
VME64x + high speed serial fabric on J0





VITA 41 Switch Slot Connectors

A. Gupta
M. Taylor
C. Cuevas

Trigger Interface (TI)

- VME64x payload board format
- Provides communication from VME to SD & CTP modules via I^2C serial links.

- Prototype module built with two fiber optic transceivers. Can be used in TD mode or TI mode.

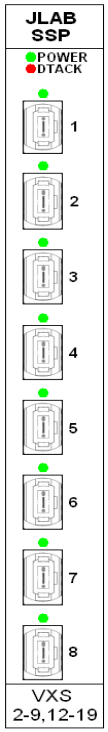
- Direct fiber optic link to Trigger Supervisor crate. Receives precision clock, synchronization, and trigger signals, plus trigger link status.

- Interfaces directly to crate SD module via the VXS backplane.

- Manages local trigger even buffers and interrupts to crate Read-Out Controller (ROC)

Sub-System Processor: (SSP)

Specification Sheet



MECHANICAL
- Single width VITA 41 Payload Module

HIGH SPEED SERIAL P0 INPUTS/OUTPUTS:
- 250MHz LVPECL Clock
- Trig 1, Trig 2, Sync Inputs
- 4x 2.5Gbps Lane SSP Subsystem Stream

Front Panel INPUTS/OUTPUTS:
- Multi-Fiber Optic transceiver
  - HFBR-7934
  - POP4 compliant 4 channel Rx/Tx fiber module
  - Up to 150meter fiber link (with 500Mhz-km fiber)
  - Up to 300meter fiber link (with 2000Mhz-km fiber)
- 2x LVPECL LEMO Outputs
- 2x LVPECL LEMO Inputs

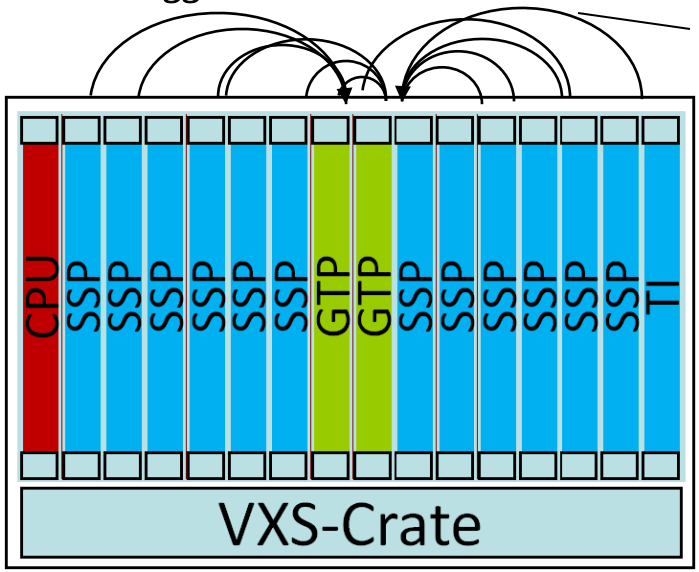
INDICATORS: (Front Panel)
- Power OK – Green LED
- VME DTACK – Red LED
- Link Status – Green LED

PROGRAMMING:
- On board JTAG Port

POWER REQUIREMENTS:
- +3.3v/+5v @ N Amps (From Backplane)
- Local regulators for other required voltages

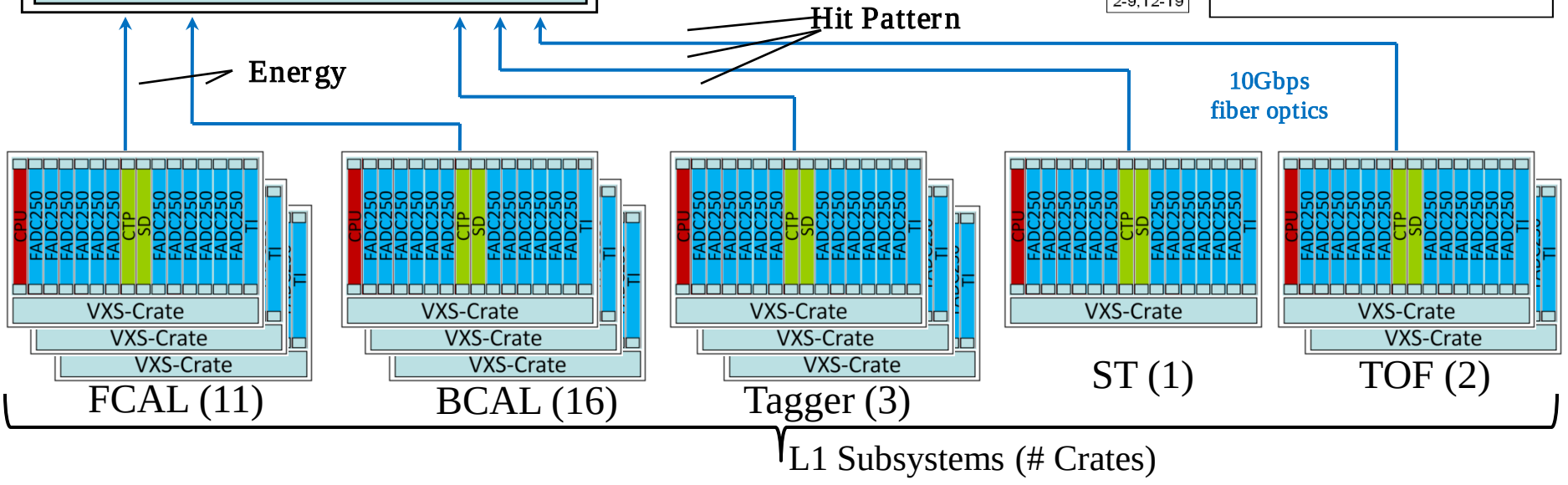
ENVIRONMENT:
- Forced air cooling: N CFM
- Commercial grade components (Celsius)

Global Trigger Crate:



Subsystem Energy Sum & Hit Pattern (10Gbps to GTP)

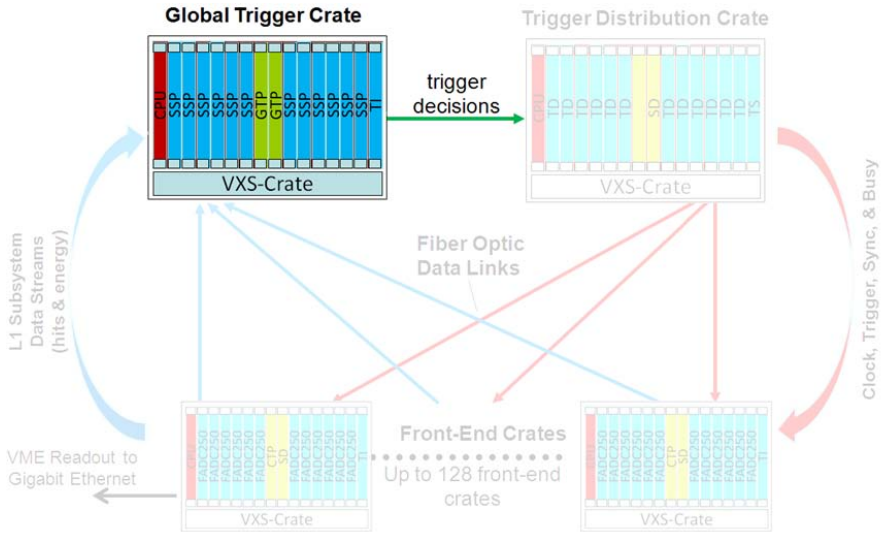
- Sub-System-Processor (SSP) consolidates multiple crate subsystems & report final subsystem quantity to Global-Trigger-Processor (GTP)
- 32bit quantity every 4ns

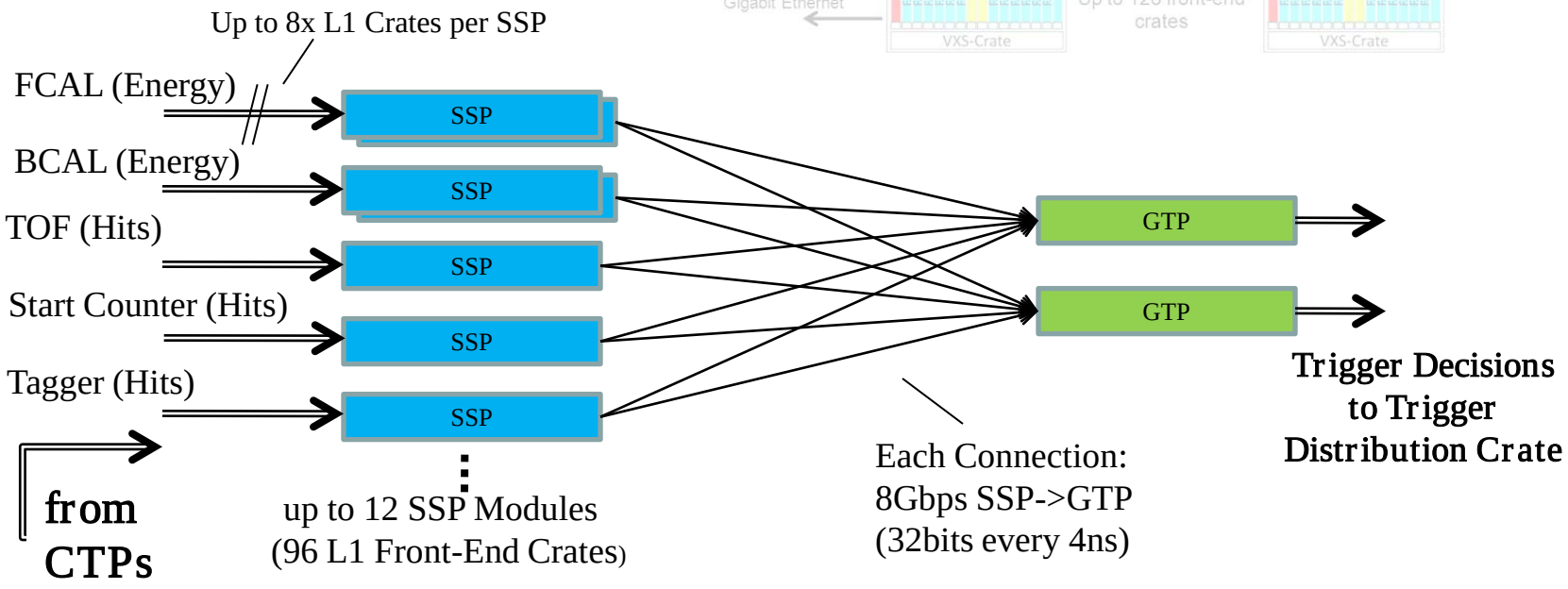


Global Trigger Processor: (GTP)

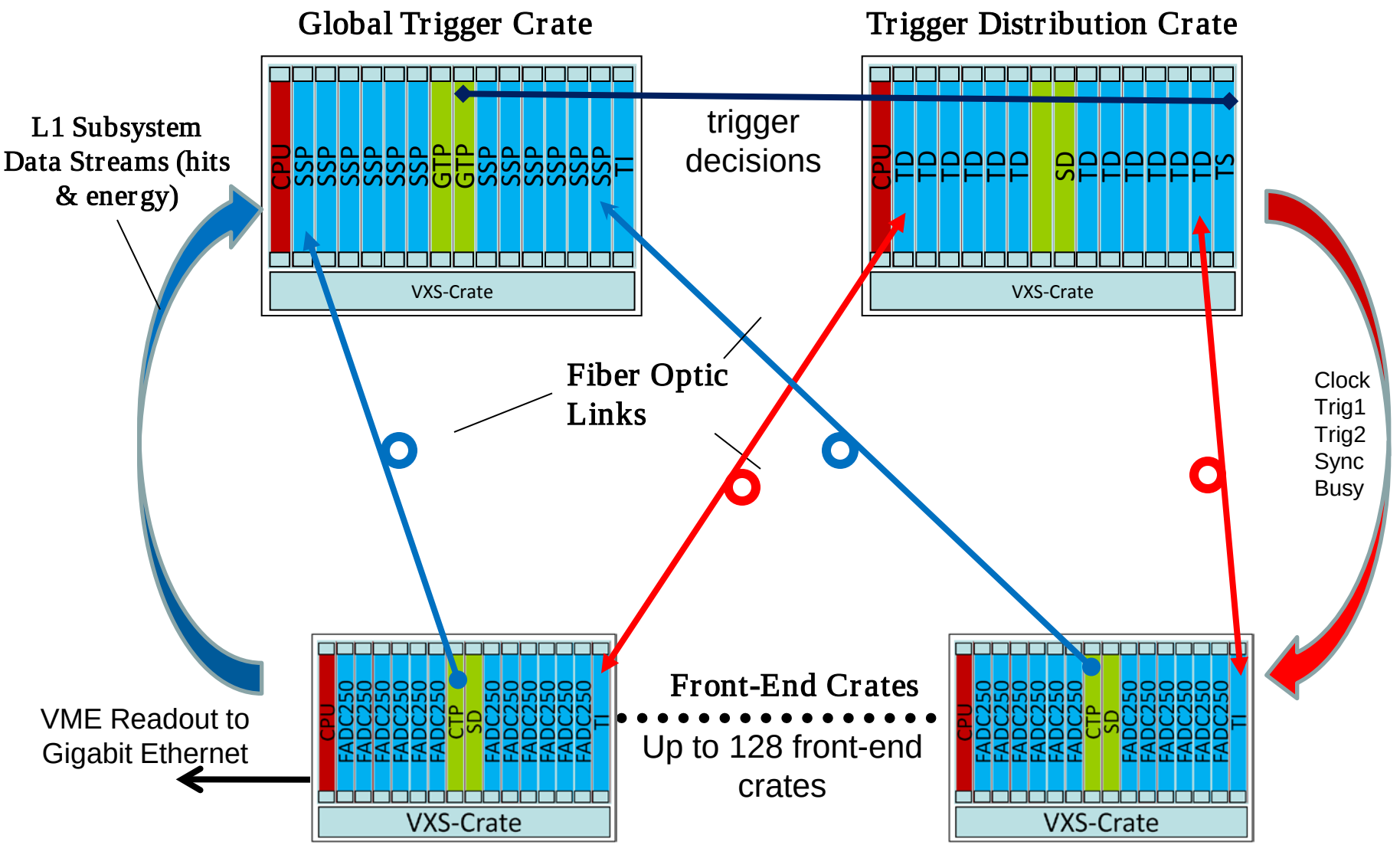
• Global Trigger Processor (GTP) receives all subsystem Level 1 data streams

• Trigger decisions made in GTP and distributed to all crates via the Trigger Distribution (TD) modules in the Trigger Supervisor Crate



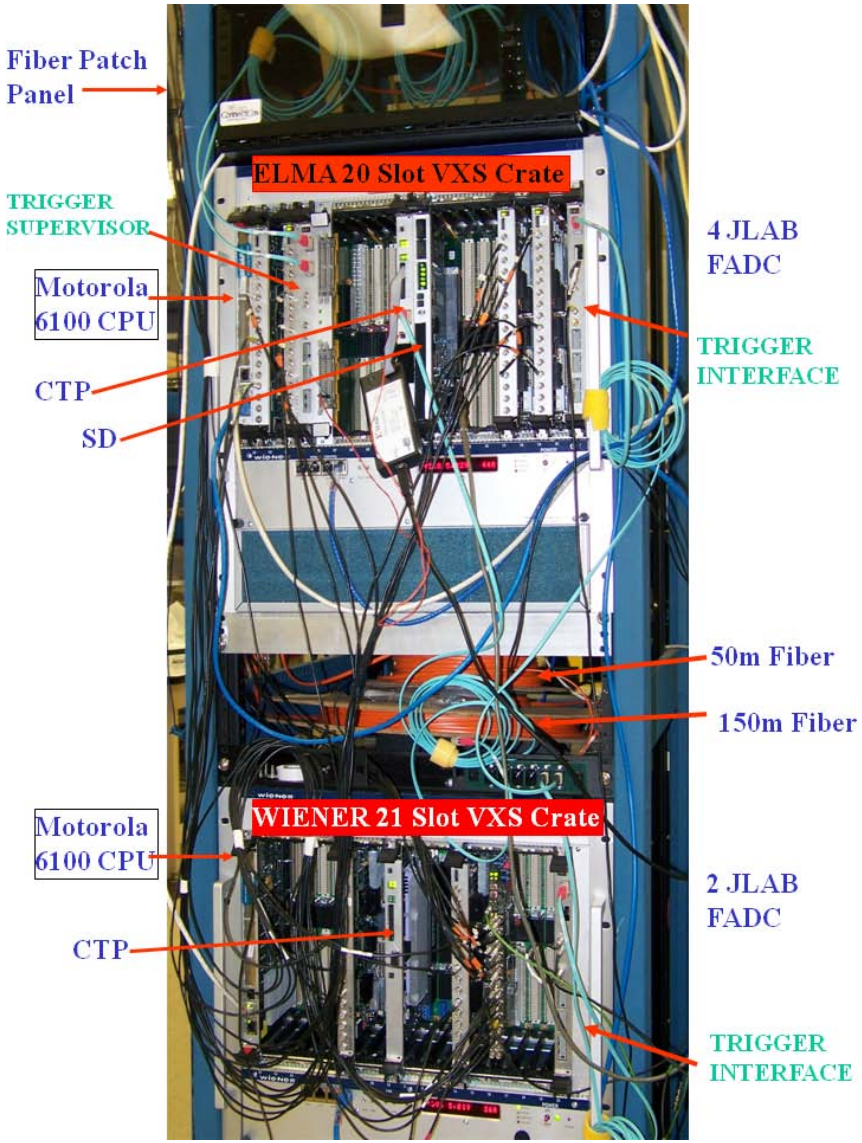


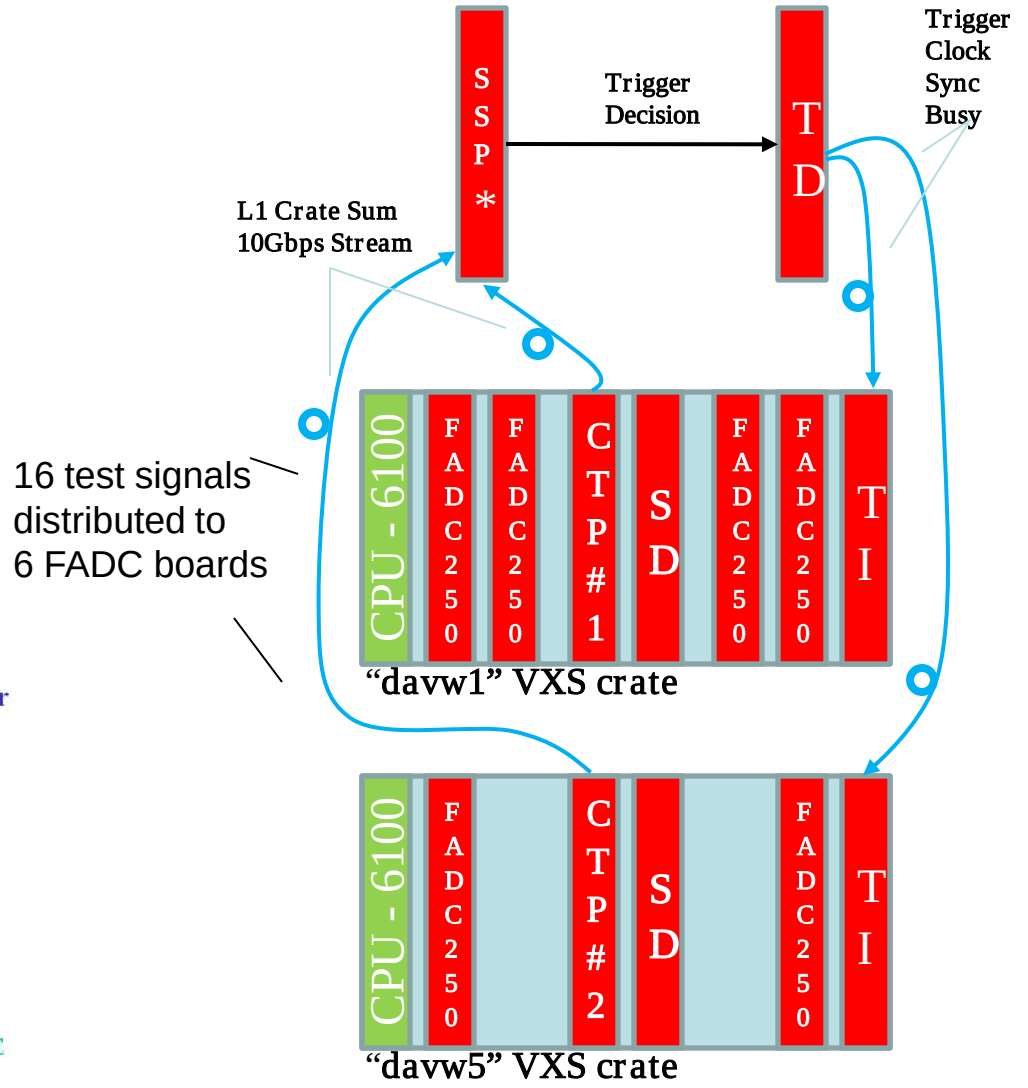
Level 1 & Trigger Distribution



Level 1 Hardware Test Results

2 Fully Prototyped Front-End Crates

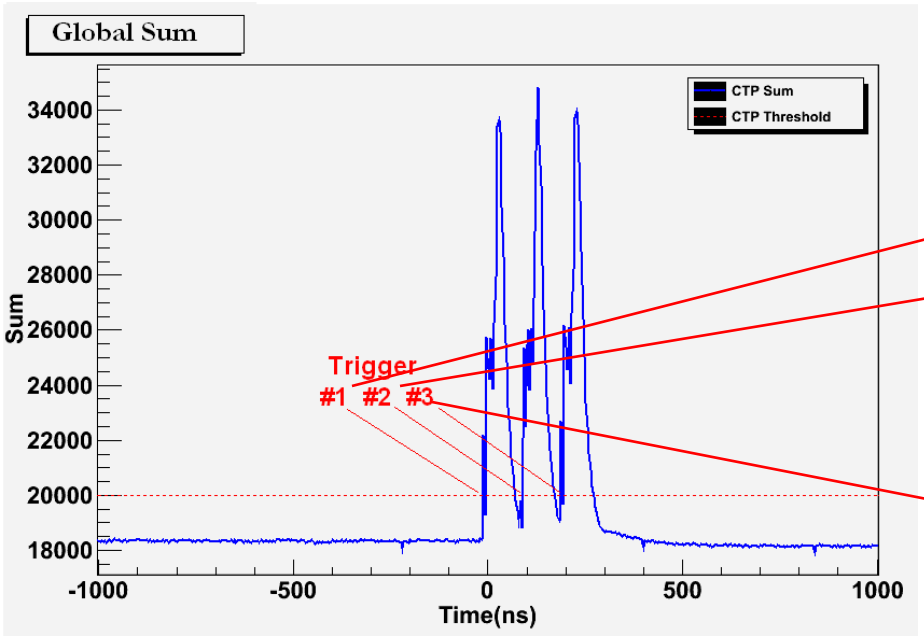




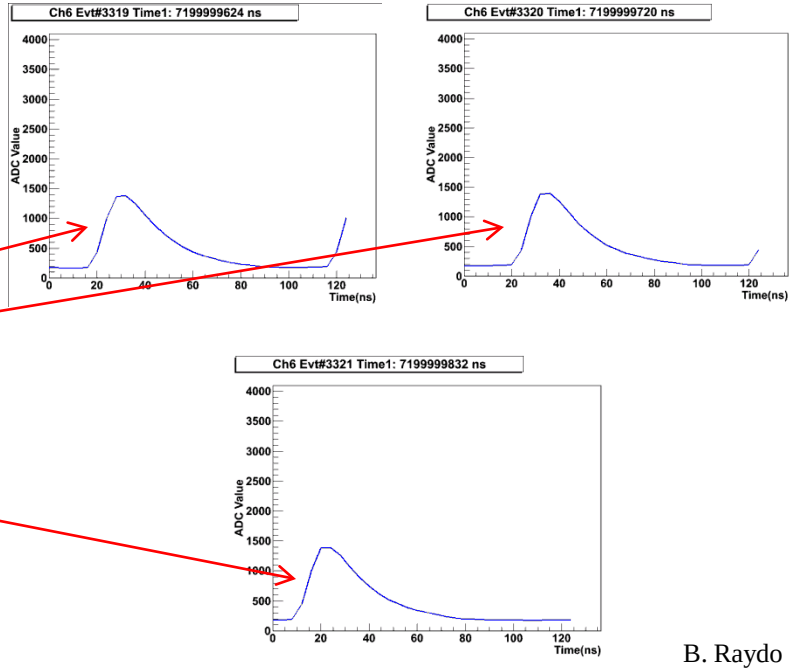
Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2μs global sum window is recorded around the trigger to see how the trigger was formed:



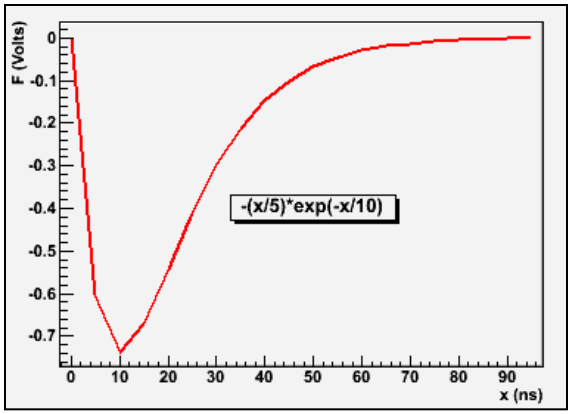
Example Raw Event Data for 1 FADC Channel:



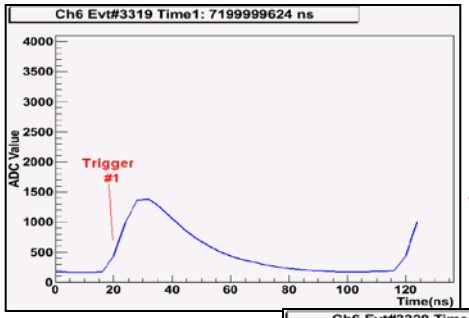
B. Raydo

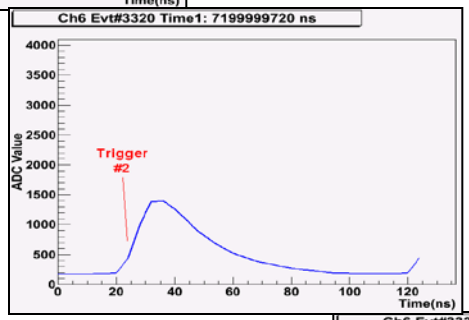
2 Crate Energy Sum Testing

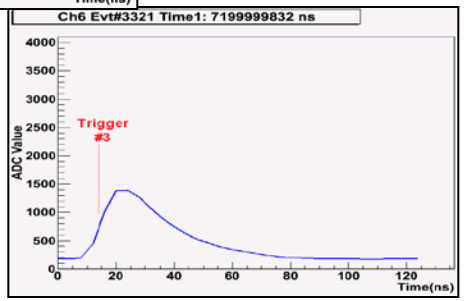
Input Signal to 16 FADC250 Channels:



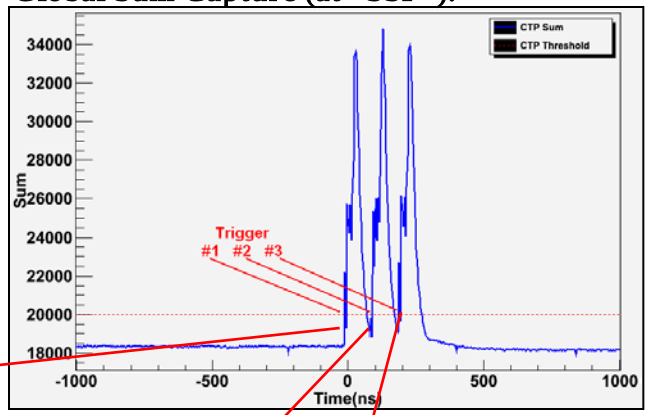
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- Threshold applied to global sum (96 digitized channels) produces 3 triggers.
- Raw channel samples extracted from pipeline shown for 1 channel.
- Runs at 250kHz in charge mode
- *Latency: 2.3μs(measured) + 660ns(GTP estimate) < 3μs*

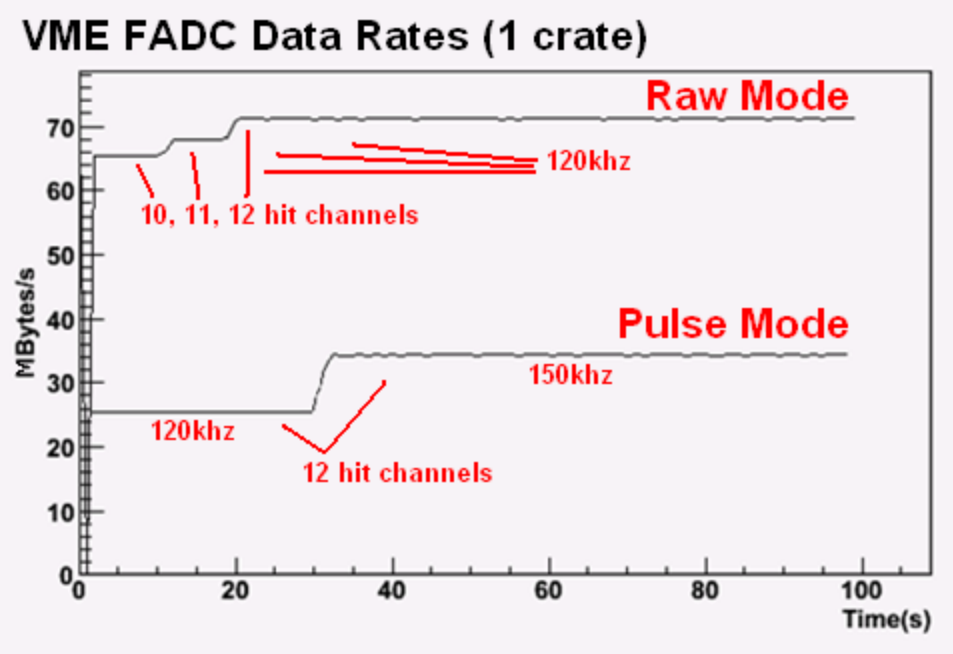
B. Raydo

Synchronized Multi-Crate Readout Rates

• FADC event synchronization has been stable for several billion events @ ~150kHz trigger rate.

• Have run up to 140kHz trigger rate in raw window mode, up to 170kHz in Pulse/Time mode.

• Ed Jastrzembski has completed the 2eSST VME Interface on FADC allowing ~200MB/s readout

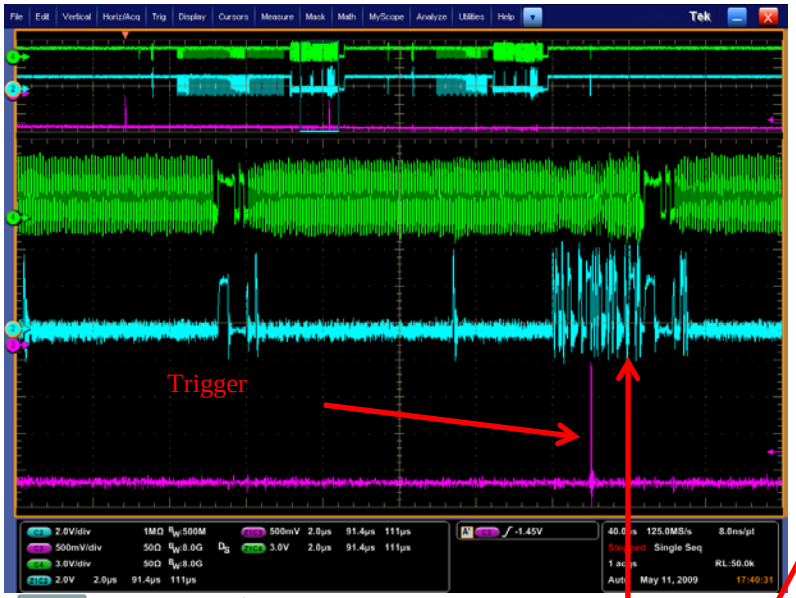


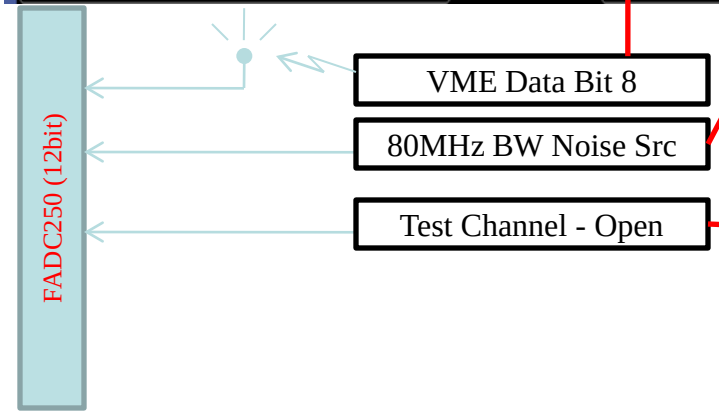
Single Crate
12 signals distributed to four FADC250

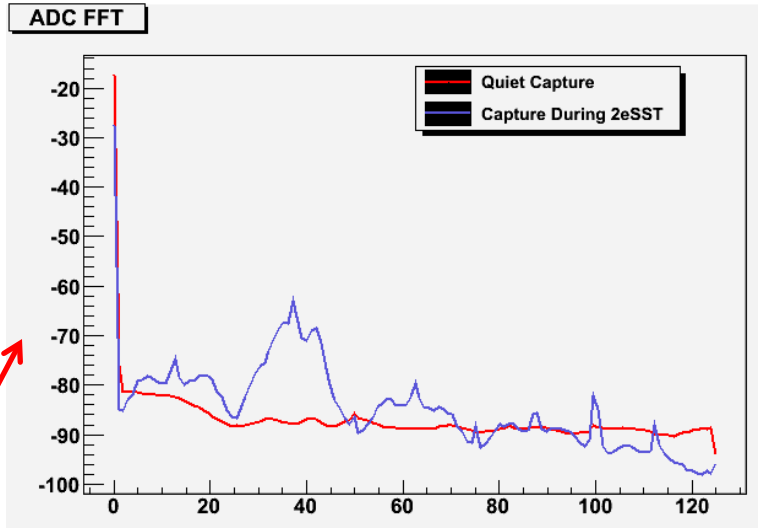
B. Raydo

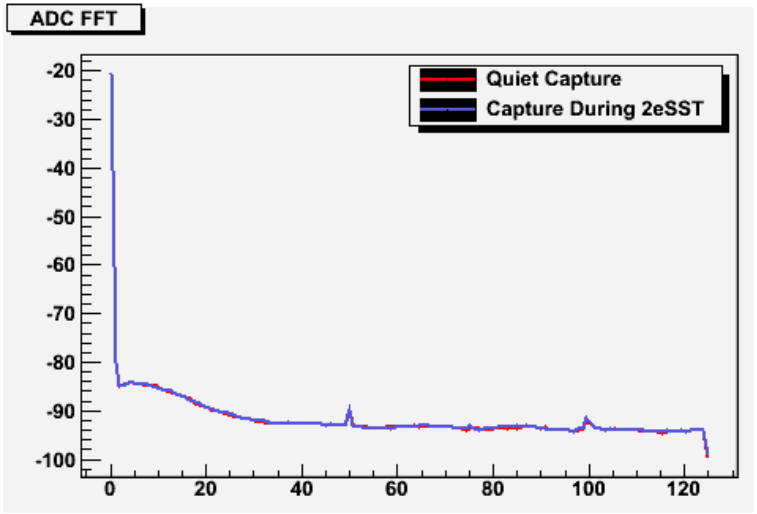
2eSST Backplane Noise Studies

• ~3,000 FADC 1µs windows FFT averages with and without a 2eSST VME transaction active during ADC capture shows almost no difference.









B. Raydo

FY10 Goals

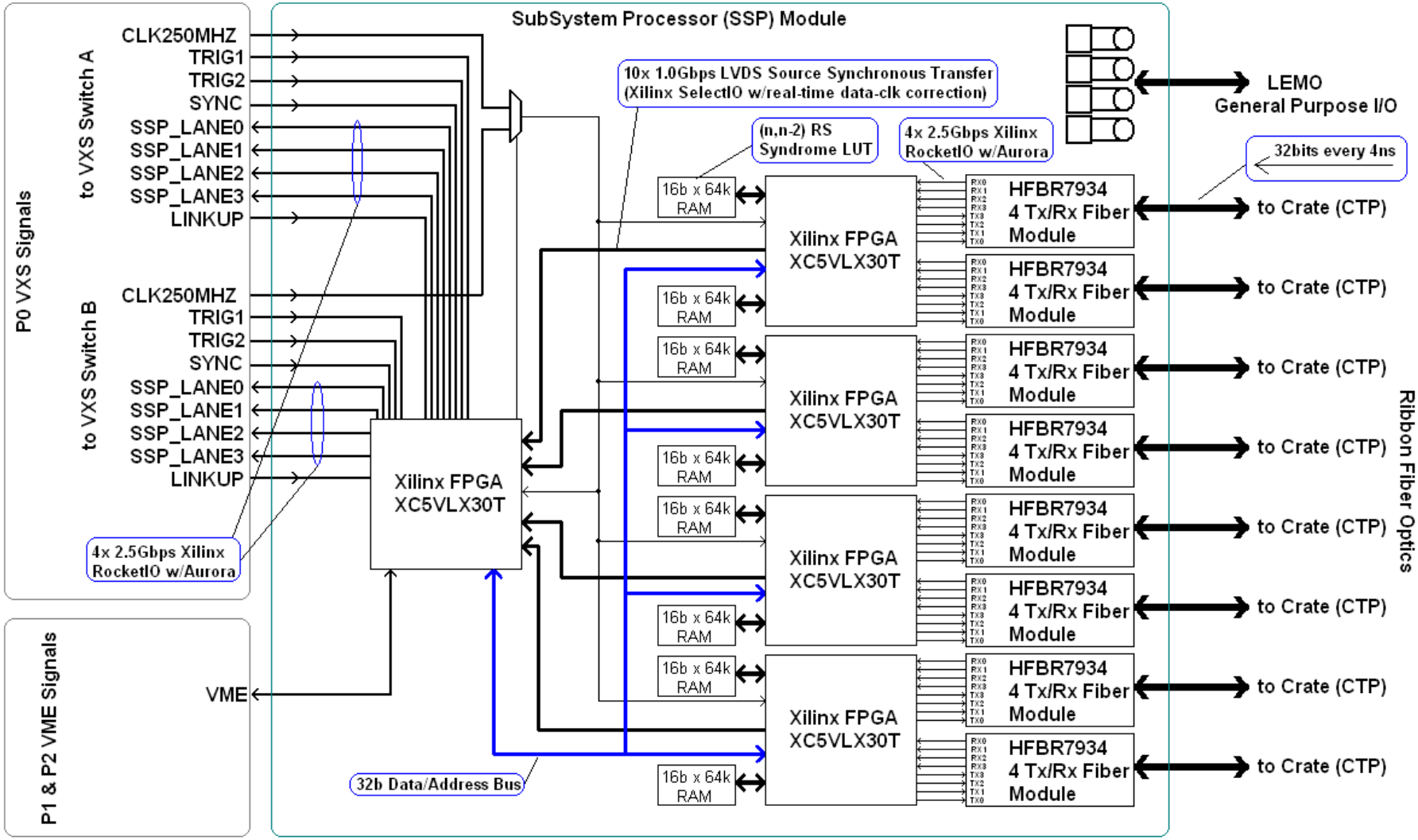
• **B**aseline **I**mprovement **A**ctivities (BIA) have been established for FY10 as funding source for design and development work required for the following board projects:

- FADC250 Rev-
  Revision includes 12bit ADC and consolidation of FPGA which will reduce part count significantly. Use latest Xilinx technology and include new requirements.
- F1-TDC Rev-2
  Revision includes 48 channel 'mode' for FDC, add VXS signaling, upgrade FPGA, add event RAM, and pulse output feature.
- SSP (Prototype)
  Complete schematic, board layout, assembly, and firmware for at least two units.
- GTP (Prototype)
  Complete schematic, board layout, assembly and firmware for a single unit.

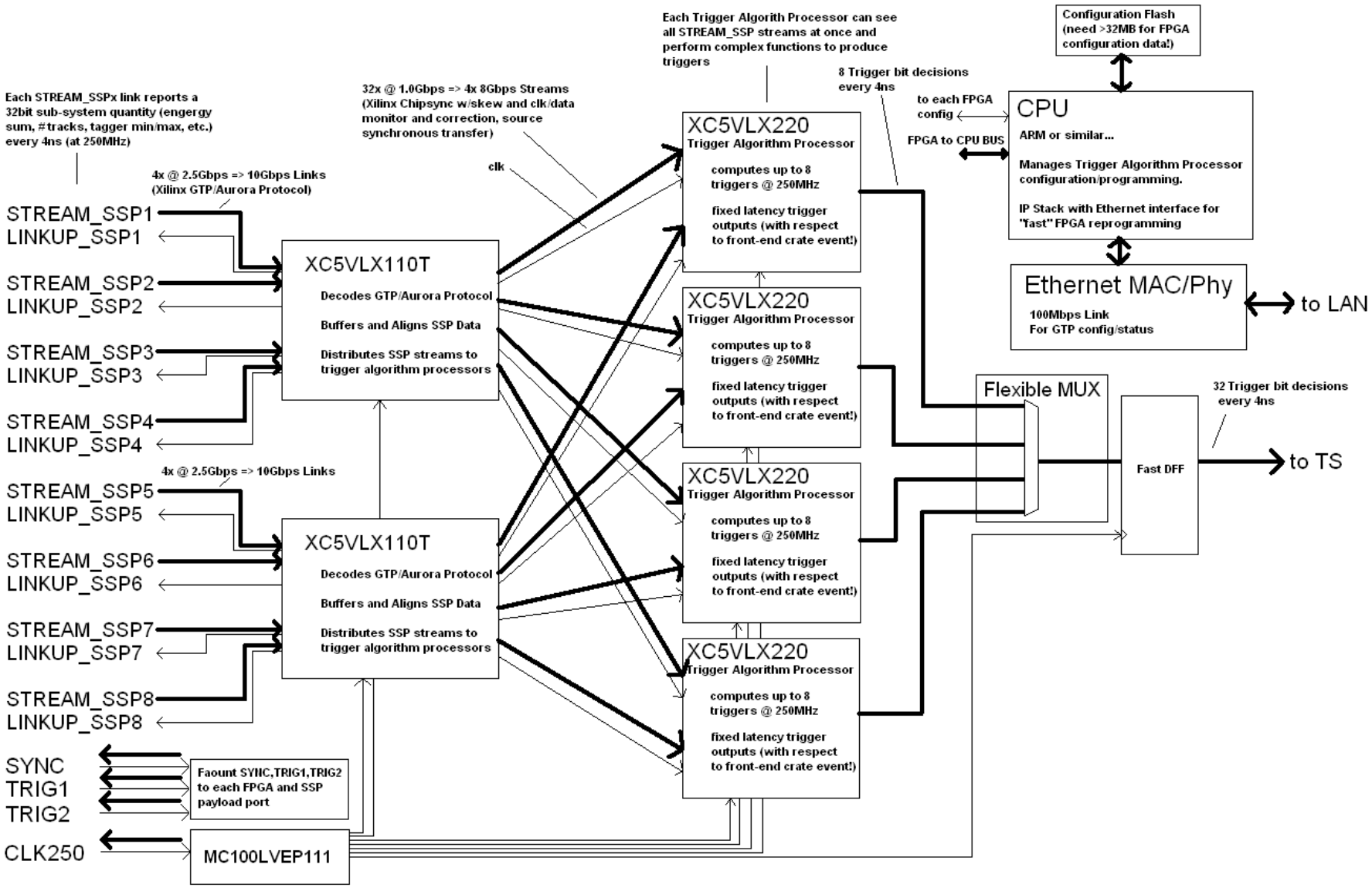
• Complete VXS crate specification and begin procurement for ALL VXS crates needed for 12GeV applications. Allows for quantity price reduction and 'phased' delivery during installation period.

Backup Slides

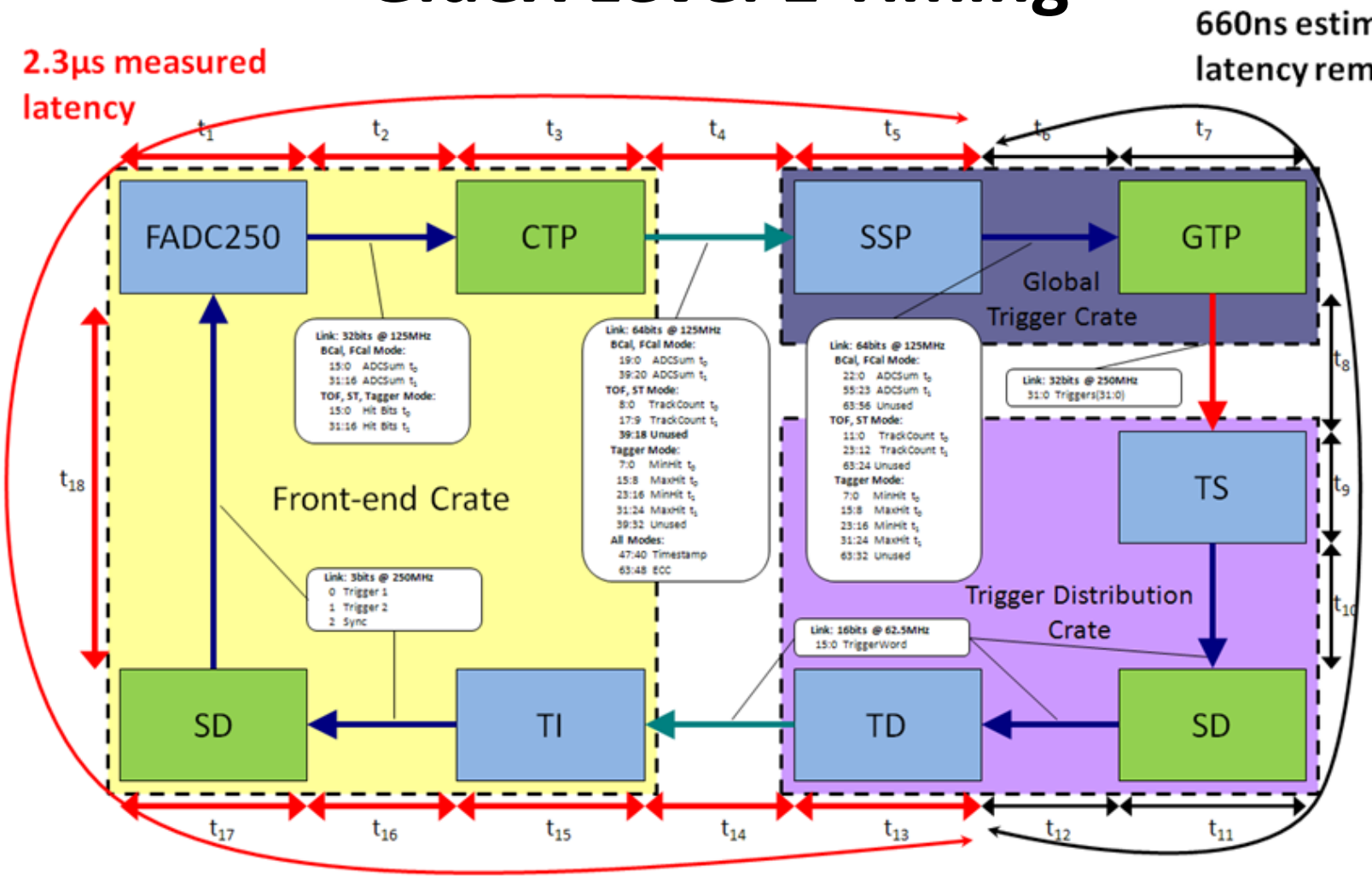
SSP Block Diagram



GTP Block Diagram



GlueX Level 1 Timing



2.3µs (measured) + 660ns (estimated) < 3µs!

Fiber Optic Link
Copper Ribbon Cable
VXS Backplane