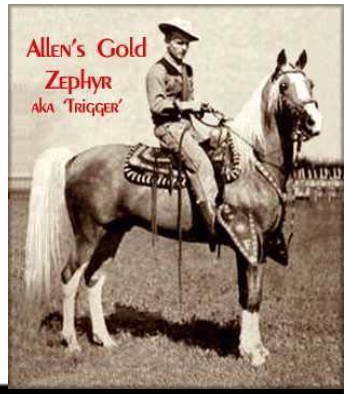
GlueX Collaboration Meeting

12GeV Trigger Electronics

28 January 2010

R. Chris Cuevas

1. FY10 Project Goals
   - Follow up from Sept '09 Meeting
   - Notes from other workshops
2. Hardware Design Status
   - Module Updates
   - ***Final*** VXS pair mapping
3. Schedule
   - FY11 and beyond



FY10 Goals

- **B**aseline **I**mprovement **A**ctivities (BIA) have been established for FY10
  - FADC250 Rev-
    Revision includes 12bit ADC and consolidation of FPGA which will reduce part count significantly. Use latest Xilinx technology and include new requirements.
  - F1-TDC Rev-2
    Revision includes 48 channel 'mode' for FDC, add VXS signaling, upgrade FPGA, add event RAM, and pulse output feature.
  - SSP (Prototype)
    Complete schematic, board layout, assembly, and firmware for at least two units.
  - GTP (Prototype)
    Complete schematic, board layout, assembly and firmware for a single unit.
  - Complete VXS crate specification and procurement for ALL VXS crates needed for 12GeV applications. Allows for quantity price reduction and 'phased' delivery during installation period.

New Trigger Requirements From Trigger Workshop

- Summary

1. Use the two trigger signals, Trig1 and Trig2 to change the mode of the flash board readout. Presently the readout mode is selected when the User programs the module before starting a 'run'. Presently the mode does not change during a 'run'. Using the two Trigger bits, the trigger supervisor can issue a specific readout mode for a given trigger event type. (e.g. Change mode to initiate a scaler readout event)

✓ 2. Dedicate a VXS differential pair from the TI to CTP and from the TI to the SD. Keep the I^2C link, but a differential pair will be needed to transfer data from the two switch cards at a higher rate than the I^2C allows. (The dedicated pair is not required to be a gigabit serial link.)

✓ 3. Add input/output signaling capabilities to the CTP and TI front panels. The number and type of signaling levels were not defined, but I/O signals will be required and allow for a number of useful features

✓ 4. Global Trigger -- Implement multiple trigger partitioning "sessions". Ed and David A. outlined a simple idea for up to 4 concurrent trigger sessions using CODA3.

✓ 5. Global Trigger – The Trigger Supervisor will need to manage external signals for calibration systems. Presently the TS is specified to connect directly to the Global Trigger Processor(s) and the additional inputs/outputs to pulsers or other hardware will need to be managed.

Other Workshops & Presentations

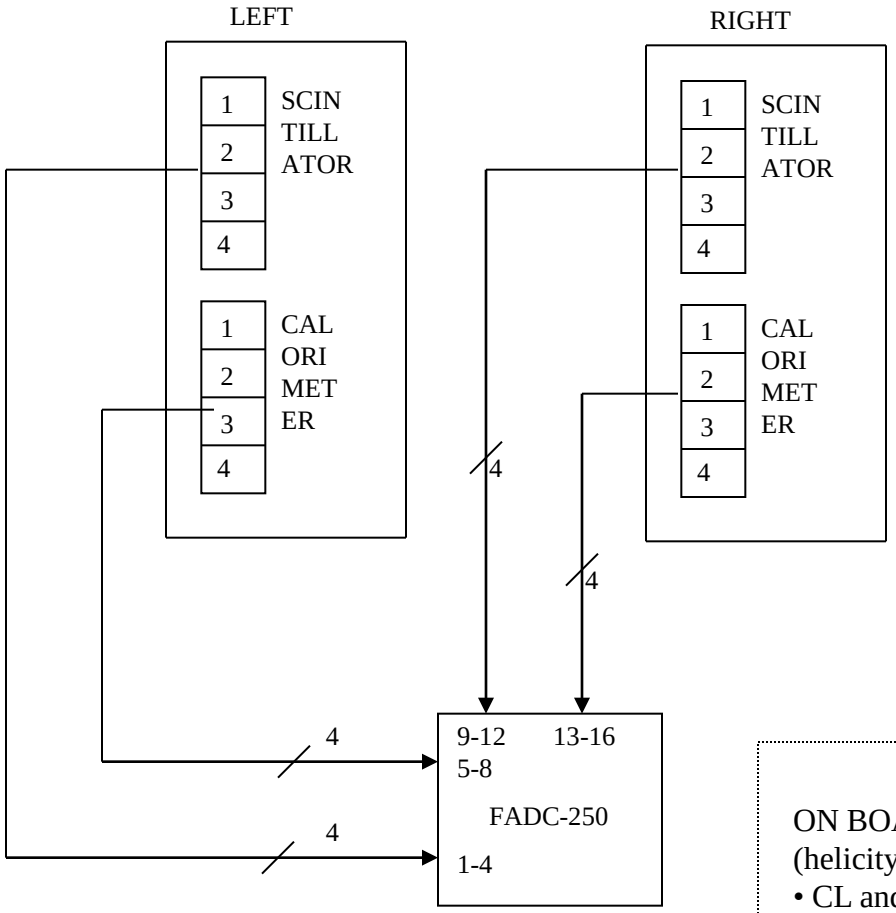
- There have been a number of presentations and reviews that have been completed since the June ‘09 12GeV Trigger Workshop @ CNU:
  - CLAS Collaboration June ‘09
  - S & T Review July ‘09
  - EIC Collaboration Nov ‘09 @Jlab
  - EIC Collaboration Jan ’10 @Stoney Brook

- I am delighted that other groups have a keen interest in the plans and performance of the new 12GeV trigger modules and system design.

- Trigger functions on the front end FADC250 have also been developed for use on 6GeV experiments. These developments and work efforts will be very useful for performance benchmarks, and firmware can be reused for future FPGA upgrade.

PREx -- HALL A Moller Polarimeter Application

H. Dong



When TRIGGER condition is met, send data that cause TRIGGER.

TRIGGER condition (or):
CL.AND.CR prescaled from 1 to at least 1000
CL prescaled from 1 to at least 1000
CR prescaled from 1 to at least 1000

$CR = \Sigma_{I=1,4}\sum_{j=1,2} P^J_I >$ threshold

$CL = \Sigma_{I=1,4}\sum_{j=1,2} P^J_I >$ threshold

$SL = (\Sigma_{J=1,2}\, S1^J >$ threshold) or ($\Sigma J=1,2\ S2^J >$ threshold) or ($\Sigma J=1,2\ S3^J >$ threshold) or ($\Sigma J=1,2\ S4^J >$ threshold)

$SR = (\Sigma_{J=1,2}\, S5^J >$ threshold) or ($\Sigma J=1,2\ S6^J >$ threshold) or ($\Sigma J=1,2\ S7^J >$ threshold) or ($\Sigma J=1,2\ S8^J >$ threshold)

ON BOARD SCALER (COUNTER) to be read out by a separate trigger (helicity and gate bits) at the helicity cycle of 30 to 2kHz.

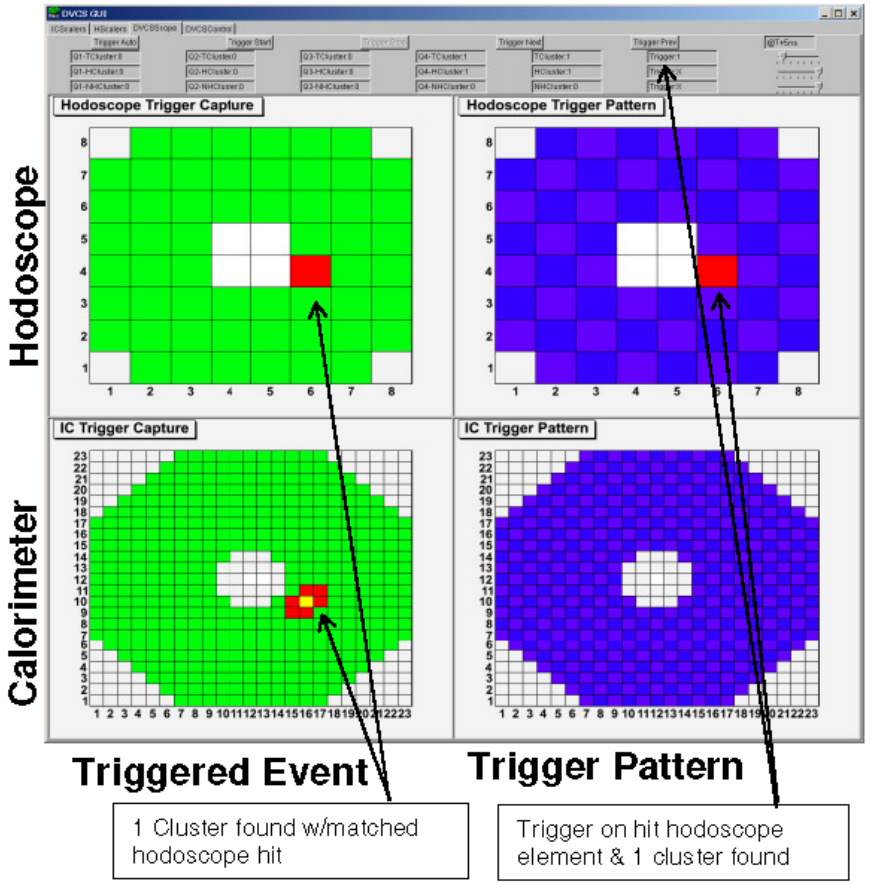
- CL and CR
- CL and SL
- CR and SR
- CL and CR and SL and SR
- CL and CR and (SL and SR delayed > 100 ns)

5.3 IC Cluster Finding Trigger

B. Raydo

424 Tower $PbWO_4$ Calorimeter & 56 Channel Hodoscope

- FPGA based trigger finds all clusters with calorimeter by considering all possible views with a 3x3 "sliding" window
- Cluster decisions can optionally be geometrically matched with hodoscope
- Decision time ~85ns, 66MHz pipeline
- Trigger module has a parallel diagnostic trigger that allows arbitrary triggers to be setup for algorithm/channel/timing verification (does not interfere with data taking)



Trigger application example
Implemented with CAEN1495

Hardware Design Status

- ***SubSystem Processor*** (Prototype by end of FY10)

Ahead of schedule
Schematic complete
Component placement complete
Preparing for routing
Firmware development on track

- ***Global Trigger Processor*** (Prototype by end of FY10)

Specification has been created and reviewed
Schematic not started
Schedule dependent on additional EE (Position open)

- ***Crate Trigger Processor*** (No work plan for FY10)

Two prototypes successfully tested! (FY09) ✓
Final revision in FY11 work plan

- ***Signal Distribution switch*** (No work plan for FY10)

Two prototypes successfully tested! (FY09) ✓
Final revision in FY11 work plan

Hardware Design Status

- ***Trigger Interface/Trigger Distribution*** (Latest revision by end of FY10)

Work activity schedule created (William Gu; Ed Jastrzembski)
Initial version of TI/TD successfully tested FY09
Latest revision specification document has been updated
Latest revision will be a single board design with TI/TD functionality
Schematic capture progressing nicely
Initial component placement has started
Board routing strategies to be developed
Firmware development on track

- ***Trigger Supervisor*** (FY11 work plan)

Specification has been created and reviewed
Detailed work activity schedule will be created

Specification Status

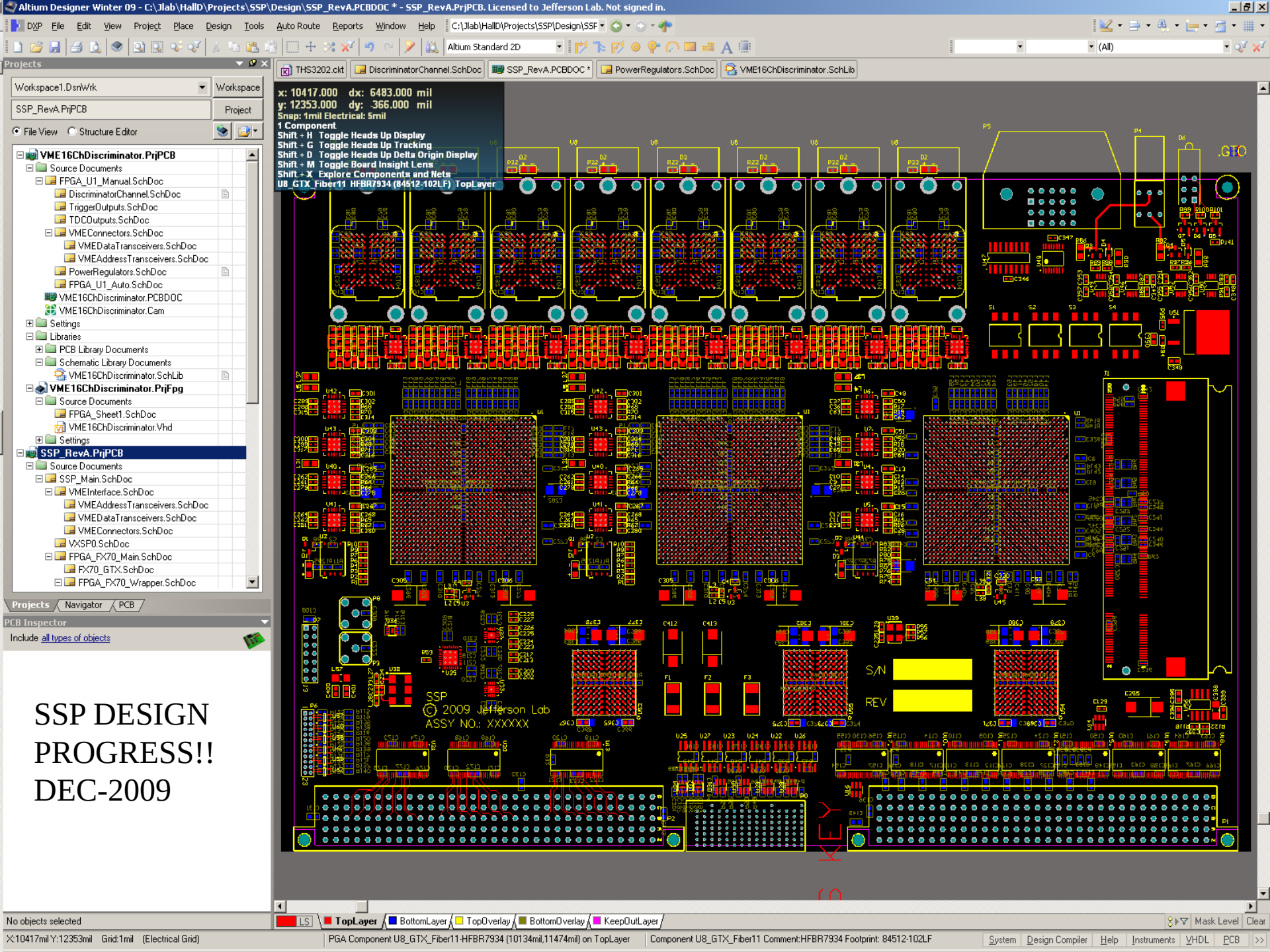
- ***VXS powered card enclosures*** (Procurement by end of FY10)

Crate specification has been created and ordering strategy discussed with procurement department. Multi-year procurement with delivery quantities per year to be determined.

- ***Trigger System Fiber Optics*** (FY11 work plan)

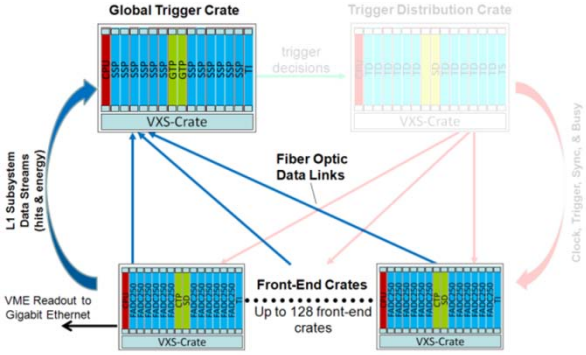
Draft system diagram has been specified

Final component specifications will need to be completed and ordered in FY11

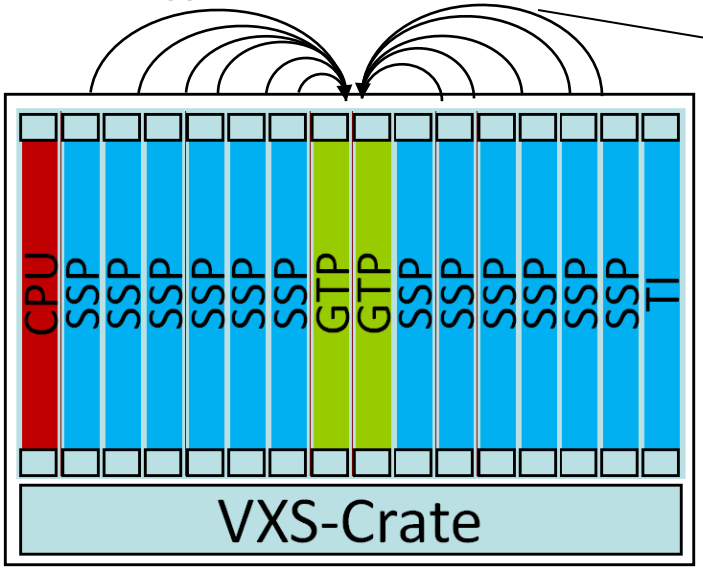


SSP DESIGN PROGRESS!!
DEC-2009

Subsystem Processor: L1



Global Trigger Crate:



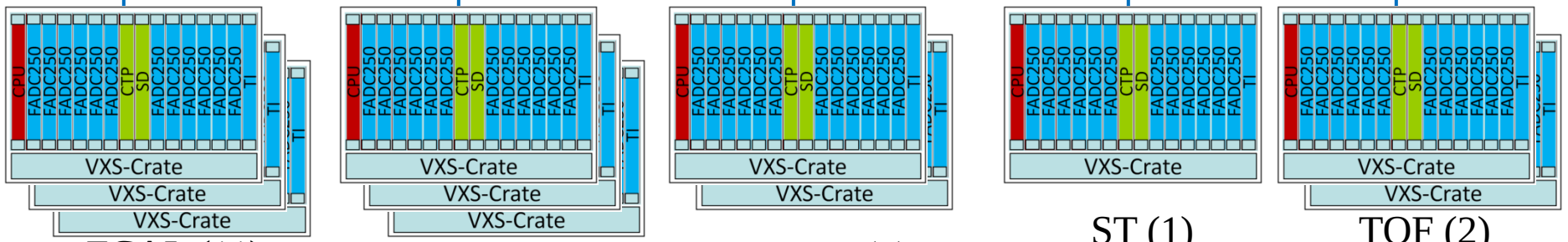
Subsystem Energy Sum & Hit Pattern (10Gbps to GTP)

- Sub-System-Processor (SSP) consolidates multiple crate subsystems & report final subsystem quantity to Global-Trigger-Processor (GTP)
- 32bit quantity every 4ns

Hit Pattern

10Gbps fiber optics

Energy



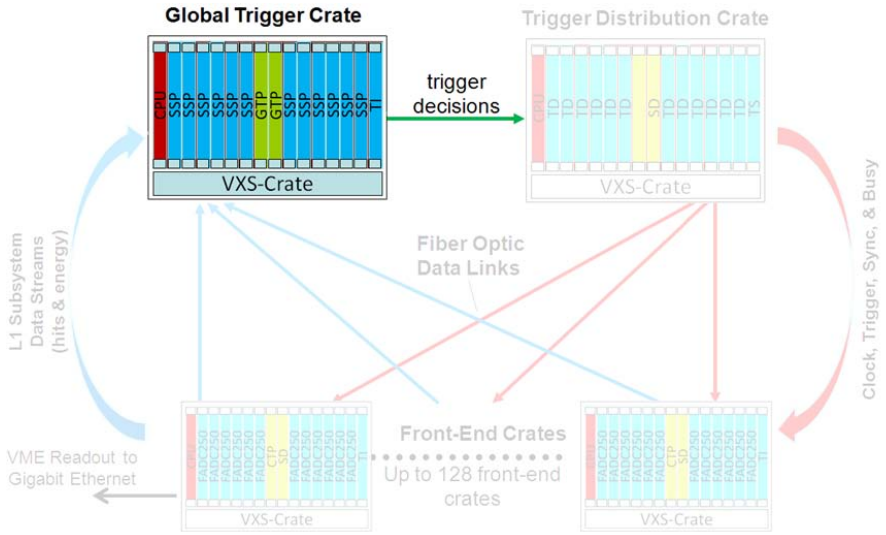
FCAL (11) BCAL (16) Tagger (2) ST (1) TOF (2)

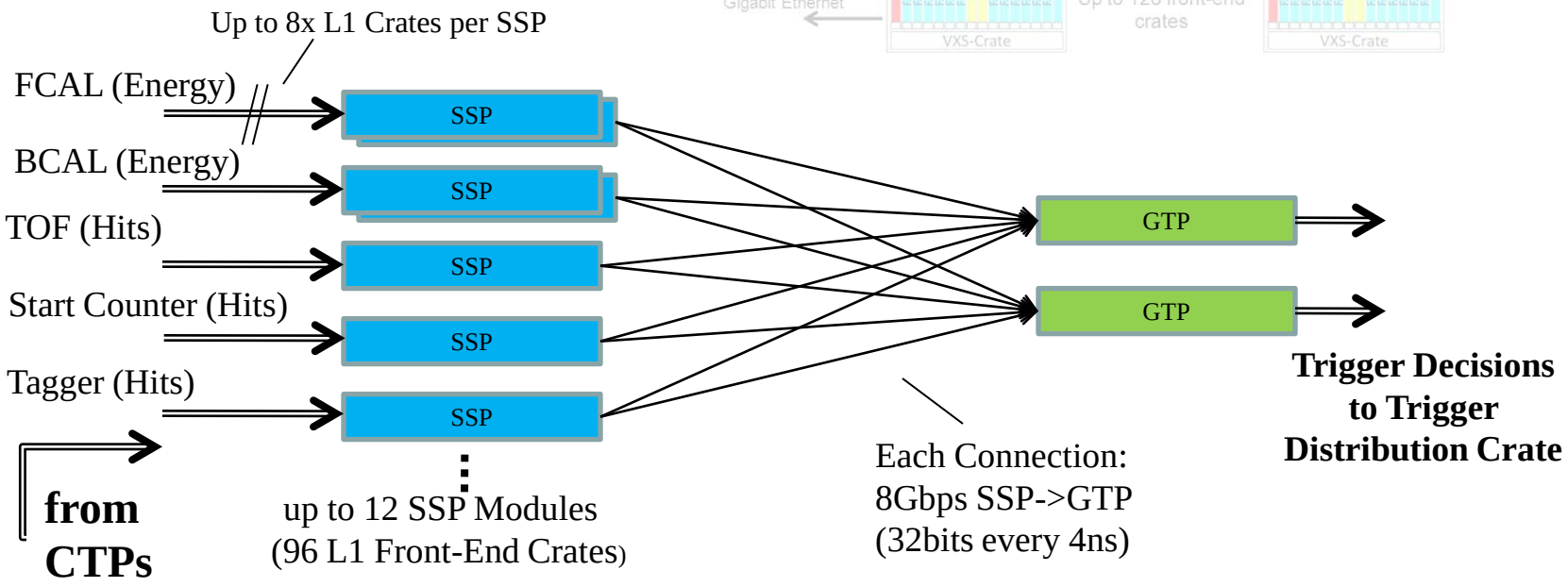
L1 Subsystems (# Crates)

Global Trigger Processor: (GTP)

- Global Trigger Processor (GTP) receives all subsystem Level 1 data streams

- Trigger decisions made in GTP and distributed to all crates via the Trigger Distribution (TD) modules in the Trigger Supervisor Crate





Trigger Interface (TI)
Trigger Distribution (TD)

• VXS payload board format
• Provides communication from VME to SD & CTP modules via I^2C serial links.

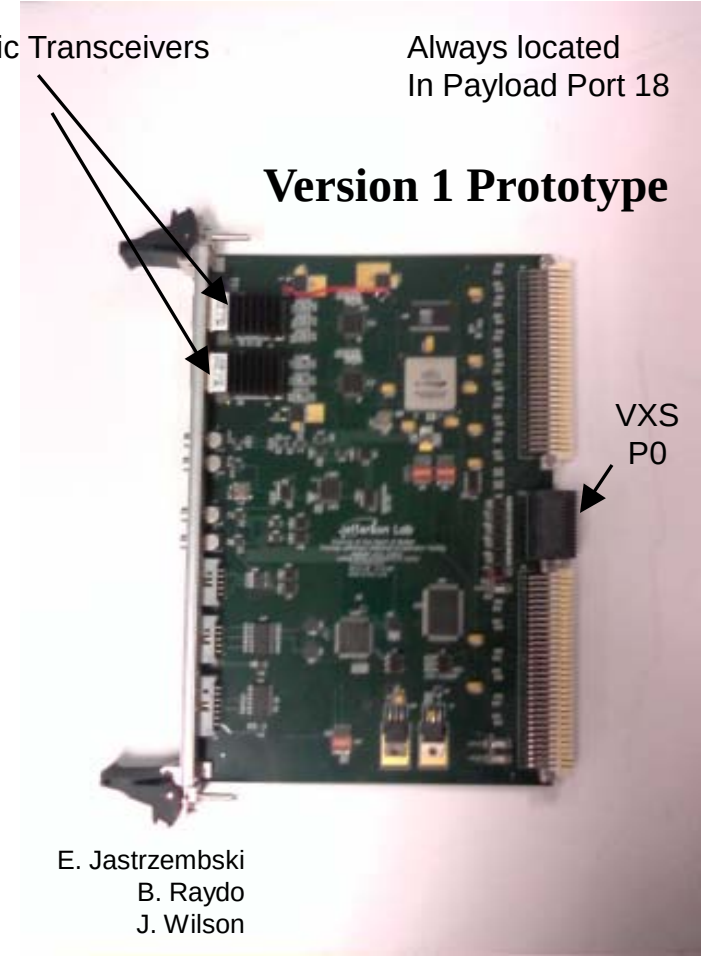
• Version 1 Prototype shown and was successfully tested with two VXS crates.

• William Gu has updated the specification and one circuit board design will be used for both TI or TD configuration.

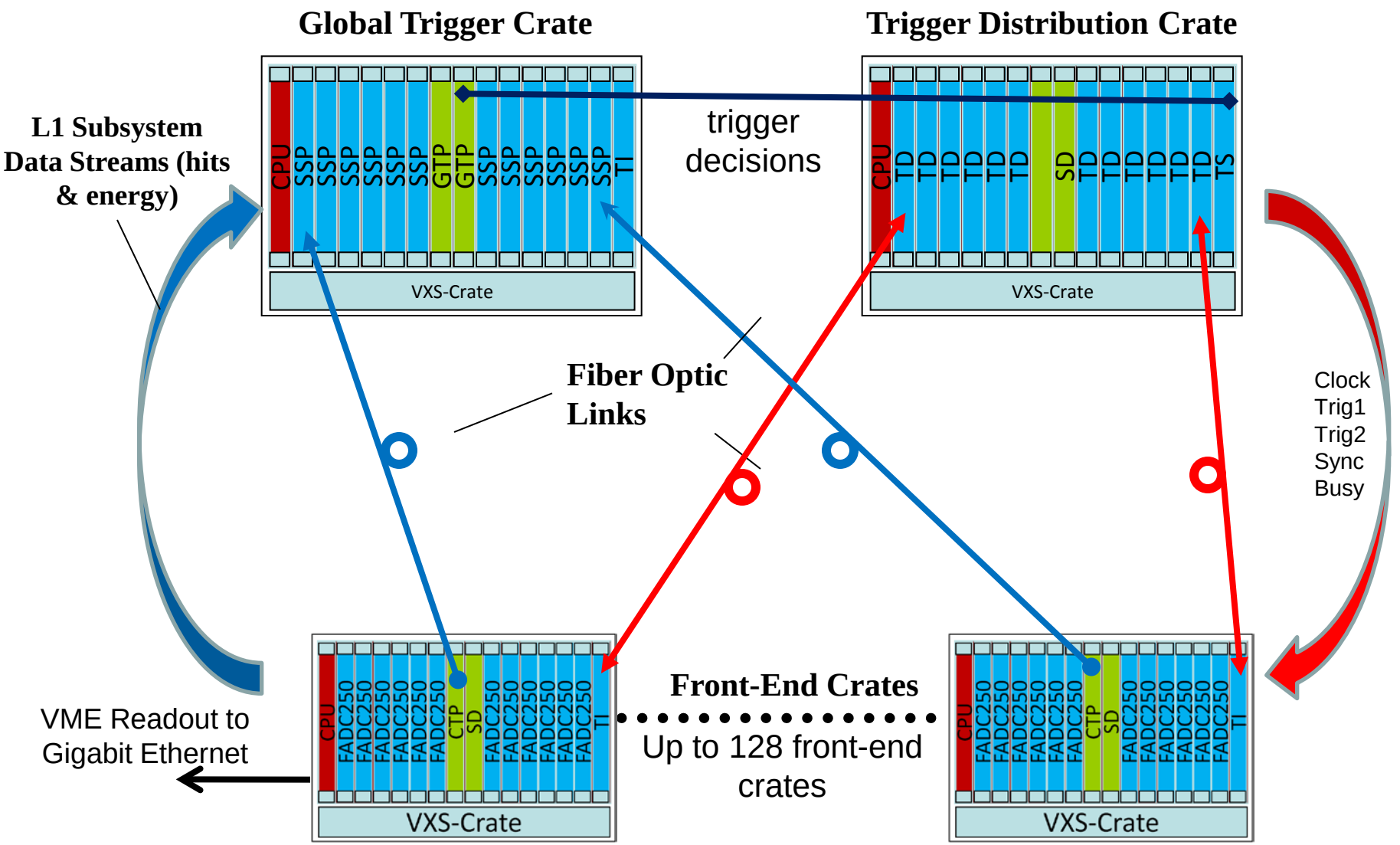
• Direct fiber optic link to Trigger Supervisor crate. Receives precision clock, synchronization, and trigger signals, plus trigger link status.

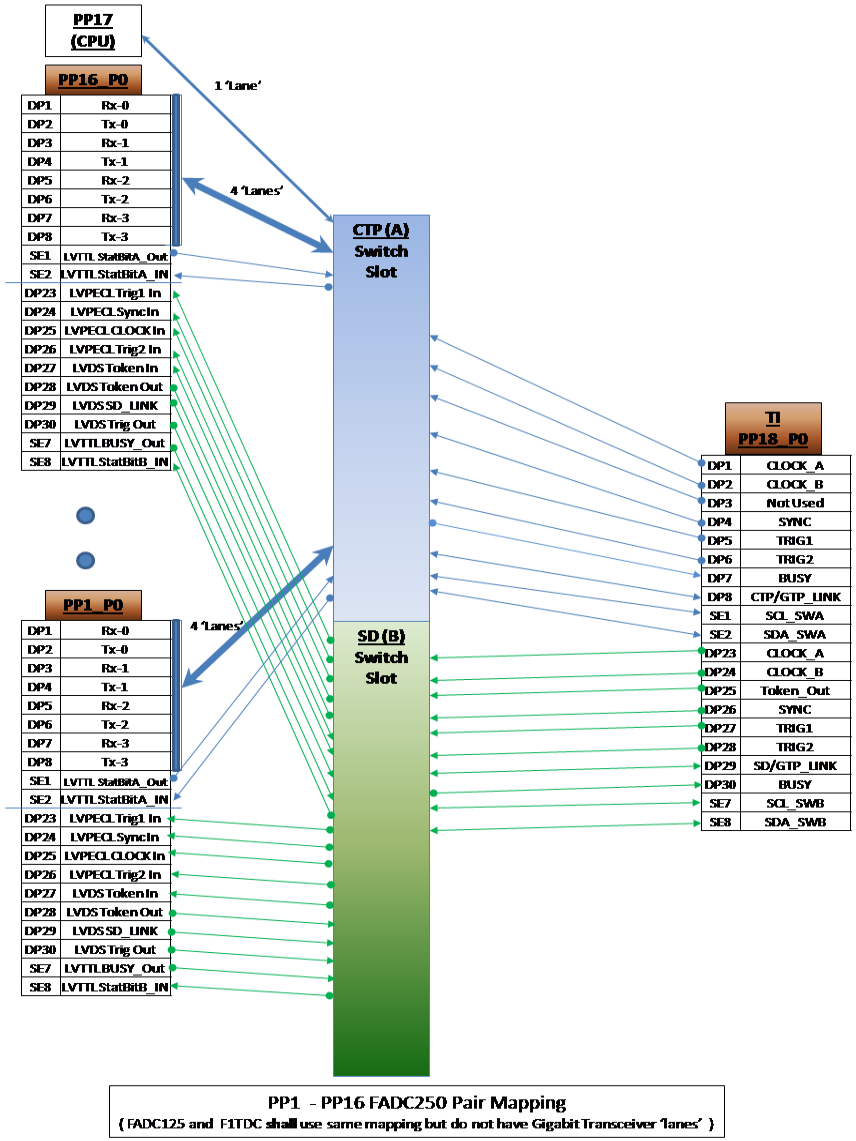
• Interfaces directly to crate SD module via the VXS backplane.

• Manages local trigger even buffers and interrupts to crate Read-Out Controller (ROC)



Level 1 & Trigger Distribution

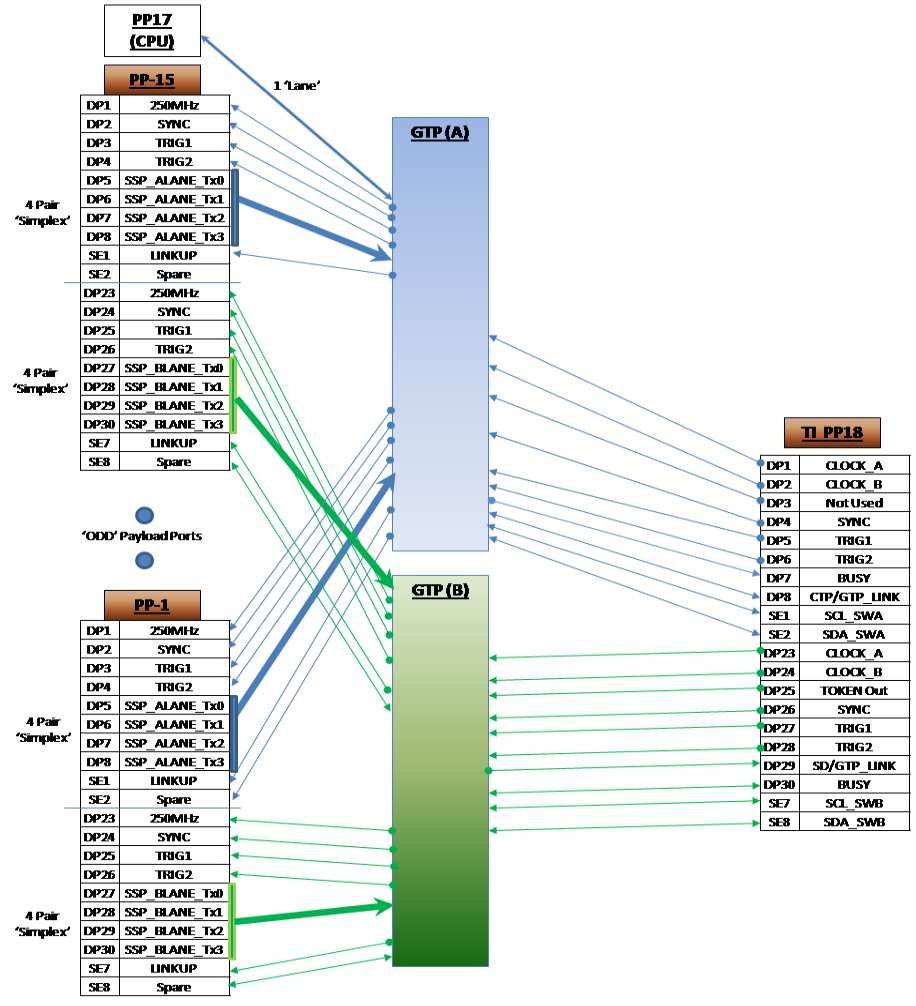




Front-End Crate VXS Pair Map

- *Final* configuration
- Other groups will use these definitions for their custom payload modules
- Careful consideration for use of SD and TI boards in the Global Trigger Crate

❖ F1-TDC and FADC125 crates will not require CTP



DP1	250MHz
DP2	SYNC
DP3	TRIG1
DP4	TRIG2
DP5	SSP_ALANE_Tx0
DP6	SSP_ALANE_Tx1
DP7	SSP_ALANE_Tx2
DP8	SSP_ALANE_Tx3
SE1	LINKUP
SE2	Spare
DP23	250MHz
DP24	SYNC
DP25	TRIG1
DP26	TRIG2
DP27	SSP_BLANE_Tx0
DP28	SSP_BLANE_Tx1
DP29	SSP_BLANE_Tx2
DP30	SSP_BLANE_Tx3
SE7	LINKUP
SE8	Spare

DP1	250MHz
DP2	SYNC
DP3	TRIG1
DP4	TRIG2
DP5	SSP_ALANE_Tx0
DP6	SSP_ALANE_Tx1
DP7	SSP_ALANE_Tx2
DP8	SSP_ALANE_Tx3
SE1	LINKUP
SE2	Spare
DP23	250MHz
DP24	SYNC
DP25	TRIG1
DP26	TRIG2
DP27	SSP_BLANE_Tx0
DP28	SSP_BLANE_Tx1
DP29	SSP_BLANE_Tx2
DP30	SSP_BLANE_Tx3
SE7	LINKUP
SE8	Spare

DP1	CLOCK_A
DP2	CLOCK_B
DP3	Not Used
DP4	SYNC
DP5	TRIG1
DP6	TRIG2
DP7	BUSY
DP8	CTP/GTP_LINK
SE1	SCL_SWA
SE2	SDA_SWA
DP23	CLOCK_A
DP24	CLOCK_B
DP25	TOKEN Out
DP26	SYNC
DP27	TRIG1
DP28	TRIG2
DP29	SD/GTP_LINK
DP30	BUSY
SE7	SCL_SWB
SE8	SDA_SWB

PP1 - PP16 Sub-System Processor Pair Mapping
(Eight SSP shown in crate map table below)
(64 Front-End Crates)

***
If CPU is a VXS payload, it will occupy PP17
Plan to implement 1 lane to both GTPA and GTPB

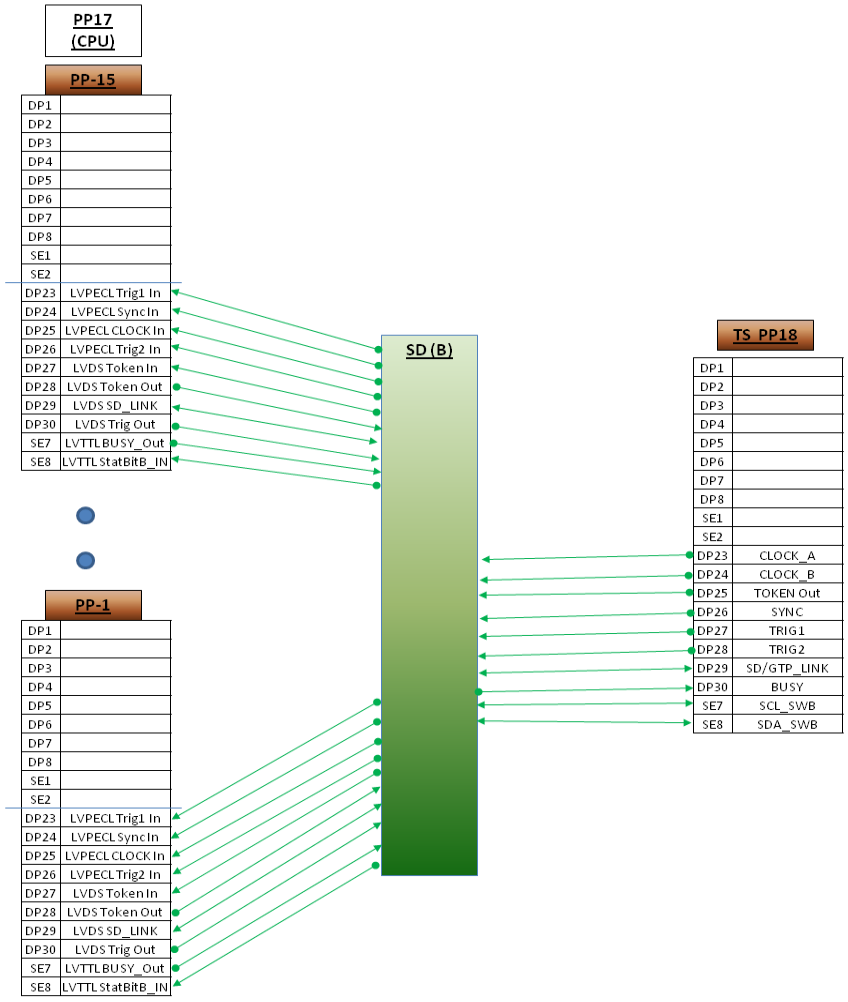
CPU	PP17	PP15	PP13	PP11	PP09	PP07	PP05	PP03	PP01	SWA	SWB	PP02	PP04	PP06	PP08	PP10	PP12	PP14	PP16	PP18
64x	***	SSP	SSP	SSP	SSP	SSP	SSP	SSP	SSP	GTPA	GTPB									TI

21 Slot VXS Crate Map

Global Trigger Crate VXS Pair Map

- SubSystem Processors are Payload board format and will communicate with two GTP

- Note TI mapping is identical to Front-End Crate



PP1 - PP16 Trigger Distribution Pair Mapping
(8 Trigger Distribution (TD) shown in crate map table below)
(64 Front-End Crates)

***
If CPU is a VXS payload, it will occupy PP17

CPU	PP17	PP15	PP13	PP11	PP09	PP07	PP05	PP03	PP01	SWA	SWB	PP02	PP04	PP06	PP08	PP10	PP12	PP14	PP16	PP18
64x	***					TD	TD	TD	TD		SD	TD	TD	TD	TD					TS

21 Slot VXS Crate Map

VXS "Trigger Supervisor/Trigger Distribution Crate"

Trigger Supervisor Crate (Trigger Distribution) VXS Pair Map

- Trigger Distribution (TD) are Payload board format and will communicate TS via a Signal Distribution (SD) switch module

- Note TD mapping is identical to Front-End Crate

Schedules, work plans for FY11 - FY13

- FY10 design projects are at full resource pace!
  - FADC250
  - F1TDC-V2
  - SSP
  - TI-TD
  - 16 Channel Discriminator/Scaler (*Hall B requirement*)
  - VXS Crate Specification
  - GTP (*Need EE full time*,)
  - Other non-trigger board projects are on-going also, but not the focus of this talk.

- Request from Larry to review work plans and budgets for FY11- FY13

- Broadly, the Hall D project plan lists substantial amounts for labor for installation and testing activities in the Hall for Trigger/DAQ and Electronics for FY11 – FY13

- Several of the board projects listed above will be available before FY11 begins

- FY11 will be an intensive year of significant 'system' level testing to assure that these boards are ready for final production quantity orders.

Schedules, work plans for FY11, FY12

Selected WBS activities extracted from Hall D project plan: Labor only

1.5.3.1 DAQ

	Start	Finish	Activity
$56,569	Jul-11	Dec-11	Install Crates
$64,526	Dec-11	May-12	Install Cabling
$47,414	Apr-12	Oct-12	Install Trigger Electronics
$94,828	Dec-11	May-12	Install Readout Electronics
$27,675	May-12	Aug-12	Check out CH Daq Equip
$27,675	May-12	Aug-09	Check out cabling
$29,176	Oct-12	Jan-13	Check out Trigger Electronics
$29,176	May-12	Sep-12	Check out Readout Electronics

1.5.4.1 FADC250

Jan-12 **ORDER 625 modules!!!!!!**

	Start	Finish	Activity
$84,919	Dec-10	Feb-11	Test feature extraction firmware
$84,919	Feb-09	Mar-11	Implement Summing and test
$6,632	Oct-12	Nov-12	Receive production modules
$13,264	Oct-12	Dec-12	Test and burn in
$16,580	Dec-12	Feb-13	Acceptance Testing
$8,290	Feb-13	Mar-13	Test in crates
$11,385	Mar-13	Jun-13	Assemble and test with Trigger

1.5.6.2 INSTALLATION

	Start	Finish	Activity
$16,975	Aug-12	Sep-12	Complete Installation of Readout System
$16,580	Jun-13	Jul-13	Install Trigger Electronics ALL
$12,598	Sep-13	Oct-13	Test of Trigger Electronics
$12,598	Oct-13	Nov-13	Hall Test of Readout System

1.5.4.2 F1TDC-V2

	Start	Finish	Activity
		Mar-09	**All F1 Chips ORDERED**!
$68,304	Dec-10	Feb-11	Test TDC timing with Discriminator
$84,919	Feb-11	Apr-11	Implement TDC firmware Test
$84,919	Apr-11	Jun-11	Dry run of test procedures
$3,316	Jan-12	Apr-12	**Receive TDCs**
$6,632	Apr-12	Jul-12	Burn in testing
$16,580	Jul-12	Nov-12	Acceptance testing single board
$8,290	Nov-12	Apr-13	Crate testing

1.5.4.3 TRIGGER

	Start	Finish	Activity
$15,914	Jul-11	Aug-11	Receive Crate Trigger Processor
$15,914	Aug-11	Oct-11	Burn In test
$26,524	Oct-11	Dec-11	Acceptance Testing
$79,548	Dec-11	Apr-12	Multi-crate Testing
$15,914	Jul-12	Aug-12	Receive balance of CTPs
$15,914	Aug-12	Oct-12	Burn In test
$21,219	Oct-12	Dec-12	Single board acceptance of GTP
$79,548	Dec-12	Apr-13	Crate acceptance testing
$53,040	Oct-11	Jan-12	GTP and TS testing
$53,048	Jul-12	Dec-12	Full Assembly of TS crate sys
$15,914	Dec-12	Jan-13	Burn in test of TS sys
$15,914	May-13	Jun-13	Board acceptance test of TS

Summary

- FY10 board design projects are on track
- ***GREAT WORK*** on keeping these projects on schedule
- Work activities exceed EE and E-Designer resources, but we push forward,
- GTP design activities must be started soon independent of new EE hire status

- Delighted to see that other groups are contributing trigger application ideas and providing important benchmark results.

- FINAL VXS pair mapping has been established so other groups (Hall A, Hall B) are able to start their custom VXS payload modules.

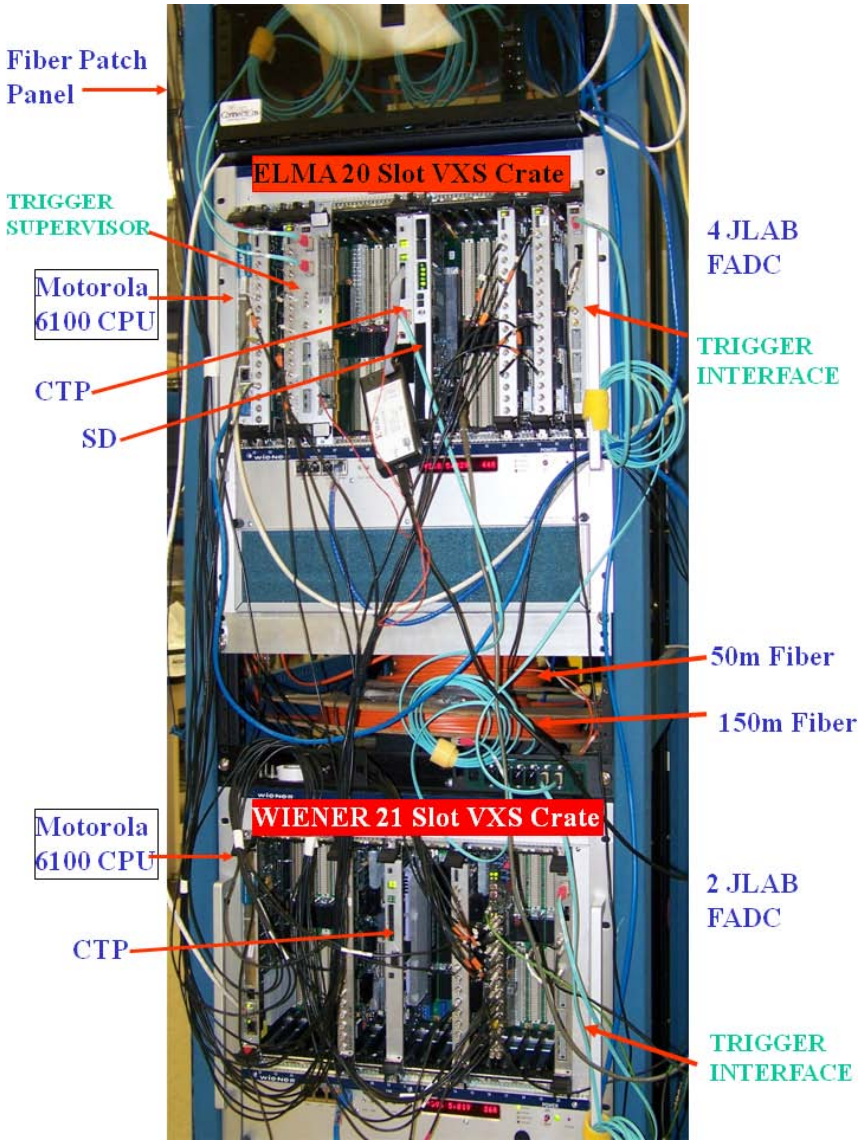
- Weekly 12GeV Trigger meeting has produced good discussions and ideas for implementation of system level test programs that will be essential for commissioning the DAQ/Trigger/Readout system in the Hall.

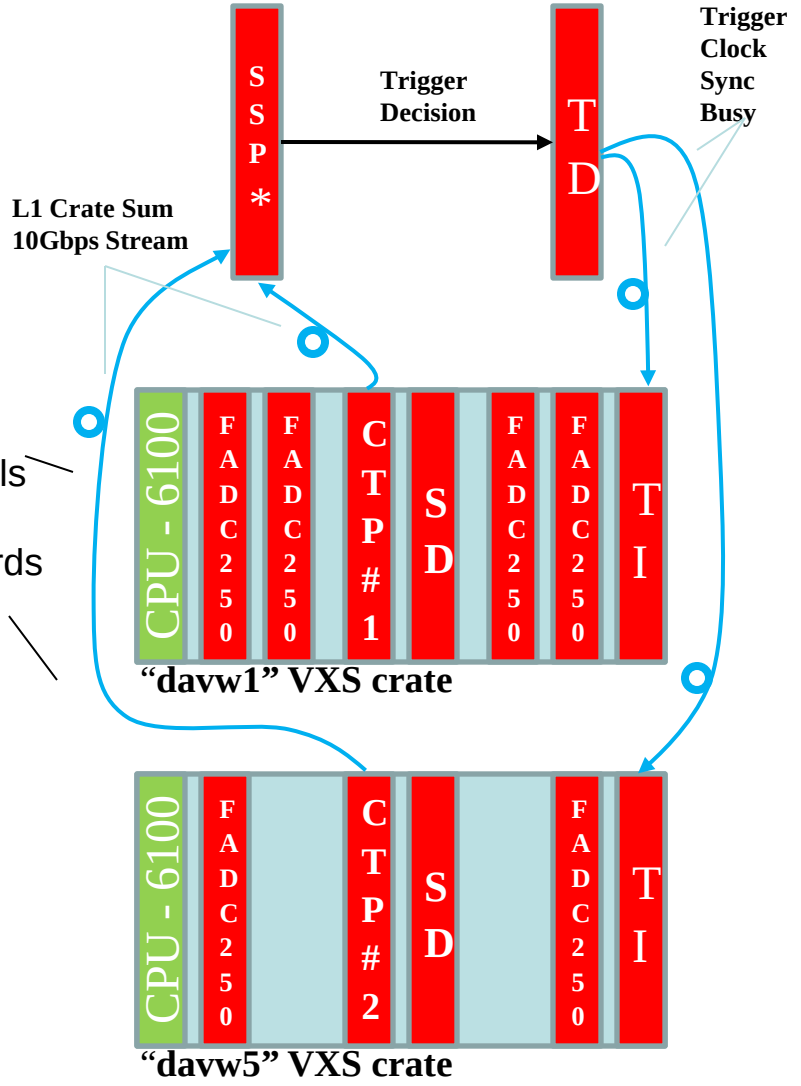
- Looking forward, the FY11 – FY13 schedule appears to be reasonable, (labor $$ included), but detailed work activities will need to be created to assure success.

Backup Slides

Level 1 Hardware Test Results

2 Fully Prototyped Front-End Crates



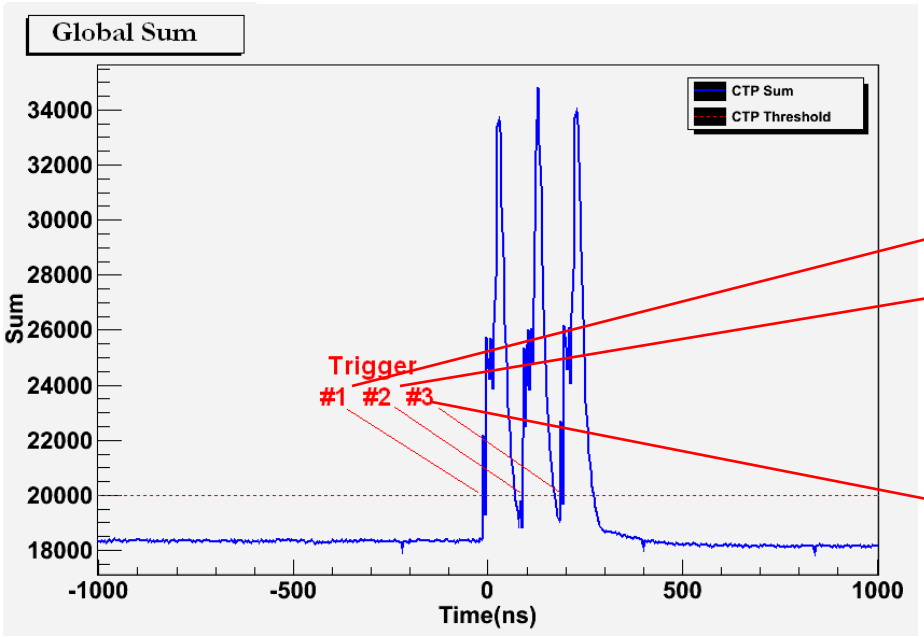


*SSP function embedded inside 2nd CTP

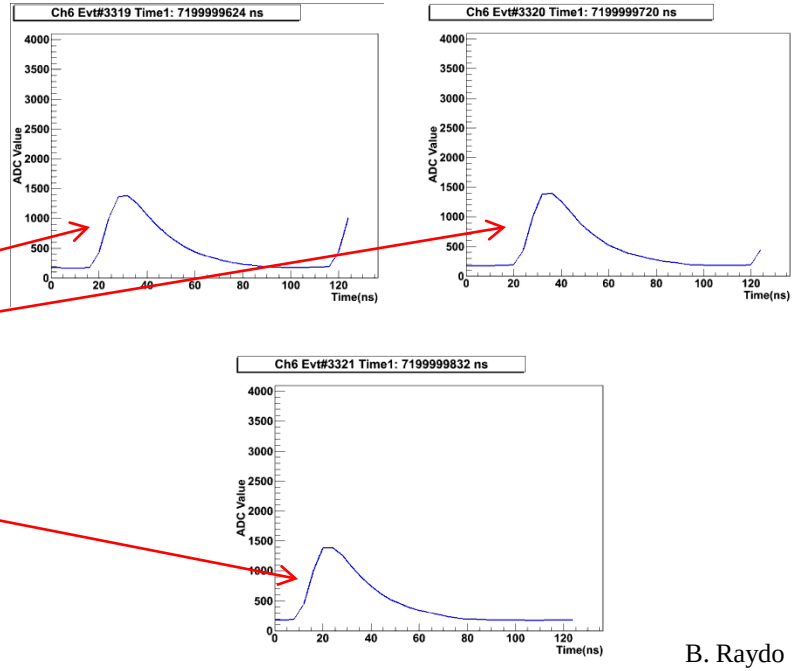
Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2µs global sum window is recorded around the trigger to see how the trigger was formed:



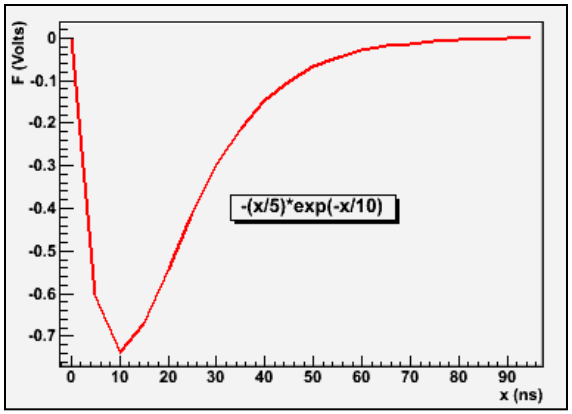
Example Raw Event Data for 1 FADC Channel:



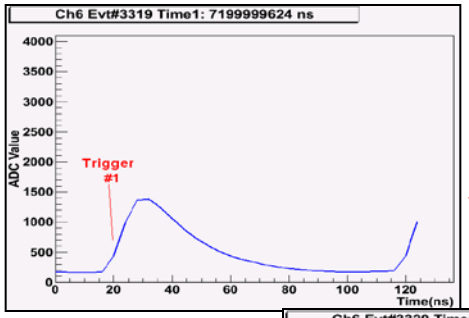
B. Raydo

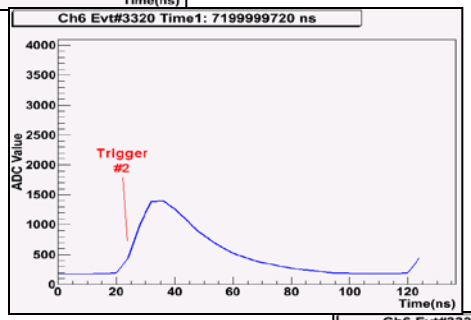
2 Crate Energy Sum Testing

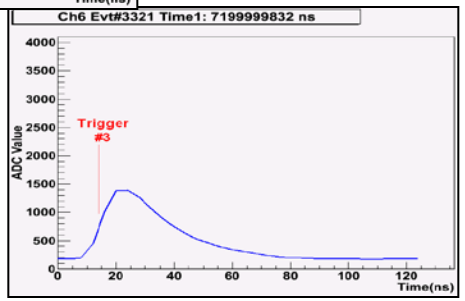
Input Signal to 16 FADC250 Channels:



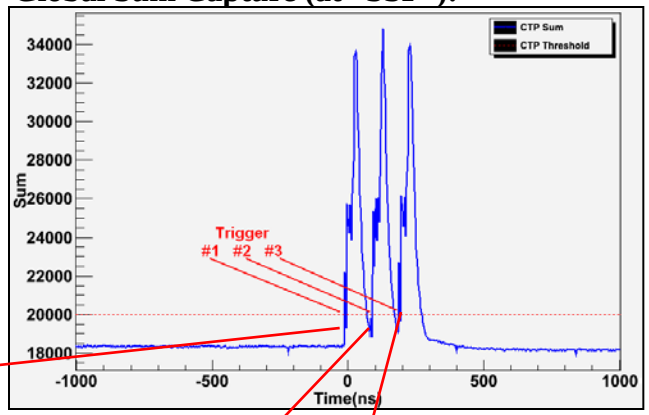
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- **Threshold applied to global sum (96 digitized channels) produces 3 triggers.**
- **Raw channel samples extracted from pipeline shown for 1 channel.**
- **Runs at 250kHz in charge mode**
- ***Latency: 2.3μs(measured) + 660ns(GTP estimate) < 3μs***

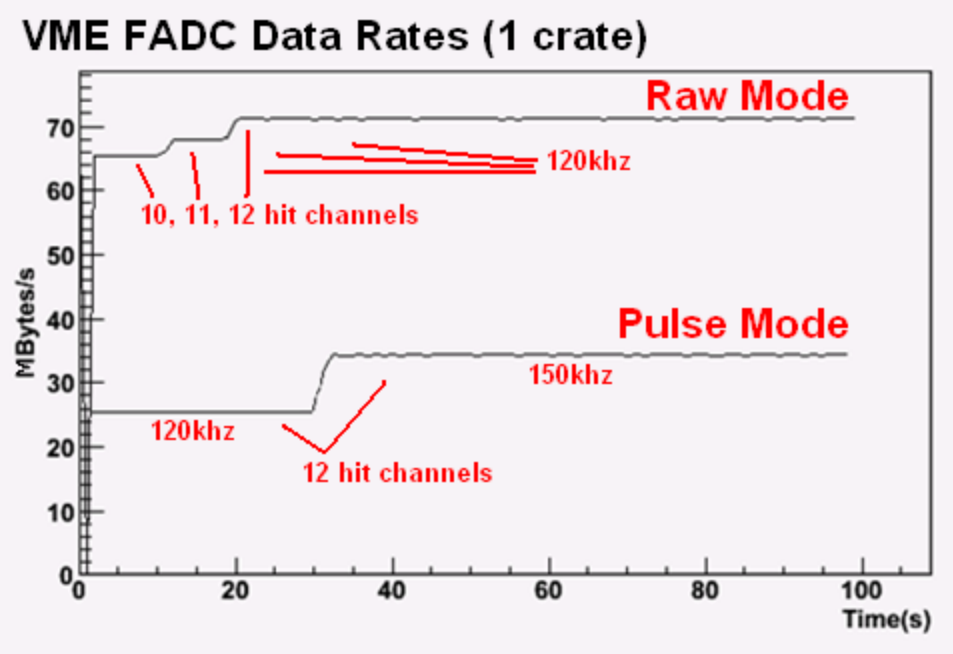
B. Raydo

Synchronized Multi-Crate Readout Rates

• FADC event synchronization has been stable for several billion events @ ~150kHz trigger rate.

• Have run up to 140kHz trigger rate in raw window mode, up to 170kHz in Pulse/Time mode.

• Ed Jastrzembski has completed the 2eSST VME Interface on FADC allowing ~200MB/s readout

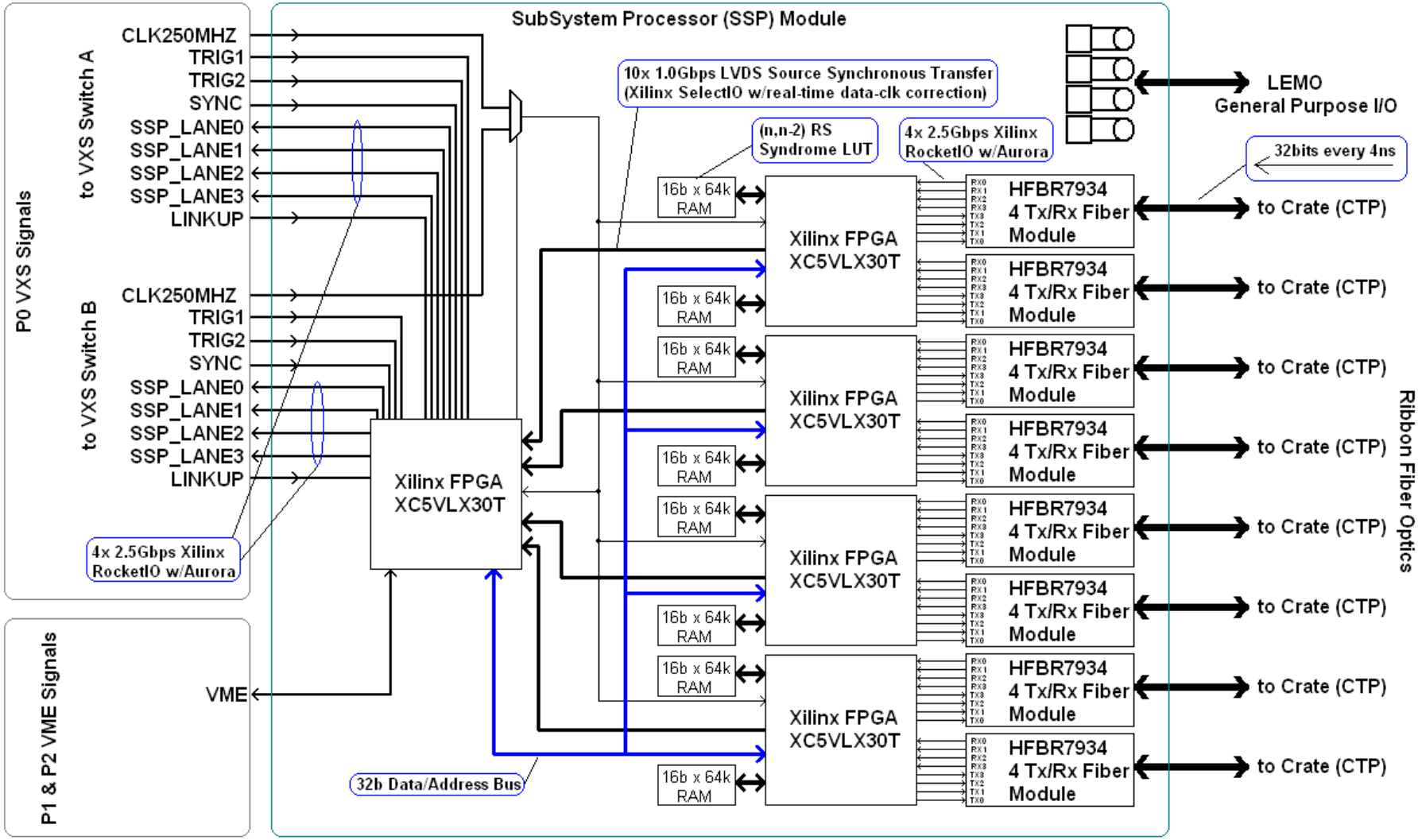


Single Crate
12 signals distributed to four FADC250

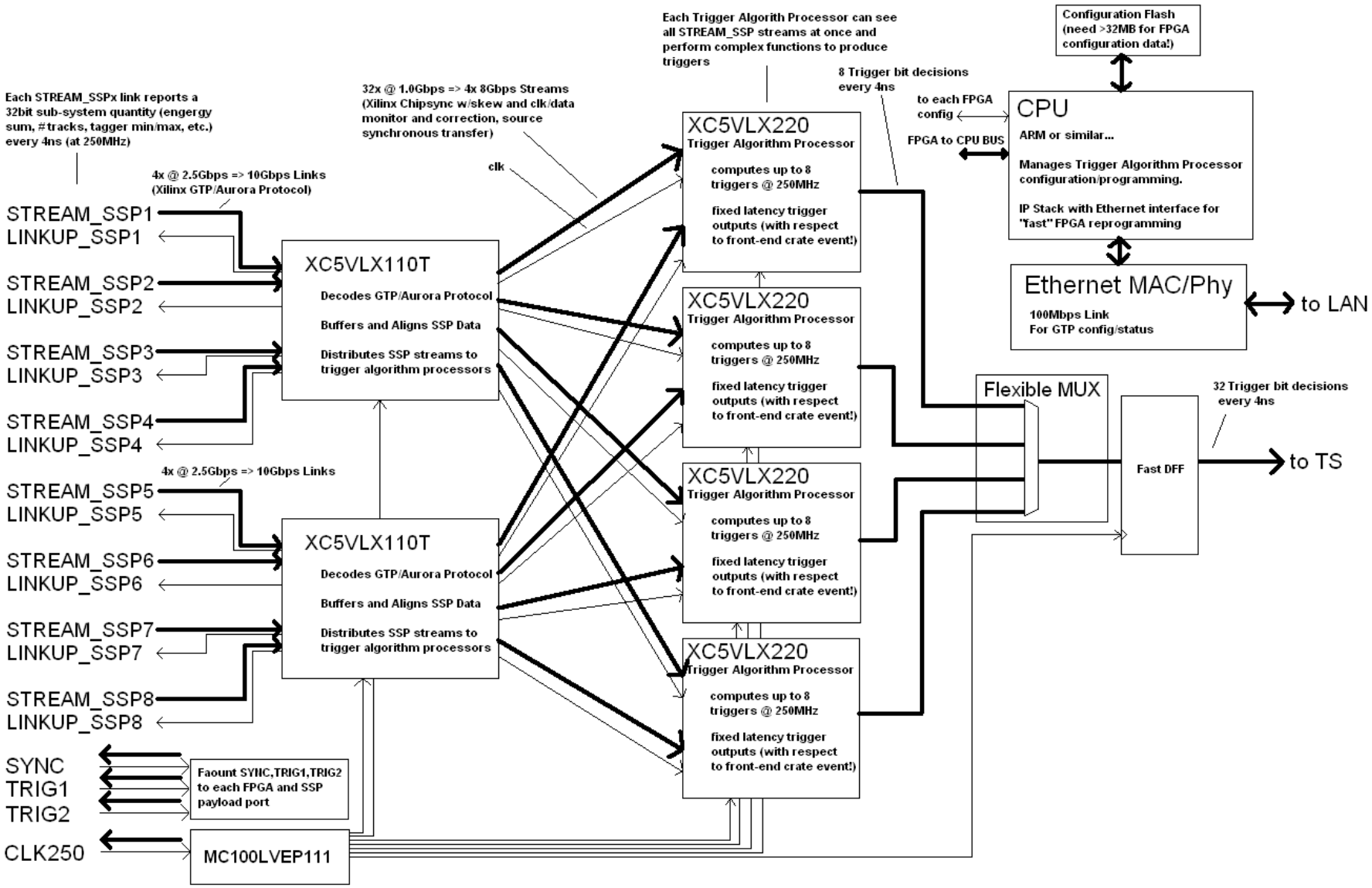
18% Occupancy

B. Raydo

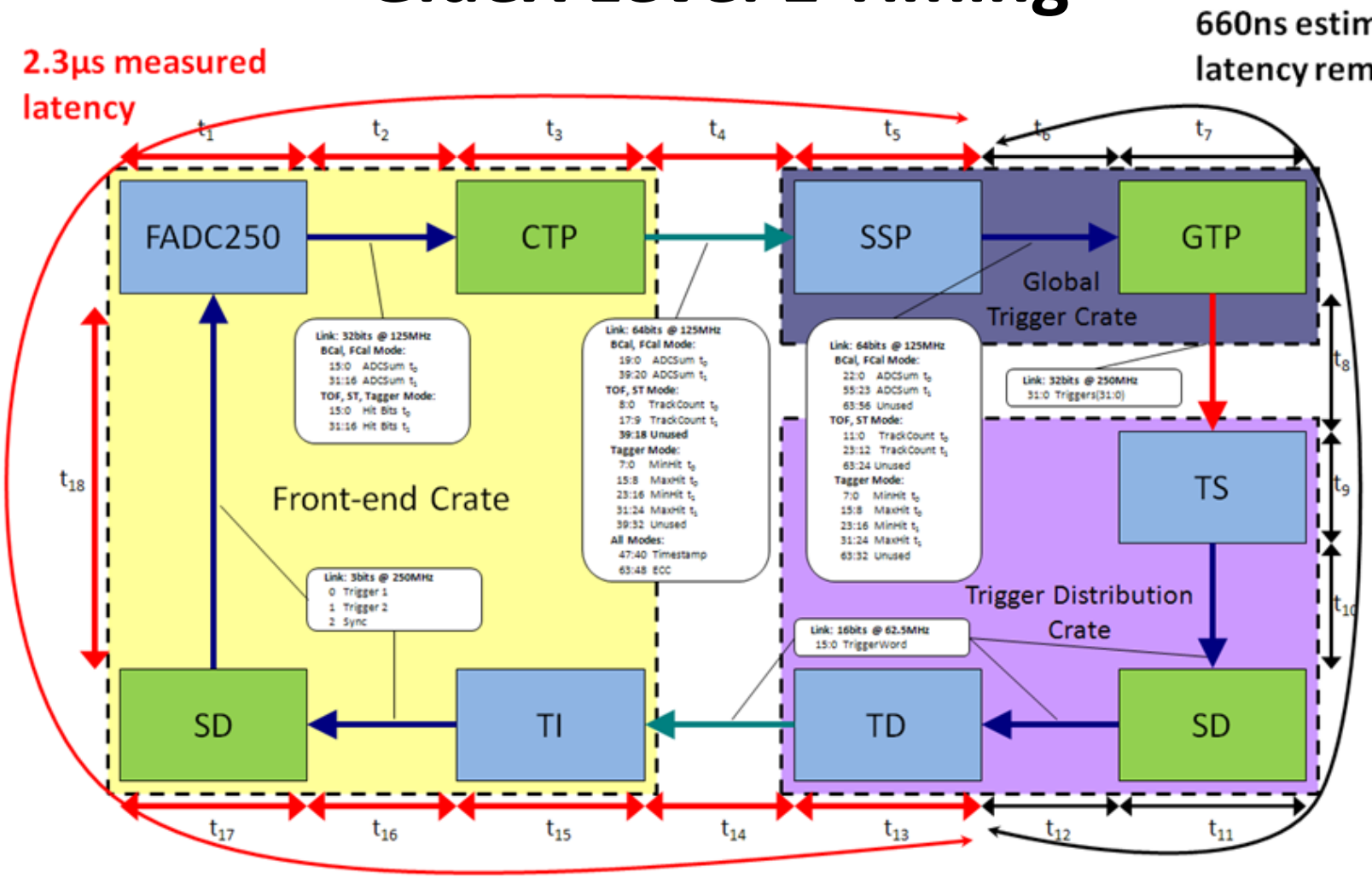
SSP Block Diagram



GTP Block Diagram



GlueX Level 1 Timing



2.3µs (measured) + 660ns (estimated) < 3µs!

Fiber Optic Link
Copper Ribbon Cable
VXS Backplane