

Fully Pipelined Custom Electronics

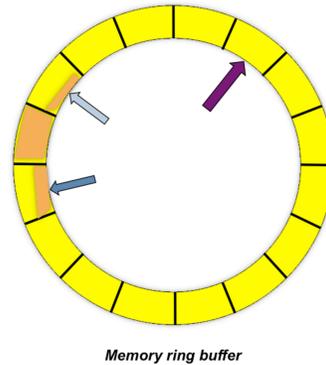
The GlueX experiment will utilize fully pipelined front end digitization electronics. This means that the detector signals will be continuously digitized in the front end boards, storing the values in on-board memory.

When a Level 1 trigger is received, the board will look back in time to the appropriate memory location and apply an FPGA-based algorithm. This will integrate the signal in a fixed time window as well as fit the leading edge of any signal to obtain the time.

Eventually, the integral and time values will be transported off the board through the VME backplane.

The ring buffers used to hold the samples for each channel are large enough to contain the last 3μs of sample data. This eliminates the need for the long, expensive delay cables used in previous generations of Nuclear Physics experiments.

Certain flash ADC modules are also equipped to sum the samples over all channels and transmit the sum via VXS (a high speed point to point connection system) to a central module to be used in the L1 trigger. A total digital sum of an entire 2800 channel calorimeter can therefore be update every 4ns. (See below)



Digitization



125 MHz Flash ADC

- 125 Msps
- 12 bits
- 72 channels
- VXS connection for clock synchronization
- Used for Drift chambers



250 MHz Flash ADC

- 250 Msps
- 12 bits
- 16channels
- VXS connection for digital sum (L1 trigger) and clock synchronization
- Used for calorimeters and scintillators



F1TDC

- 60ps or 115ps LSB
- 12 bits
- 32 or 48 channels (depends on desired resolution)
- VXS connection for clock synchronization
- Used for Fast detectors (60ps mode) and Drift chambers (115ps mode)

Level 1 Trigger System

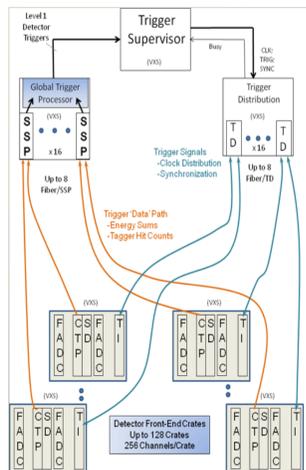


Illustration of the Level 1 trigger system

The level 1 trigger system (L1) will include both partial and total sums of the calorimeters. The >3500 calorimeter channels will be digitally summed every 4 ns and a threshold applied. This is done starting at the Flash ADC module level by summing all channels in the module and sending the sum over a high speed VXS connection to a dedicated Crate Trigger Processor (CTP) module.

The CTP will digitally sum the signals from all of the flash ADC modules in the crate and send the 32bit value over a high speed optical connection to a SubSystem Processor (SSP) module.

The SSP modules will each create a sum of the inputs from several crates and pass it over a VXS connection to the Global Trigger Processor (GTP) module.

The GTP will create the final stage sum as well as include signals from the Tagger and Time Of Flight (TOF) detectors to form the Level 1 trigger.

A Trigger Supervisor (TS) module manages the L1 trigger and communication with all of the crates.

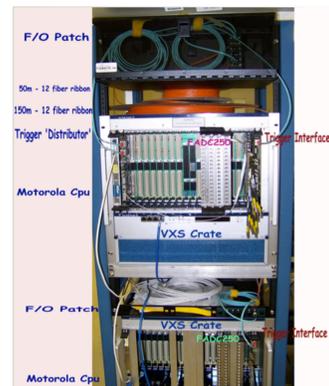
A Trigger Interface(TI) board and Signal Distribution(SD) board are used to distribute trigger and clock synchronization information to all of the modules in a crate.



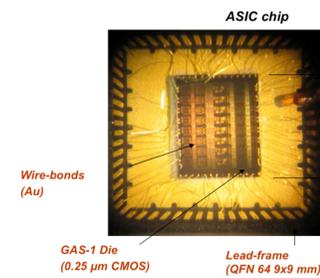
SD: Signal Distribution module



CTP: Crate Trigger Processor module



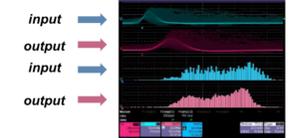
Drift Chamber Pre-amp



ASIC (Application Specific Integrated Circuit)

- Pre-amplifier and shaper
- Discriminator mode
- 8 channels per chip
- Custom design for GlueX

Performance of the shaper circuit in the ASIC



GPC-II (GlueX Pre-amp Card)

- 3 ASIC chips (one underneath)
- 24 channels
- Drift Chambers
- Custom design for GlueX

