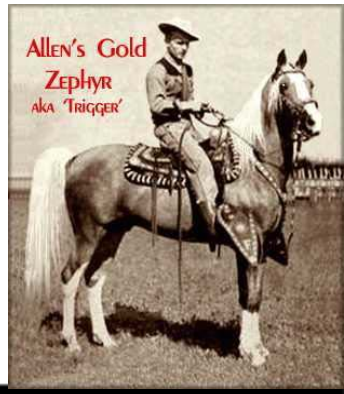
GlueX Collaboration Meeting

12GeV Trigger Electronics

9 – 10 May 2011

R. Chris Cuevas

1. Hardware Design Status Updates
   - Trigger Interface
   - Signal Distribution
   - Crate Trigger Processor
   - Sub-System Processor
   - Global Trigger Processor
   - DAq 'crate' status
   - Parallel Fiber Optics
2. Two full crates → DAq and Trigger Testing
3. Summary



Trigger Hardware Status

- **F**lash **ADC** 250Msps (**FADC250**)
  - ✓ Initial version 2 boards have been thoroughly tested and are working in the lab. – *See Fernando's update*
  - ✓ Will receive 35 pre-production boards in May!
  - ✓ Automatic board level verification test station is complete.
  - ✓ CODA library 'driver' updated and will be used for two full crate DAq testing

- **C**rate **T**rigger **P**rocessor (**CTP**)
  - ✓ We have 4 fully functional CTP modules
  - ✓ 2 latest CTPs include FPGA that support higher Gigabit speed (5Gbp/s)
  - ✓ A new CTP was used for verification of new WIENER VXS backplane
  - ✓ FADC250-V2 Gigabit outputs verified with CTP @2.5Gb/s per lane!

  - Collects trigger data (SUM) from 16 FADC250 modules within one crate *(16 bit sum every 4ns from 16 boards equals **64Gb/s!**)*
  - Transports trigger data over fiber to Global Trigger crate (SSP)
    - 10Gbp/s capability (8Gbp/s successfully tested)

Trigger Hardware Status

- **S**ignal **D**istribution (**SD**)
  - ✓ Precision low jitter fan-out of ADC clock, trigger and synch signals over VXS backplane to FADC250 modules
  - ✓ Revisions include clock jitter attenuation PLL
  - ✓ Two Rev-2 boards have been tested with Trigger Interface
  - ✓ A few power supply issues have been resolved, and updates to firmware have been completed to support PLL for jitter attenuation
  - ✓ I^2C communication with latest Trigger Interface is complete
  - ✓ Two boards will be used for full crate testing before ordering pre-production quantities.

  - ✓ Pre-production quantity of six boards will be ordered as soon as two crate DAq test verifications are complete. (June, 2011)
  - ✓ We have components and front panels for at least six more units

Trigger Hardware Status

- **T**rigger **I**nterface – **T**rigger **D**istribution (**TI - TD**)
  - ✓ FY11 test goals have been achieved and two units have been configured and installed in two crate DAq test station.
  - ✓ Minor design changes have been recorded and schematics and board layout changes have been implemented for pre-production order.
  - ✓ Plan is to order ten units after two crate DAq tests are verified.
  - ✓ Peripheral modules for TI-D have been completed.
    (i.e. Fan-out board for CAEN V1290 TDC)
  - ✓ CODA library has been updated for latest TI-D revision.

  - Direct link to Trigger Supervisor crate via parallel fiber optic cable
  - Distributes precision clock, triggers, and sync to crate SD modules
  - Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
  - Manages crate triggers and ReadOut Controller events

Trigger Hardware Status

- **S**ub**S**ystem **P**rocessor (**SSP**)
  - ✓ *Prototype board has been tested and is ahead of schedule.*
  - ✓ *New applications have been proposed for the SSP (CLAS12)*
  - ✓ Will use SSP during two crate DAq testing
  - ✓ Firmware to handle trigger information from two CTP streams will be completed soon.
  - ✓ SSP will collect trigger data from the two full crates and deliver the final trigger signal to the Trigger Interface.
  - ✓ SSP to GTP serial link definitions have been fully specified and implemented for VXS

  - Manages trigger information from up to 8 front end crates. (2048 channels!)
  - Trigger data received on front panel with fiber transceivers
  - 10Gbp/s input capability (4 lanes @3.125Gbps*(8/10b))
  - 10Gpb/s output stream to GTP on VXS backplane

Trigger Hardware Status

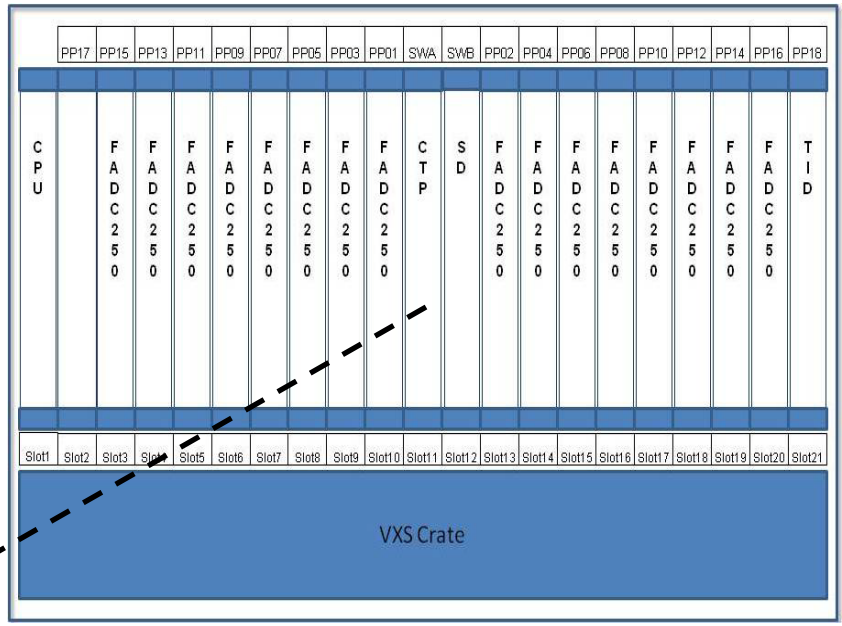
- **G**lobal **T**rigger **P**rocessor (**GTP**) (FY - 11)
  - ✓ Schematic is complete and board layout activities are nearly complete!
  - ✓ Significant activity for checking board fabrication files and assembly data before ordering prototype unit.
  - ✓ On track for FY11 goal to build initial prototype and test with SSP for global crate functions
  - ✓ Revisions to initial specification has been updated and finalized
  - ✓ Interface requirements to SSP and TS have been finalized
  - ✓ Large scale FPGA has been purchased and received including other long lead items.
  - ✓ Xilinx's Aurora protocol has been tested with Altera FPGA. Will be verified when prototype is received.
  - ✓ Great deal of firmware and verification activity after prototype is received from assembly company'

Trigger Hardware Status

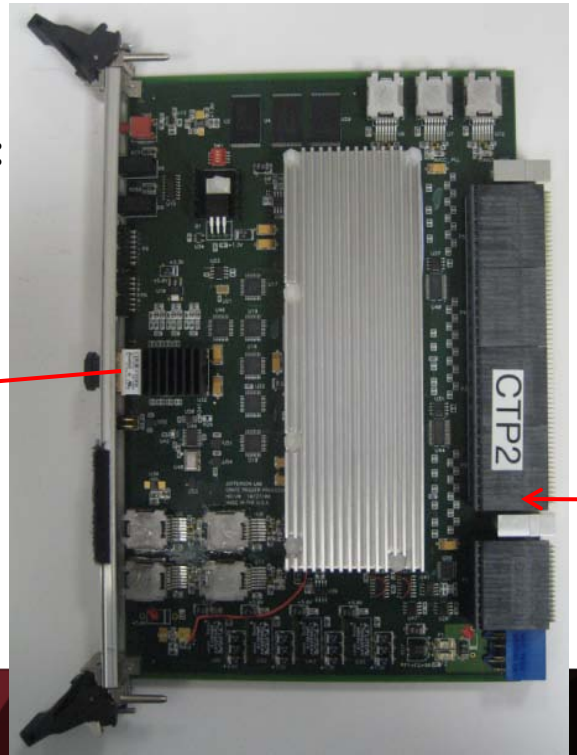
- **T**rigger **S**upervisor (**TS**) (FY-12 activity)
  - ✓ New board format – VXS Payload module
  - ✓ Distributes precision clock, triggers, and sync to front end crates via the Trigger Distribution modules.
  - ✓ Manages global triggers and ReadOut Controller events
  - ✓ Global Trigger Processor drives 32 bit trigger word to TS over copper cables.
  - ✓ Specification has been updated to match GTP output
  - ✓ Schematic and board layout activities will become full time activity after full DAQ crate testing is complete and pre-production orders for TI-TD and other boards have been completed.

Crate Trigger Processor

- **4** Fully assembled are tested and in the lab!!
- 2 newest units include VirtexV FX70T that supports higher serial speeds. (5Gbps) Matches FX70T on FADC250
- Initial CTP unit used to verify new WIENER VXS backplane map
- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)
- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



CTP Prototype:



MTP Parallel Optics

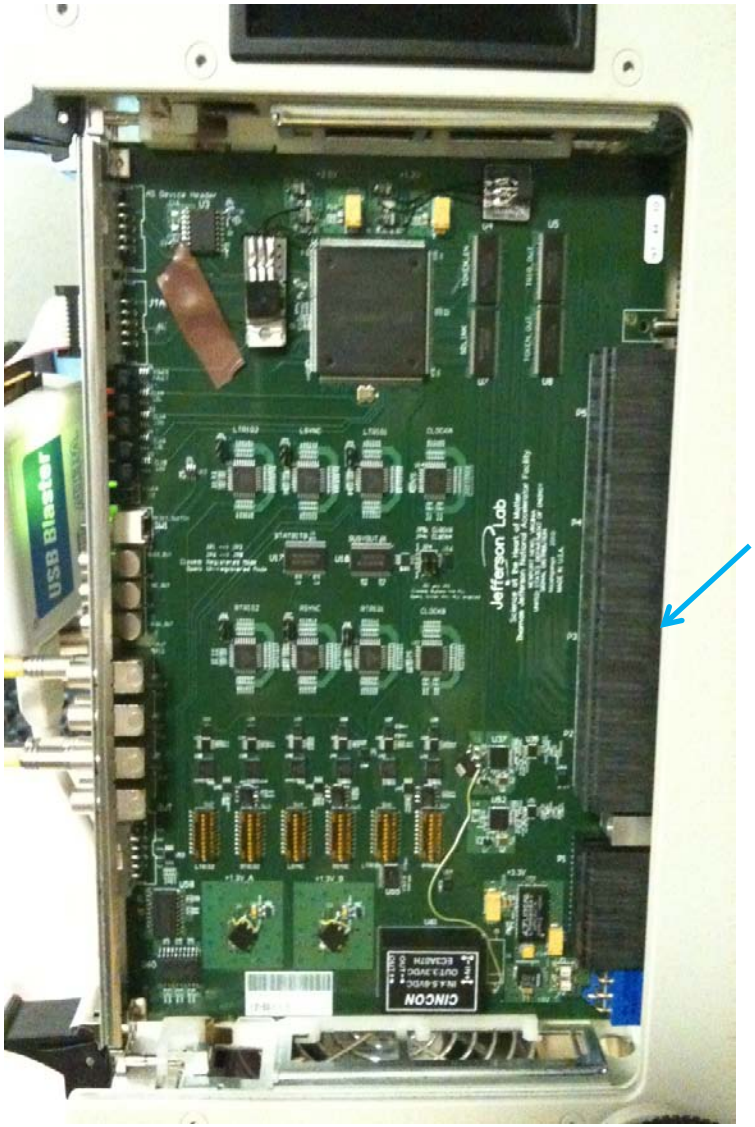
10Gb/s to SSP

VXS Connectors Collect serial data from 16 FADC-250

- Minor circuit modifications (ECO) needed before ordering production units. Goal is to order pre-production quantity by fall.
- Significant verification testing will be performed with 2 crate DAq station.
- Hall D requires 23 units
- Hall B requires 21 units

Crate Level – Signal Distribution (SD) -Rev 1

N. Nganga
10-Oct-2010



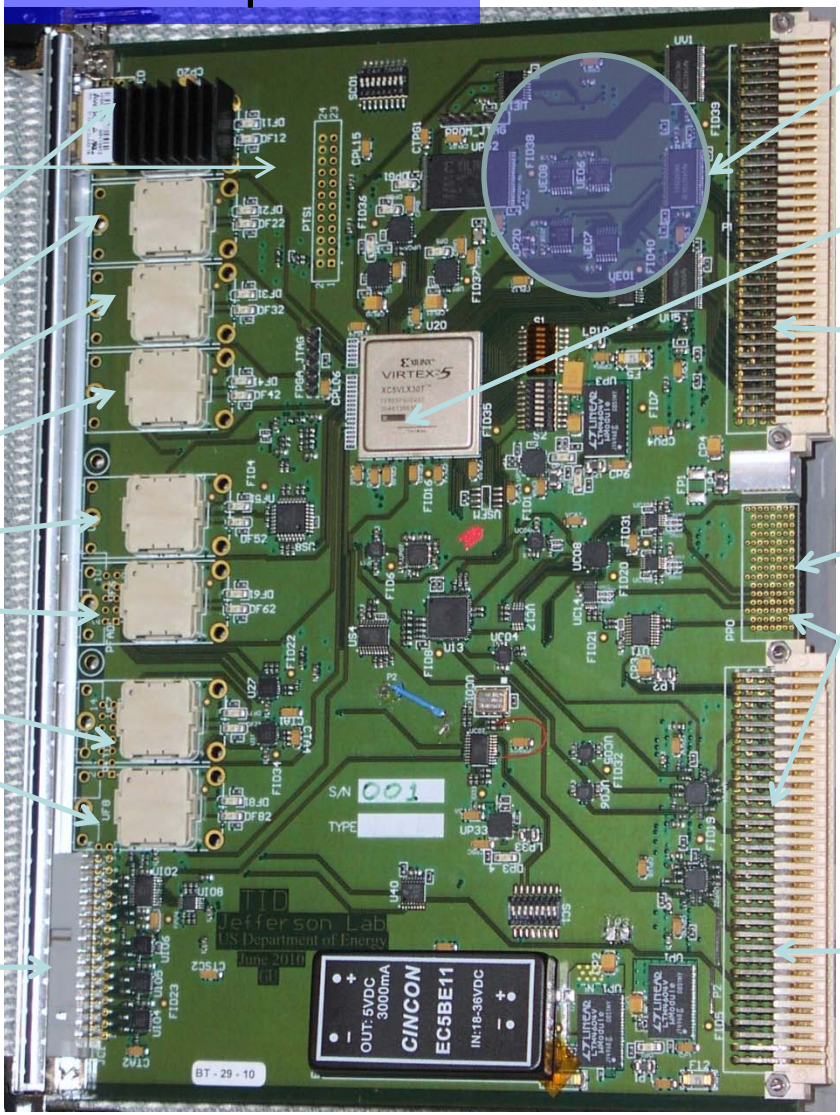
VITA 41 Switch Slot Connectors

- Two boards fully assembled and essential functions have been tested
- Rev_1 includes jitter attenuation PLL circuit that significantly reduces clock jitter to final payload (FADC250) slots
    - Jitter Attenuation achieves 1.5ps rms measured at payload slots.
- I^2C programming functions via TI have been tested
- Circuit corrections (ECO) have been identified and implemented in schematic and circuit board in preparation for pre-production order.
- We have the components and front panels required for a pre-production order of 6 units. Order by late summer.
- Production quantities:
    - Hall D needs 49 SD units
    - Hall B (and other Halls) need 30 units

Trigger Interface - Distribution

W. Gu
DAQ Group

TID Components



'Legacy' Trigger Supervisor Interface

Eight Optical Transceivers HFBR-7924

External I/O (trg, clk…)

VME→PROM (FPGA firmware) Emergency/remote re-programming

Xilinx VirtexV LX30T-FG665

VME 64x

VXS P0
TD mode: from SD
TI/TS mode: to SD

One dedicated link for redundant data collection

Trg/Clk/Syc outputs On row_C

Trigger Interface - Distribution

W. Gu
DAQ Group

✓ Testing is complete and this TI revision is ready for a pre-production order. Order will be placed as soon as two crate DAq testing is verified.

✓ Minor circuit modifications (ECO) have been completed and the circuit board files updated in preparation for the pre-production order.

✓ Ten pre-production units will be ordered and tested by end of summer. Final production quantities as follows:

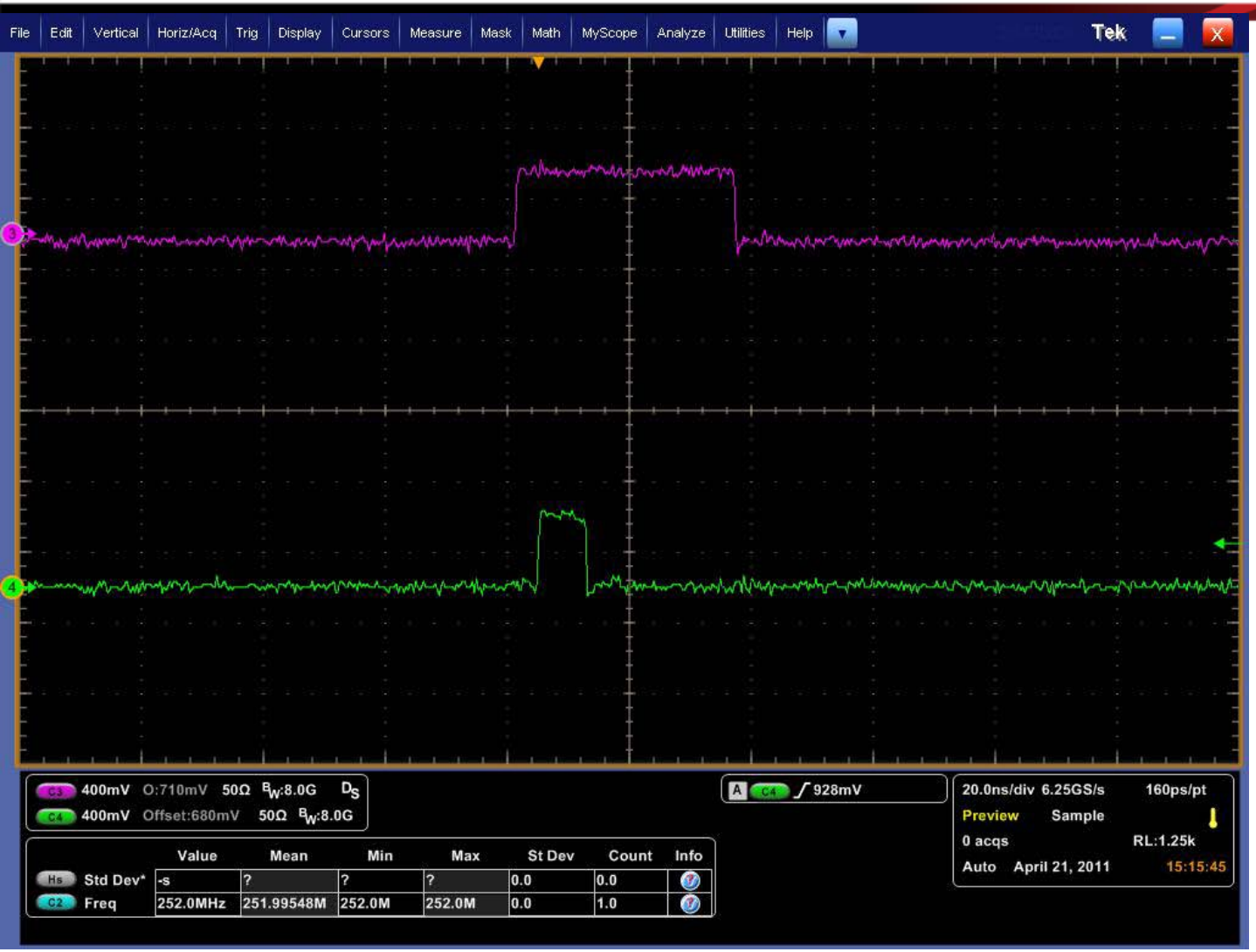
- Hall D: 56 units
- Other Halls: 35+ units

✓ Procedure to align (de-skew) trigger signal has been completed and verified with two crates in the lab.

Trigger Interface - Distribution

W. Gu
DAQ Group

5/6/2011



- ✓ Trigger signal aligned for two crates
- ✓ Trigger pulse width is programmable from 4ns to 128ns via TI
- ✓ 100m is fiber optic length difference that has been ‘de-skewed’ in this photo

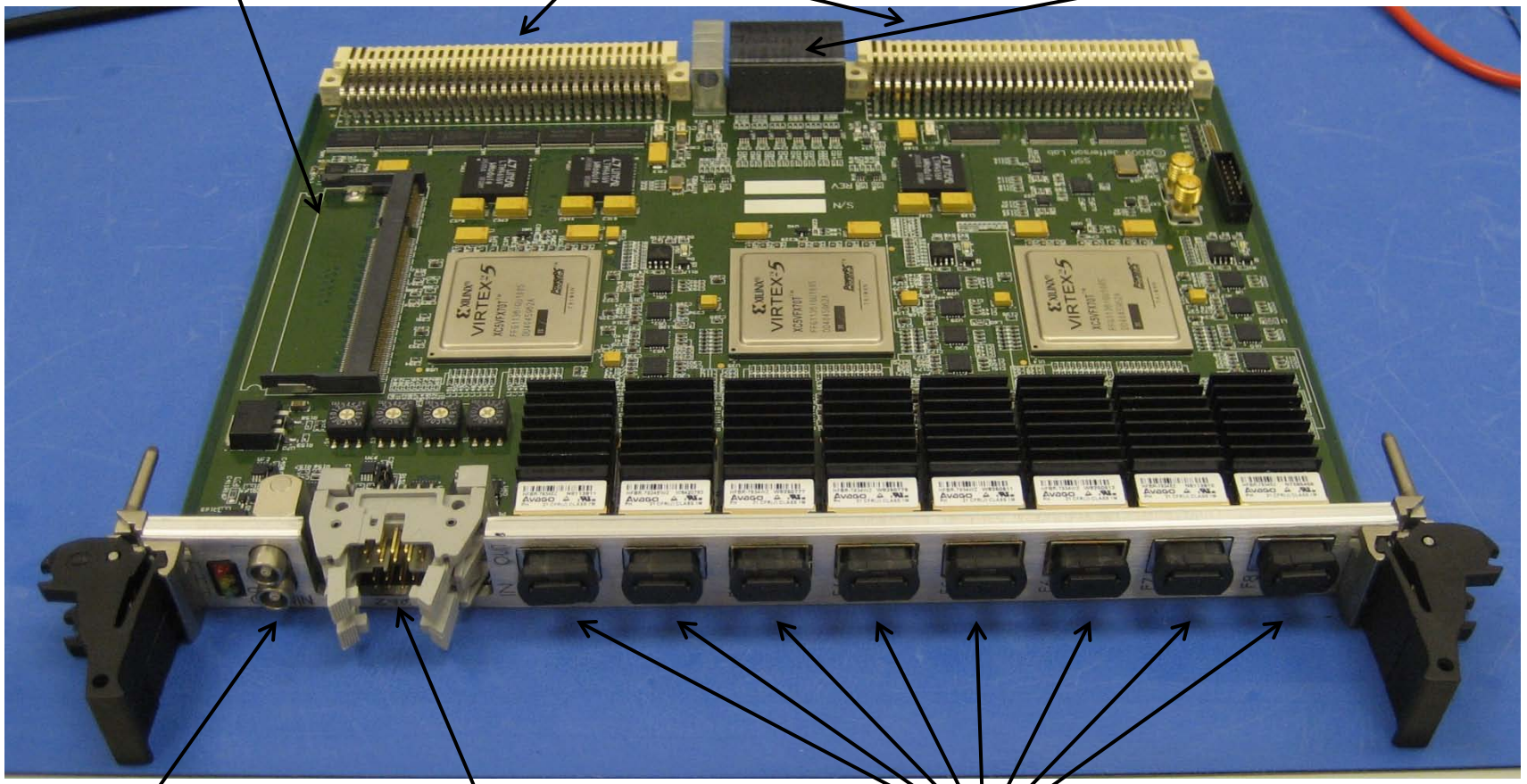
SSP Prototype

Ben Raydo
9-Sept-2010

Optional DDR2 Memory Module (up to 4GByte)

VME64x (2eSST support)

VXS-P0 (up to 16Gbps to each GTP)



2x NIM (bidirectional)

4x ECL/PECL/LVDS In
4x LVDS Out

8x Fiber Ports (10Gbps each to CTP)

Sub-System Processor

Ben Raydo
9-Sept-2010

✓ SSP prototype has been thoroughly tested and has been ahead of schedule.

✓ SSP will be used in the two crate DAq testing to demonstrate crate summing and other features, plus will source the final trigger output to the TI

✓ Very minor circuit modifications (ECO) have been identified on the prototype and the circuit board files updated in preparation for the production order.

✓ Relatively low quantity for all 12GeV experimental Halls, so pre-production order may not make sense. Final production quantities as follows:

Hall D: 8 units
Other Halls: <20 units

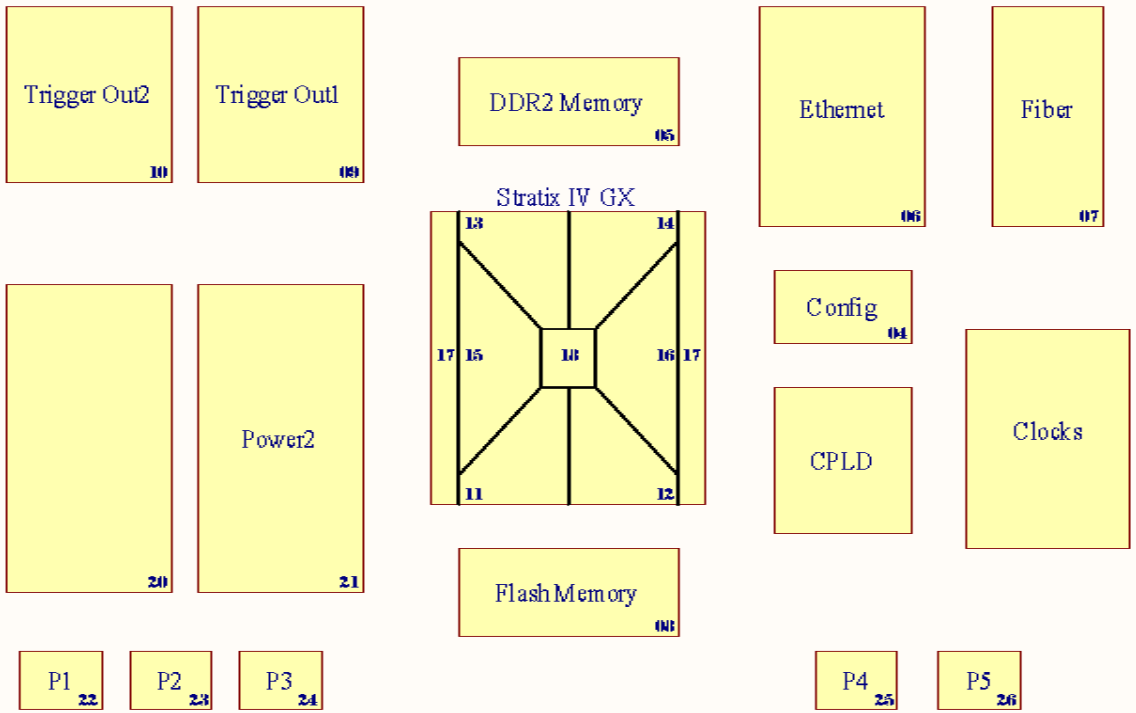
✓ On track to order by end of fiscal year 2011

Global Trigger Processor: (GTP)

Scott Kaneta
May 2011

Table of Contents

Stackup
1 - Top
2 - Power (1.8V, 1.1V, 1.5VCCA_GXB)
3 - GND
4 - Signal
5 - Signal
6 - GND
7 - Power (3.3V, 0.9V)
8 - Power (0.9VCCD_PLL, 2.5VCCA_PLL, 2.5VCCAUX, 3.0VCCA_GXB)
9 - GND
10 - Signal
11 - Signal
12 - GND
13 - Power (2.5V, +1.5VCC_PT, 0.9VRBF)
14 - Bottom



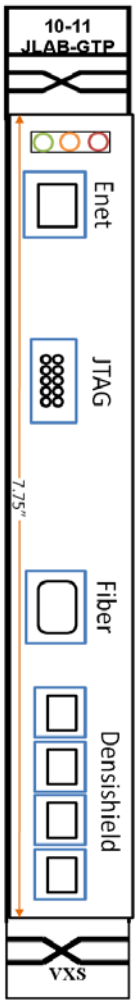
- Schematic Complete
- Layout essentially complete
- FPGA purchased and received
- Other long lead items received

Title: *Global Trigger Processor*			Jefferson Lab Fast Electronics 12000 Jefferson Avenue Newport News, VA 23606
Size: B	Number:	Revision:	
Date: 5/2/2011	Time: 8:57:38 AM	Sheet 1 of 26	
File: 01_GTP_Block_DiagramSch.Dsn			

Scott Kaneta
Jan-2011

Global Trigger Processor: (GTP)

Specification Sheet



MECHANICAL
- Single width VITA 41 Switch Module

HIGH SPEED SERIAL I/O:
From Payload Port20 (Trigger Interface module)
- 250MHz Clock (LVPECL)
- Trig1, Trig2, Sync (LVPECL)
- BUSY out (LVDS)

To Payload Ports 1-16 (SSP/spare modules)
- 2x 5 Gbps SSP Stream (Xilinx Aurora)
- LINKUP out (LVTTL)

Outputs:
- Trigger output decision time <512ns

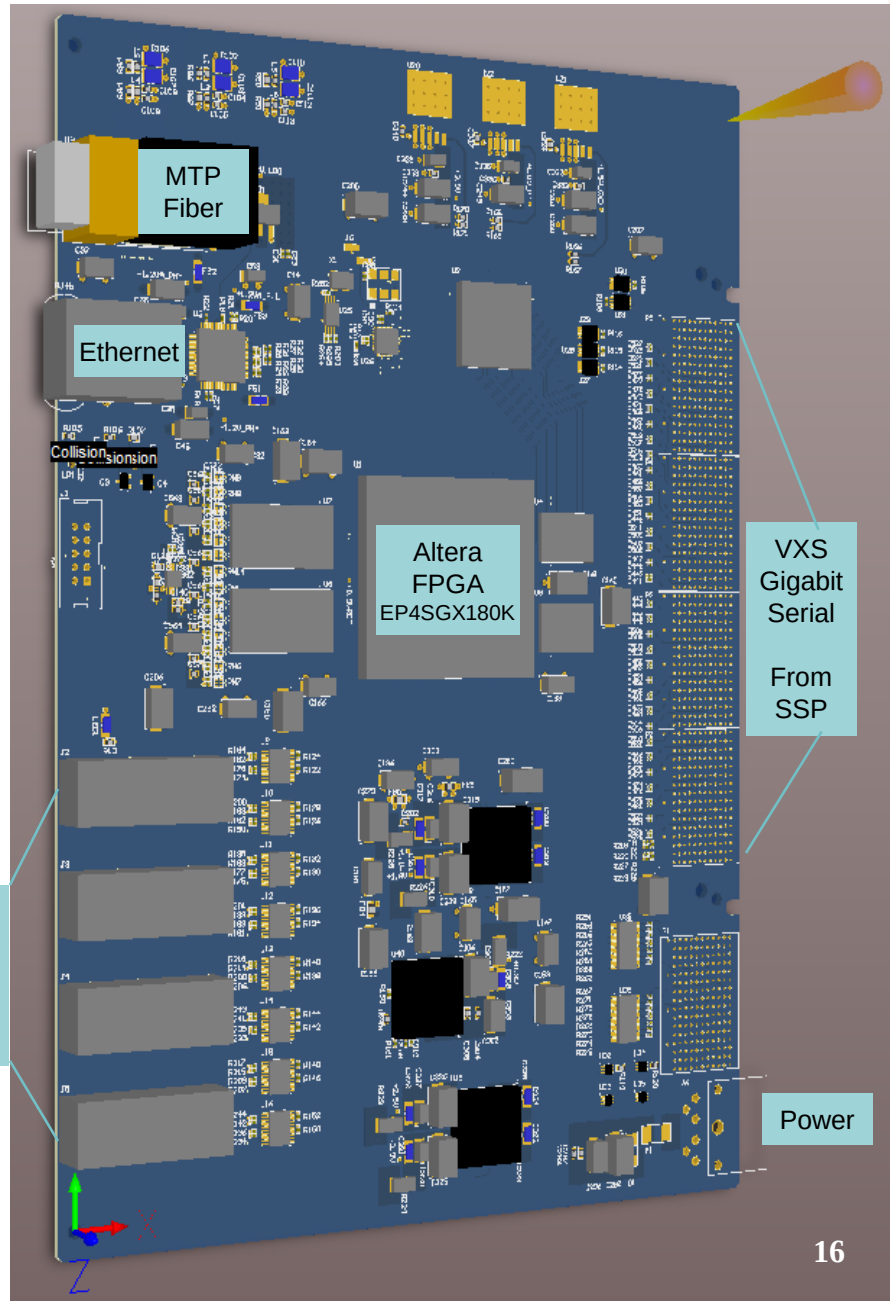
Front Panel:
- 1x RJ45: Ethernet
- 4x Densishield: Trigger Signals (LVPECL)
- 1x 4-channel Fiber Transceiver: CTP -> SSP
- 1x JTAG

Indicators: (Front Panel)
- Power OK – Green LED
- Link – Amber LED
- Alarm – Red LED

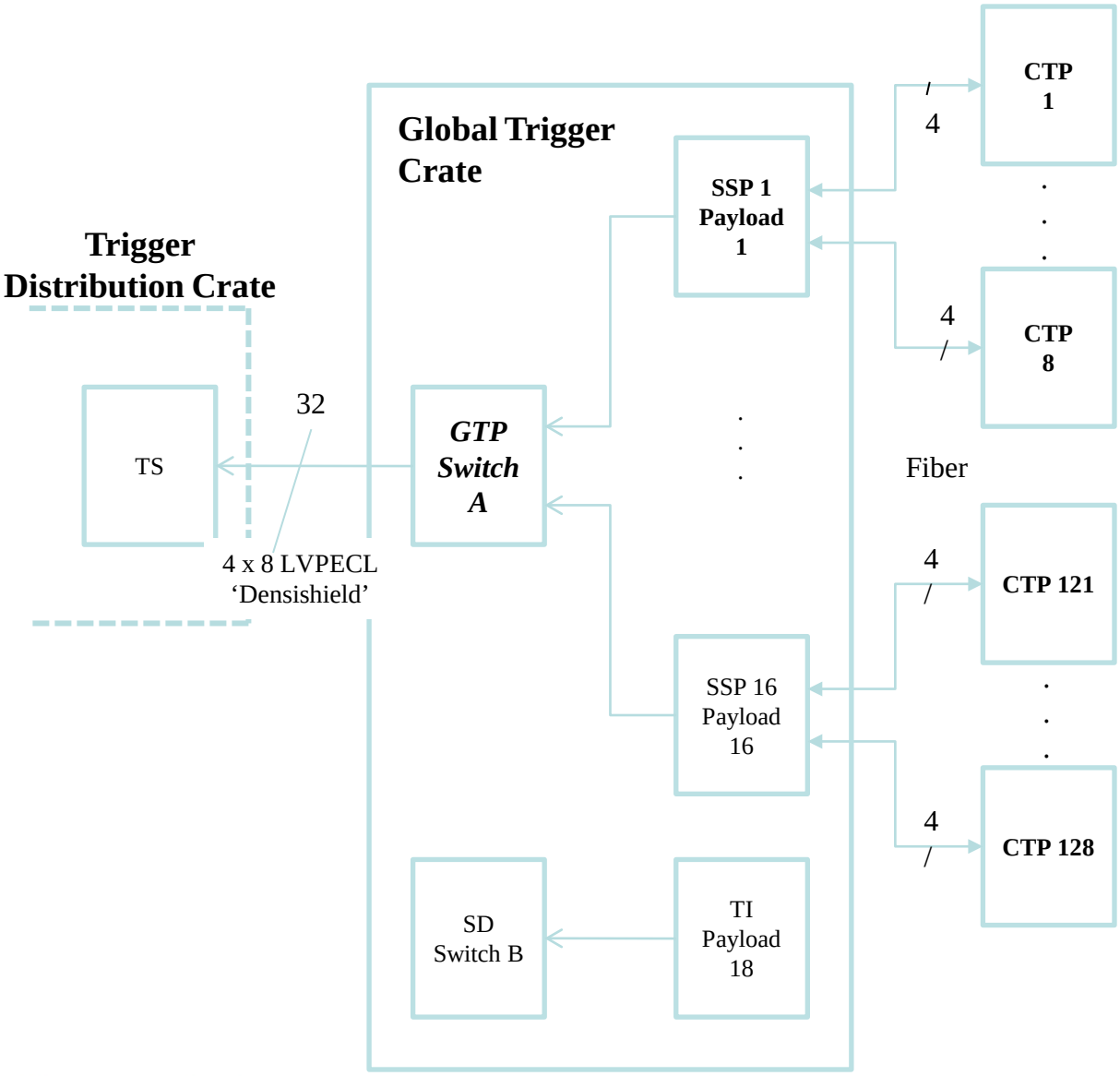
Programming:
- On board JTAG Port
- 100/1000Mbps Ethernet Interface (RJ45 connector)
- Trigger equation and processing for up to 16 JLAB SubSystem Processors

Power Requirements:
- +5v @ N Amps (From Backplane)
- Local regulators for other required voltages

Environment:
- Forced air cooling: N CFM
- Commercial grade components (Celsius)



Global Trigger - Block Diagram:

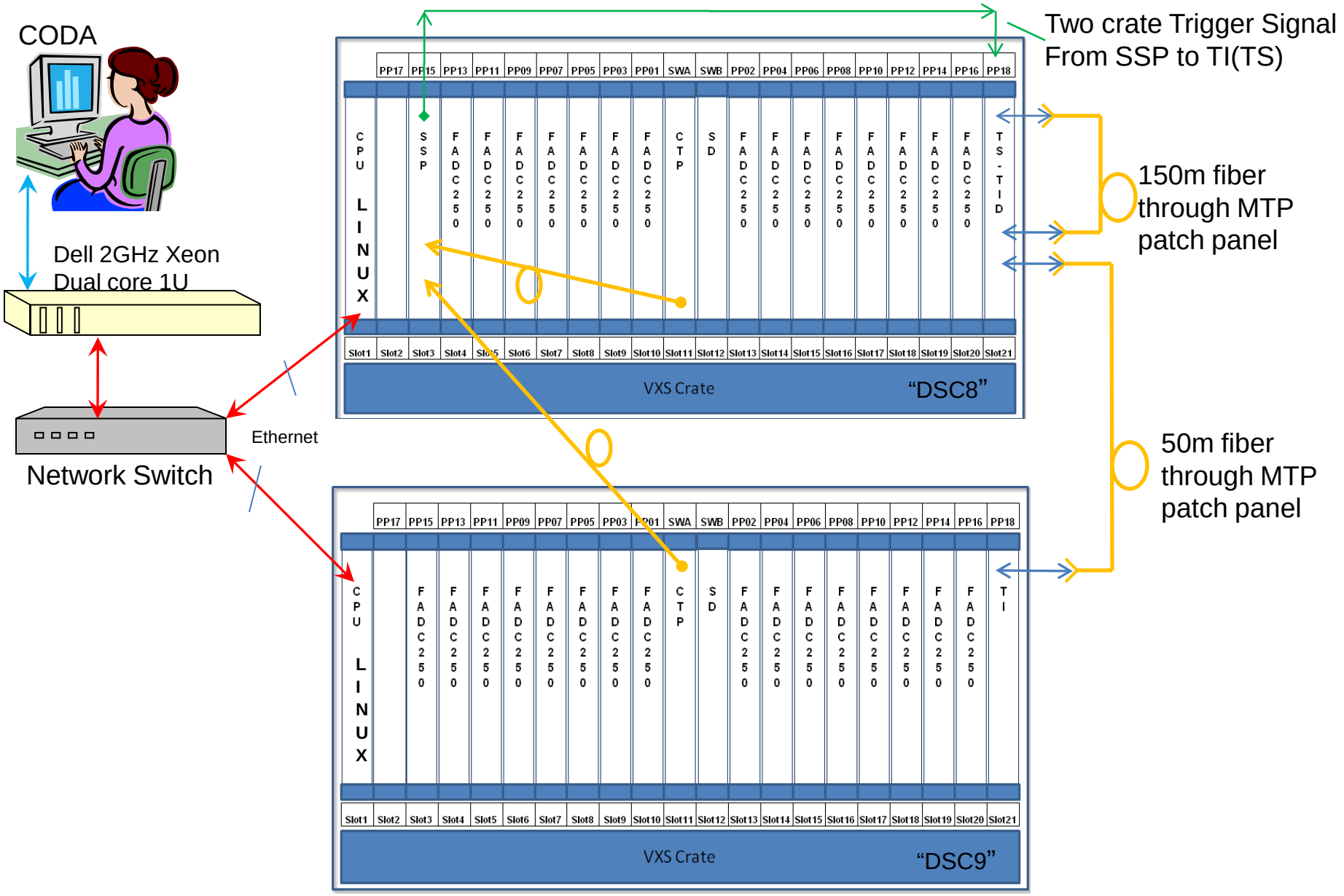


- Global Trigger Processor (GTP) receives all subsystem Level 1 data streams from SSP
- Trigger decisions made in GTP and distributed to all crates via the Trigger Distribution (TD) modules in the Trigger Supervisor Crate
- Schematics and component selection activities are progressing well
- Preliminary component placement and layout strategies have been completed
- Xilinx's 'Aurora' Gigabit protocol has been ported to Altera device successfully

Specification Status

- ***VXS and VME64x powered card enclosures***
  - ✓ Multi-year contract awarded to W-IE-NE-R, Plein & Baus, Ltd.
  - ✓ First article crates (VXS) accepted February 2011
  - ✓ 12 VME64x crates received 8-Feb-2011. Test when needed.
  - ✓ Slight delay for remainder of FY11 order
    - 16 VXS due 8-May-2011 (Original plan was 10-March)
    - 56 VXS due in FY-12 (Date To Be Determined)
    - 17 VME64x due in FY-12 (Date to Be Determined)

- ***Trigger System Fiber Optics*** (FY11 work plan)
  - System diagrams have updated for Hall D installation
  - Pre-Procurement Plan in draft form
  - Received budgetary pricing from two companies for Hall D quantities (lengths) including labor for installation and post installation testing.
  - Draft specification for parallel fiber optic cable and required peripheral components will be complete before June.
  - Hall B will use the same specification, and the quantities (lengths) will be the only difference.



Two DAQ Crate Testing: FY11

Two DAQ Crate Testing: FY11

- Activities are progressing well for the two full crate DAq test station.
- This test station is an essential infrastructure element needed to test and verify the front end and trigger hardware/software before installation in the Halls.
- After commissioning and CD4 the test stand will be vital to troubleshoot and repair the plethora of custom front end and trigger modules.
- Multiple crate 'system level' testing is imperative before approving large quantity orders.
  - Will verify Gigabit serial lanes from each slot
    - *1st Time for 16 boards/crate!!!*
  - Will measure total trigger latency
  - Will measure trigger rates/VME data rate
  - Will measure BitErrorRates
  - Will test using "Playback" mode
    - No input cables necessary

- Fully verify Trigger Interface features
- Test station used for firmware and software development
- Commissioning "tools" can be developed and tested with the front end hardware
- Minor Re-configuration of two crate test station will allow for Global Trigger module testing in the near future.
  - SSP→GTP→TS→TD

Summary

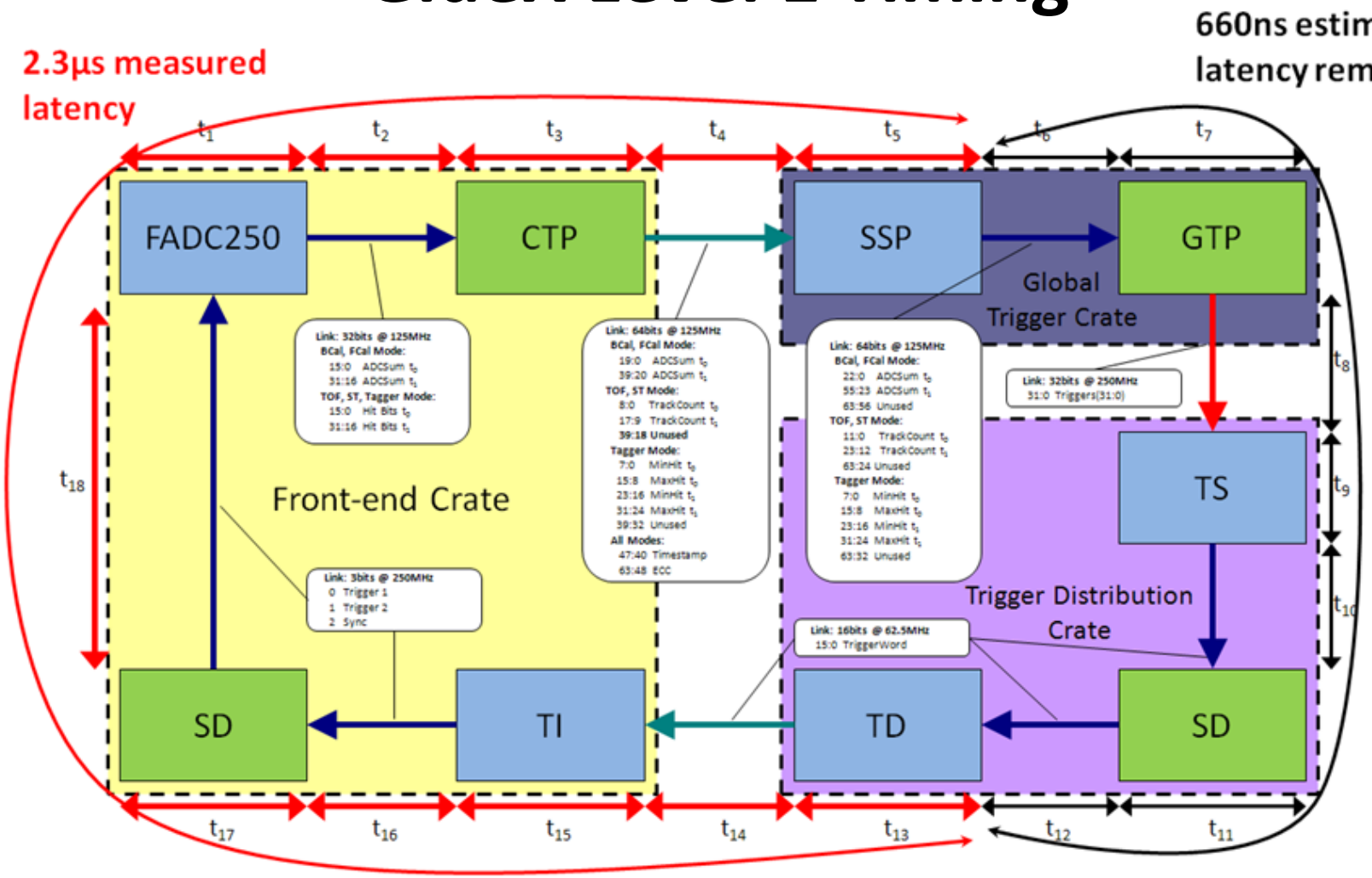
- FY11 board design project goals are on track
  - Small pre-production orders will be completed this year for TI, and SD to support detector test plans
  - Possible to order pre-production quantity for CTP and SSP by end of FY11 but immediate detector test plans do not require CTP and SSP functions
- ***Can never give enough credit to the exemplary work efforts of the design team!***
- Weekly 12GeV Trigger meeting continues to produce good discussions and implementation reports.

- Two full crate DAq testing is imminent and will produce essential test results to fully qualify the existing board designs.

Backup Slides

All sorts of good stuff

GlueX Level 1 Timing



2.3µs (measured) + 660ns (estimated) < 3µs!

Fiber Optic Link
Copper Ribbon Cable
VXS Backplane

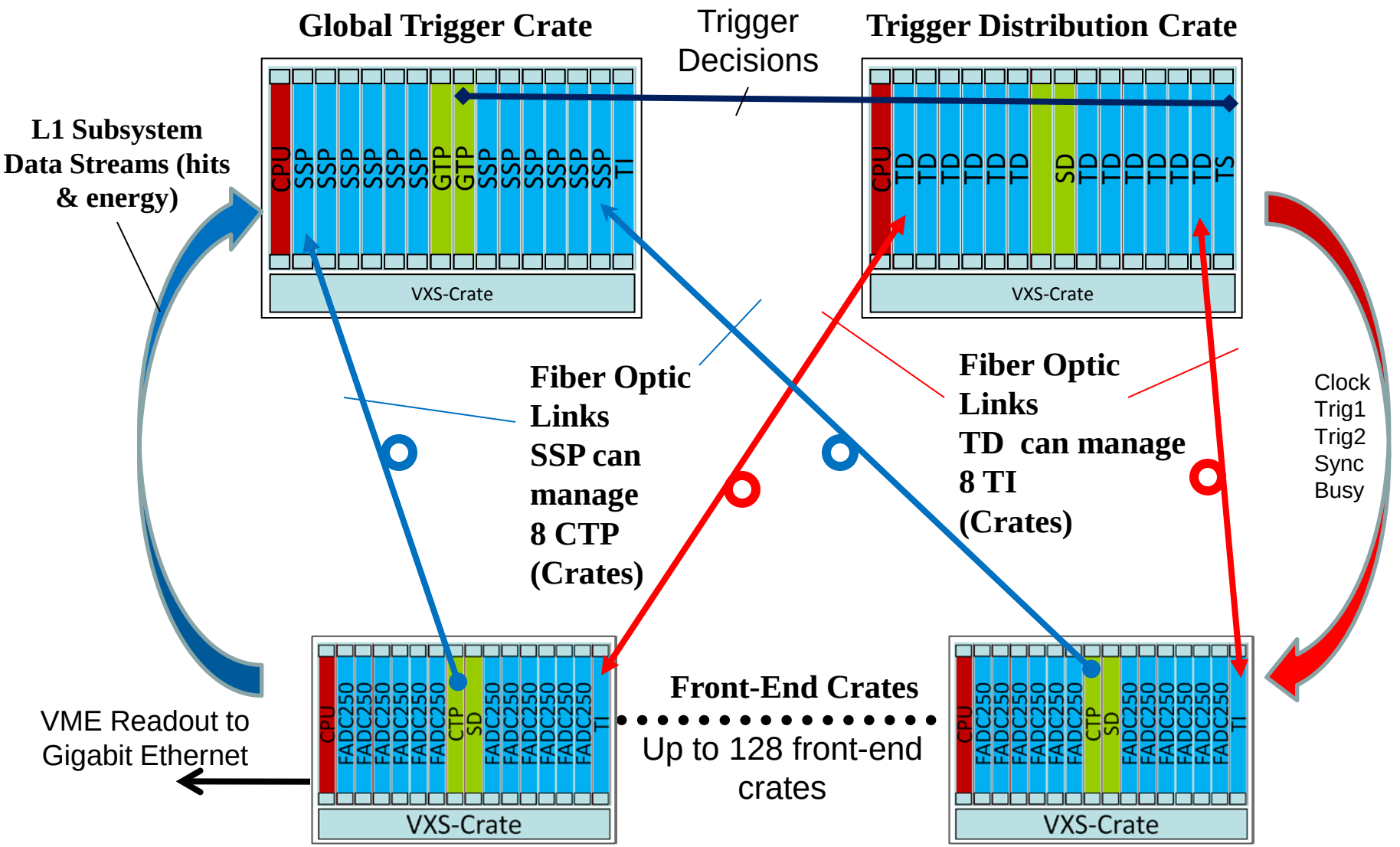
Schedules, work plans for FY11 - FY13

- FY10 design projects are at full resource pace!
  - FADC250 → Latest revision at end of FY10. TEST in FY11.
  - F1TDC-V2→ Work plan moved to FY11
  - SD → Latest revisions virtually complete. Order, assemble, TEST in FY11
  - SSP → Prototype received. Initial testing is proceeding nicely. Further testing in FY11.
  - TI-TD → Prototype(s) received. Initial testing is proceeding nicely. Firmware development and multi-crate testing in FY11
  - 16 Channel LE Discriminator/Scaler (*Hall B requirement*)
    7 'production' units under test now
  - VXS Crate Specification → Order should be awarded before Oct-10
  - GTP → Scott Kaneta joins the group! GTP slips to FY11
  - TS → Specified, and planned for FY11-FY12

- Baseline Improvement Activities (BIA) review on 17-September

- FY11 will be an intensive year of significant 'system' level testing to assure that these boards are ready for final production quantity orders in early FY12

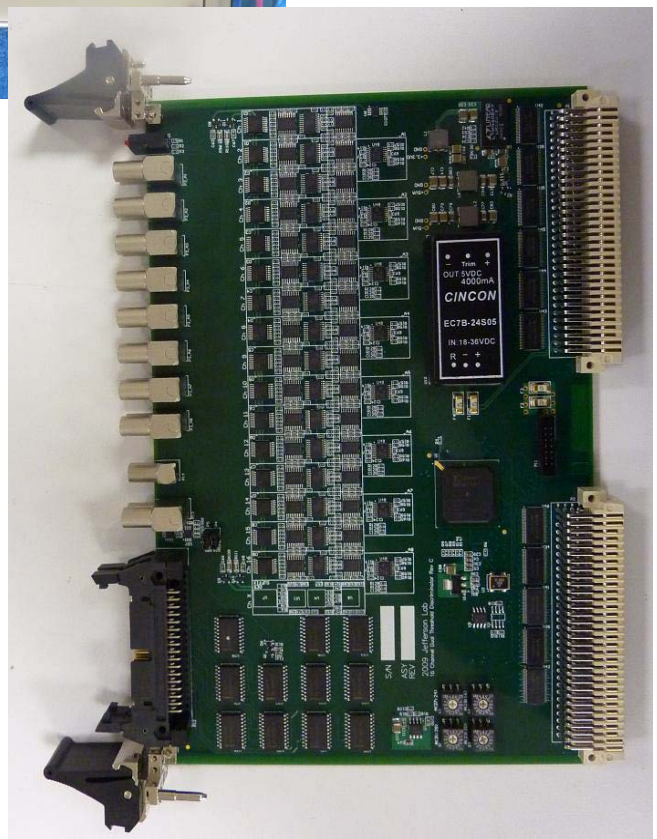
Level 1 & Trigger Distribution



Discriminator Status

(Not truly trigger system hardware, but very nice new development)

16 modules in crate



Pre-Production version
Note: VME64x connectors

- 16 Pre-Production modules have been assembled and received

- Significantly cheaper than V895:
  - -cost < $2,000

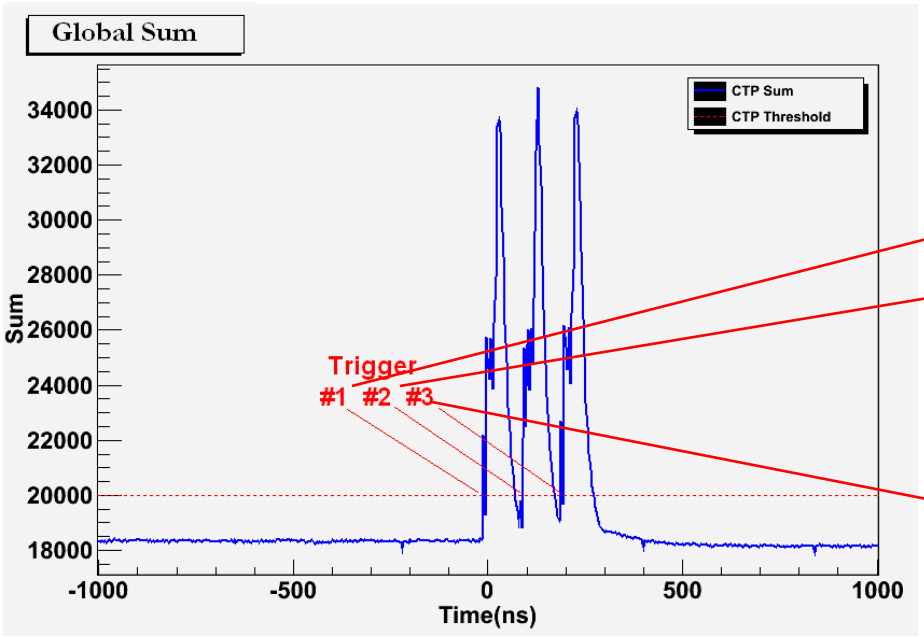
- Provides several features not found on V895:
  - -32bit scalers on all channels at both thresholds
  - -Calibrated pulse widths: from 8 to 40ns
  - -Trimmed input offset (<2mV error)
  - -Second 34pin output connector is fully programmable.
  - -Able to perform logic based on all channels at both thresholds

- Final revision has VME64x J1-J2 connector
- Full test stand developed by Pedro Toledo(USM – Chile) will be re-used
- Hall Groups will test with detectors

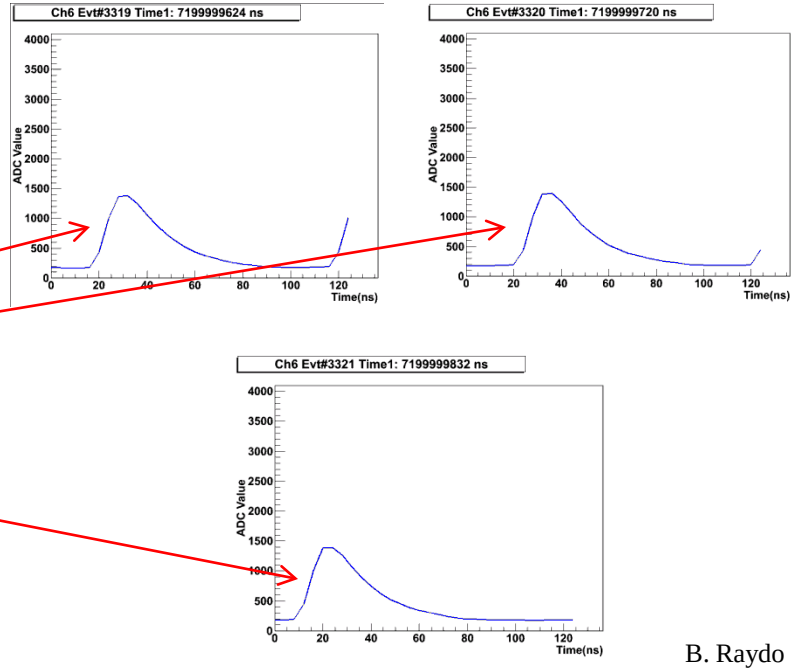
Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2µs global sum window is recorded around the trigger to see how the trigger was formed:



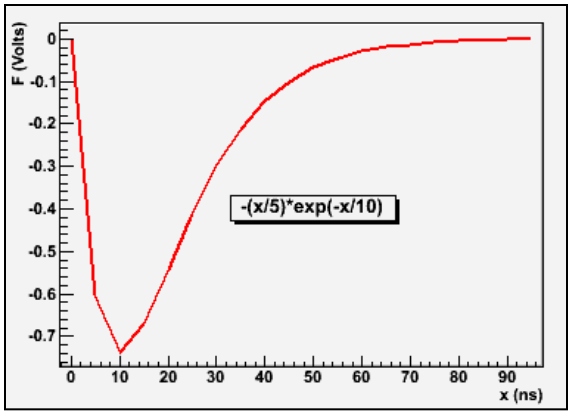
Example Raw Event Data for 1 FADC Channel:



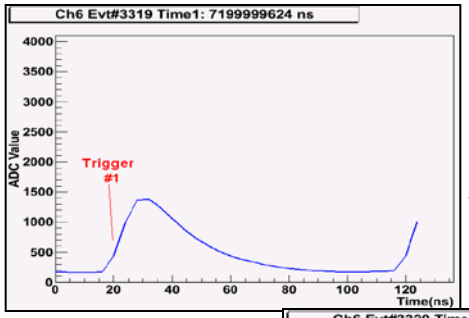
B. Raydo

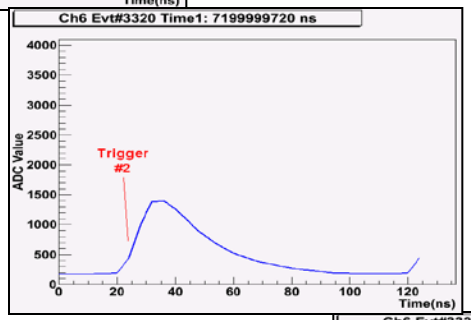
2 Crate Energy Sum Testing

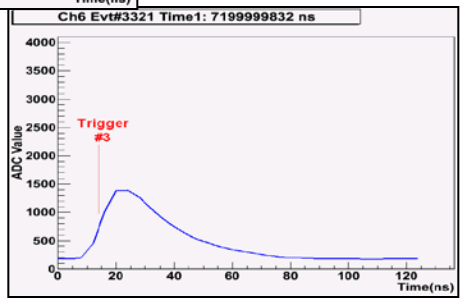
Input Signal to 16 FADC250 Channels:



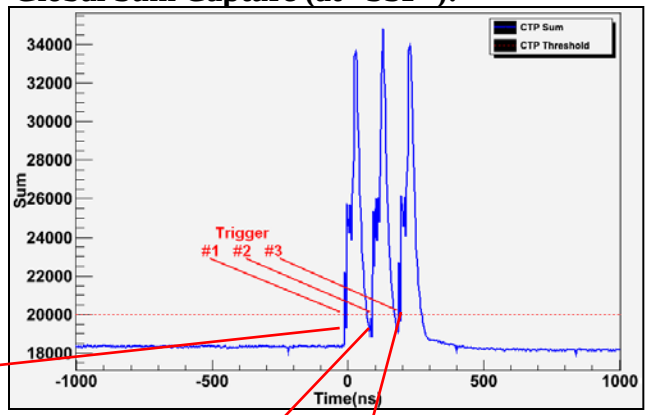
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- **Threshold applied to global sum (96 digitized channels) produces 3 triggers.**
- **Raw channel samples extracted from pipeline shown for 1 channel.**
- **Runs at 250kHz in charge mode**
- ***Latency: 2.3μs(measured) + 660ns(GTP estimate) < 3μs***

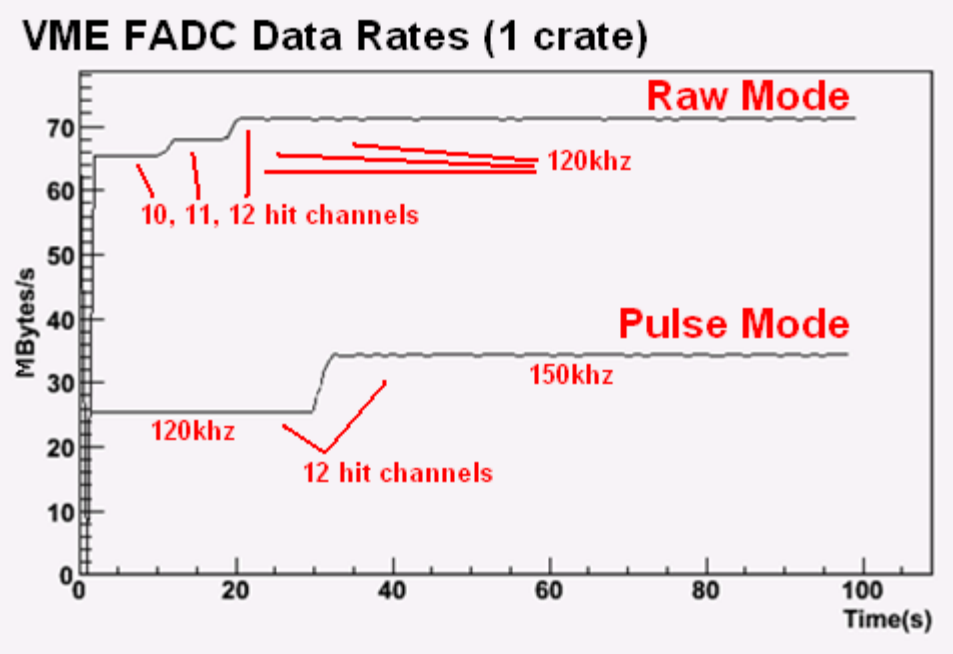
B. Raydo

Synchronized Multi-Crate Readout Rates

• FADC event synchronization has been stable for several billion events @ ~150kHz trigger rate.

• Have run up to 140kHz trigger rate in raw window mode, up to 170kHz in Pulse/Time mode.

• Ed Jastrzembski has completed the 2eSST VME Interface on FADC allowing ~200MB/s readout



Single Crate
12 signals distributed to four FADC250

18% Occupancy

B. Raydo