Prototype of the Global Trigger Processor

GlueX Collaboration

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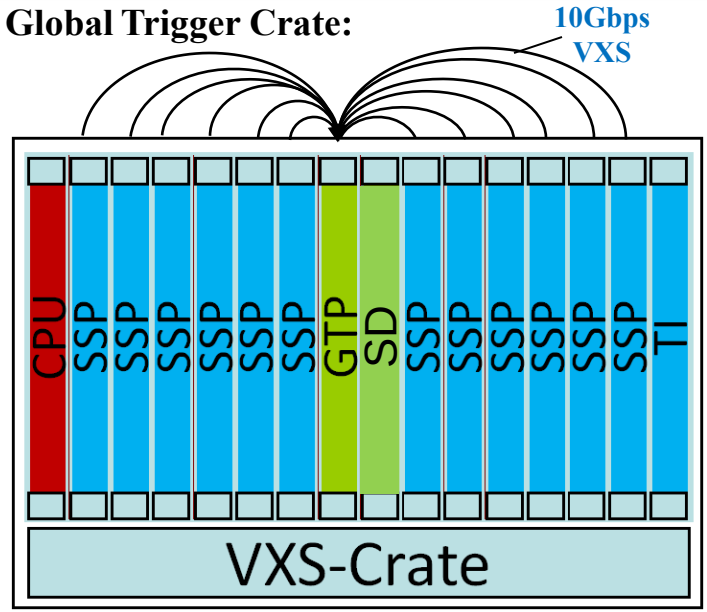
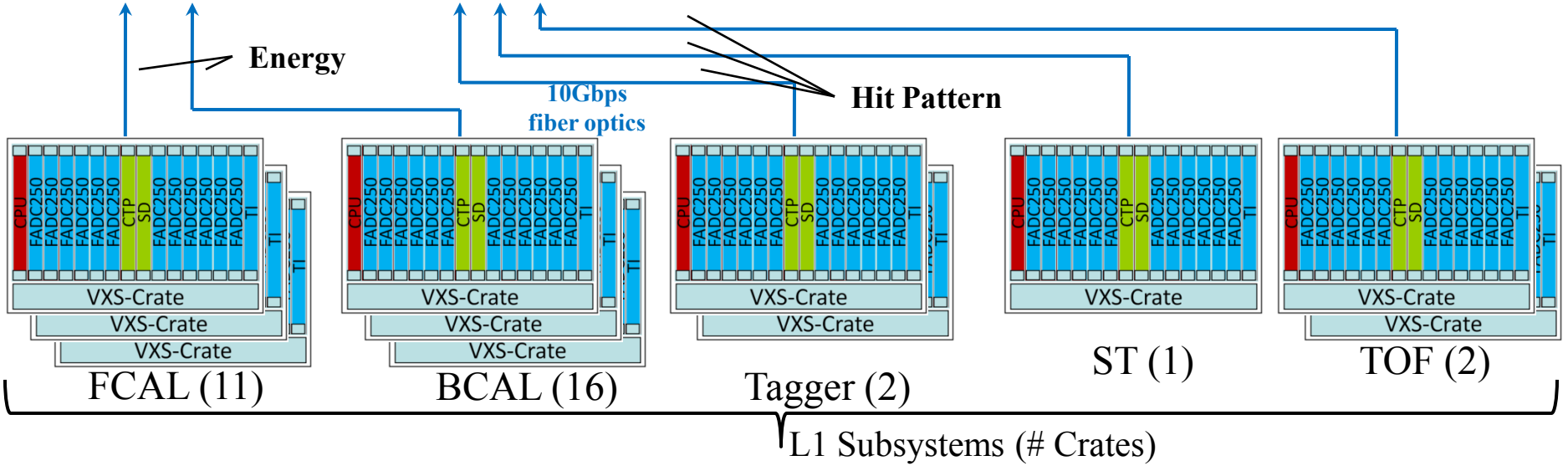
Presentation Outline

- Level 1 Trigger Architecture Overview
- GTP Hardware
  - Specification
  - Block Diagram
  - Prototype
- GTP Prototype Status
- Trigger Equations

Level 1 Trigger Architecture



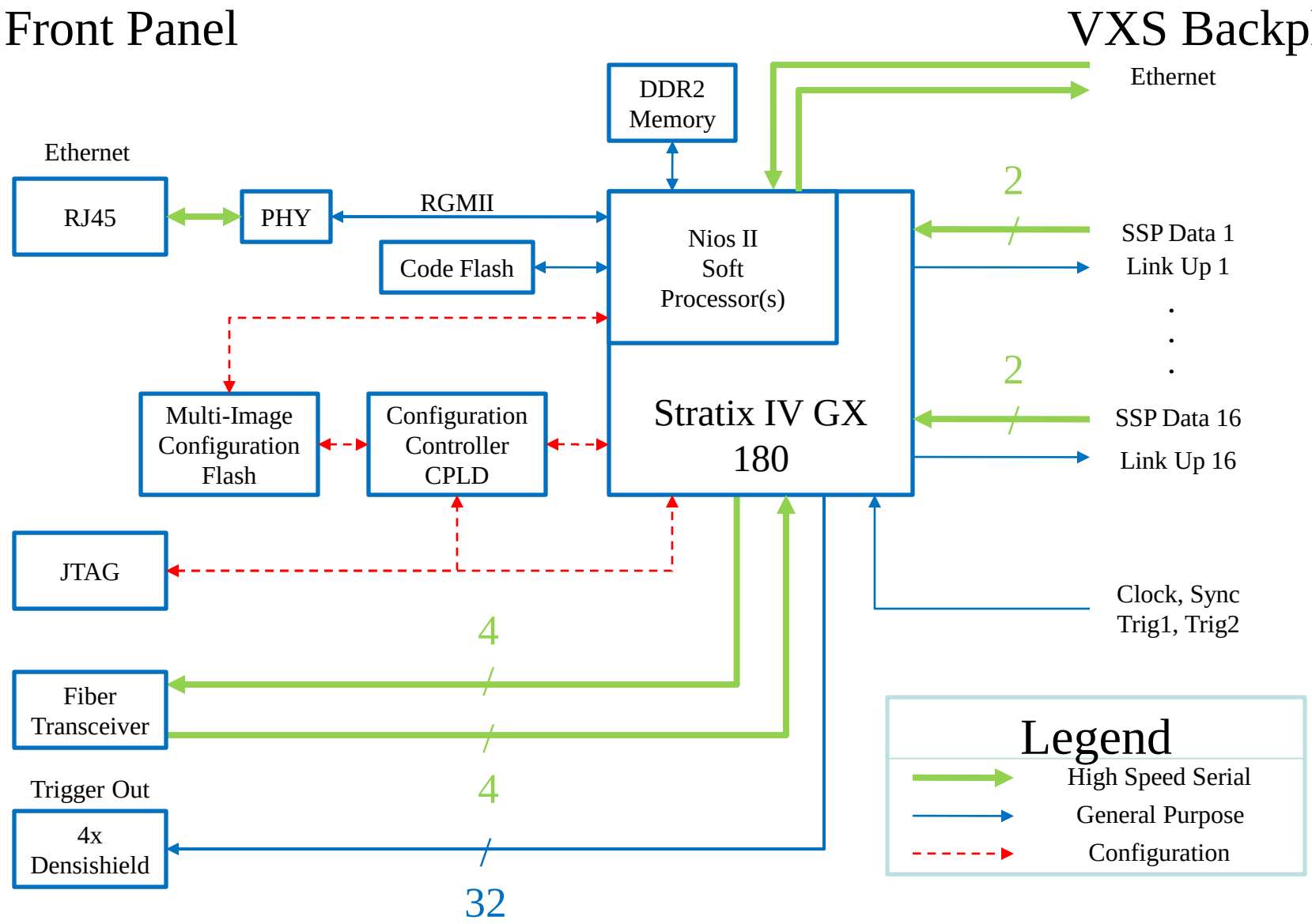
- Switch A in Global Trigger Crate
- Trigger Distribution not shown



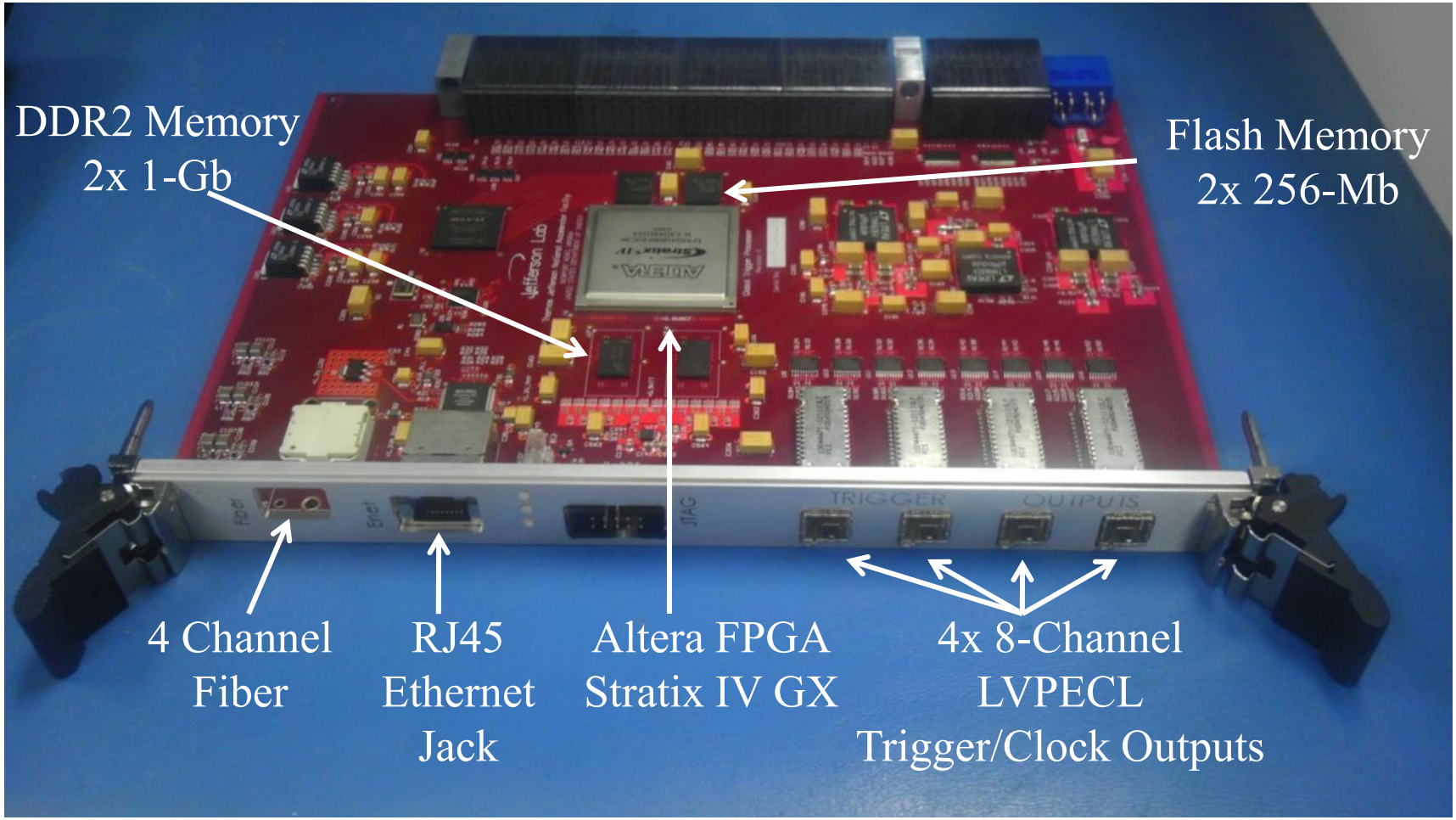
GTP Hardware Specification

- Altera Stratix IV GX 180
  - Pin compatible expansion up to 530k logic elements ($)
- Support for up to 16 VXS payloads
  - 2x 5-Gbps links per payload
- 32 LVPECL trigger/clock outputs to TS
- 4 channel full duplex Fiber transceiver
- 2 Gb DDR2 Memory
  - Two independent 1-Gb Interfaces
- 512 Mb Flash Memory
  - 256 Mb dedication for configuration
  - 256 Mb for code or other
- 10/100/1000 Ethernet Interface on Front Panel

GTP Hardware Block Diagram



GTP Prototype



Prototype Evaluation Status

Test	Initial	Moderate	Extensive	Done	Notes
Power	X	X	X		Complete except testing specifications under realistic load
Clocking	X	X			Local oscillators only
Transceivers	X	X			Pass 5 Gbps from SSP on some slots, need to test all lanes
Flash	X	X			R/W config flash from CPLD, Toolkit evaluation of code flash
Configuration	X	X			Non-volatile configuration from flash
DDR2	X	X			EMIF Toolkit Evaluation
Trigger Out	X	X			Tested with test board, TS testing in upcoming Global Crate test
Ethernet	X	X			ARP and Ping functional using VHDL TCP/IP Stack and MAC
Fiber					Evaluation has not yet begun

Ethernet Testing

- ARP and Ping fully verify hardware
  - VHDL TCP/IP stack
- Significant work required for usable interface

667	3107.993190	Dell_90:1e:d5	Broadcast	ARP	42 Who has 172.16.1.128? Tell 172.16.1.5
668	3107.993259	3com_03:04:05	Dell_90:1e:d5	ARP	60 172.16.1.128 is at 00:01:02:03:04:05
669	3107.993270	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=51/13056, ttl=128
670	3107.993342	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=51/13056, ttl=128
671	3109.024664	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=52/13312, ttl=128
672	3109.024718	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=52/13312, ttl=128
673	3110.038523	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=53/13568, ttl=128
674	3110.038577	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=53/13568, ttl=128
675	3111.052566	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=54/13824, ttl=128
676	3111.052626	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=54/13824, ttl=128
677	3112.066761	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=55/14080, ttl=128
678	3112.066816	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=55/14080, ttl=128
679	3113.080584	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=56/14336, ttl=128
680	3113.080655	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=56/14336, ttl=128
681	3114.094456	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=57/14592, ttl=128
682	3114.094511	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=57/14592, ttl=128
683	3115.108563	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=58/14848, ttl=128
684	3115.108617	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=58/14848, ttl=128
685	3116.122547	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=59/15104, ttl=128
686	3116.122604	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=59/15104, ttl=128
687	3117.136539	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=60/15360, ttl=128
688	3117.136601	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=60/15360, ttl=128
689	3118.150463	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=61/15616, ttl=128
690	3118.150516	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=61/15616, ttl=128
691	3119.164460	172.16.1.5	172.16.1.128	ICMP	74 Echo (ping) request id=0x0001, seq=62/15872, ttl=128
692	3119.164514	172.16.1.128	172.16.1.5	ICMP	74 Echo (ping) reply id=0x0001, seq=62/15872, ttl=128

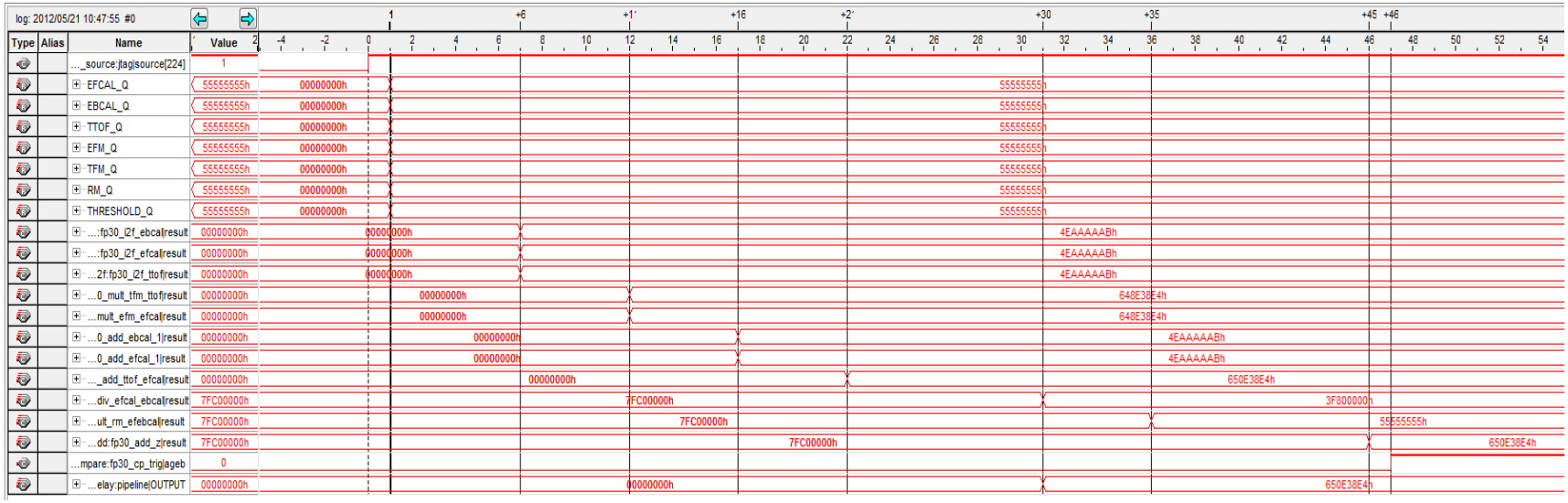
```
⊞ Frame 672: 74 bytes on wire (592 bits), 74 bytes captured (592 bits)
⊟ Ethernet II, Src: 3com_03:04:05 (00:01:02:03:04:05), Dst: Dell_90:1e:d5 (b8:ac:6f:90:1e:d5)
  ⊞ Destination: Dell_90:1e:d5 (b8:ac:6f:90:1e:d5)
  ⊞ Source: 3com_03:04:05 (00:01:02:03:04:05)
    Type: IP (0x0800)
⊞ Internet Protocol Version 4, Src: 172.16.1.128 (172.16.1.128), Dst: 172.16.1.5 (172.16.1.5)
⊟ Internet Control Message Protocol
    Type: 0 (Echo (ping) reply)
    Code: 0
    Checksum: 0x5527 [correct]
    Identifier (BE): 1 (0x0001)
    Identifier (LE): 256 (0x0100)
    Sequence number (BE): 52 (0x0034)
    Sequence number (LE): 13312 (0x3400)
    [Response To: 671]
    [Response Time: 0.054 ms]
  ⊟ Data (32 bytes)
      Data: 6162636465666768696a6b6c6d6e6f707172737475767761...
      [Length: 32]
```

GTP Equations

- From Dave Doughty's presentation January 2008
- Z >= TFM*TTOF + EFM*EFCal + RM*((EFCal +1)/(EBCal + 1))
  - TTOF - Tracks Forward TOF
  - EFCal - Energy Forward Calorimeter
  - EBCal - Energy Barrel Calorimeter
- Modified from Ben's implementation for Stratix IV
  - ~2% of FPGA resources
- Looking for feedback regarding equations
  - User modification of equations
  - FPGA density
- Multiple configurations if necessary

GTP Equation

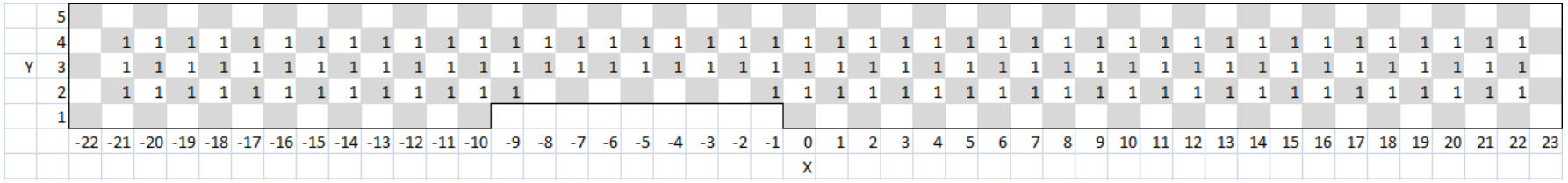
```
-- Stage 1 (6 cycles): Convert Ints=>Floats
fp30_i2f_efcal: fp_i2f port map(dataa => EFCAL_Q, clock => CLK, result => EFCAL_f);                                  -- latency = 6,  total = 6
fp30_i2f_ebcal: fp_i2f port map(dataa => EBCAL_Q, clock => CLK, result => EBCAL_f);                                  -- latency = 6,  total = 6
fp30_i2f_ttof: fp_i2f port map(dataa => TTOF_Q, clock => CLK, result => TTOF_f);                                     -- latency = 6,  total = 6

-- Stage 2: Simplify Stage 1 (TFM*TTOF + EFM*EFCAL + RM*(EFCAL+1)/(EBCAL+1) => TTOF_SC+EFCAL_SC+RM*EFCAL_ADD1/EBCAL_ADD1)
fp30_mult_tfm_ttof: fp_mult port map(dataa => TFM_Q, datab => TTOF_f, clock => CLK, result => TTOF_SC);             -- latency = 5,  total = 11
fp30_mult_efm_efcal: fp_mult port map(dataa => EFM_Q, datab => EFCAL_f, clock => CLK, result => EFCAL_SC);           -- latency = 5,  total = 11
fp30_add_efcal_1: fp_add port map(dataa => EFCAL_f, datab => x"00000001", clock => CLK, result => EFCAL_ADD1);       -- latency = 10,  total = 16
fp30_add_ebcal_1: fp_add port map(dataa => EBCAL_f, datab => x"00000001", clock => CLK, result => EBCAL_ADD1);       -- latency = 10,  total = 16

-- Stage 3: Simplify Stage 2 (TTOF_SC+EFCAL_SC+RM*EFCAL_ADD1/EBCAL_ADD1 => TTOF_EFCAL_SUM+RM*EFCAL_EBCAL_DIV)
fp30_add_ttof_efcal: fp_add port map(dataa => TTOF_SC, datab => EFCAL_SC, clock => CLK, result => TTOF_EFCAL_SUM);  -- latency = 10,  total = 21
fp30_div_efcal_ebcal: fp_div port map(dataa => EFCAL_ADD1, datab => EBCAL_ADD1, clock => CLK, result => EFCAL_EBCAL_DIV);  -- latency = 14, total = 30

-- Stage 4: Simplify Stage 3 (TTOF_EFCAL_SUM+RM*EFCAL_EBCAL_DIV => TTOF_EFCAL_SUM_DLY + EFCAL_EBCAL_SC)
fp30_mult_rm_efebcal: fp_mult port map(dataa => EFCAL_EBCAL_DIV, datab => RM_Q, clock => CLK, result => EFCAL_EBCAL_SC);  -- latency = 5,  total = 35
pipeline : pipeline_delay GENERIC MAP(delay => 9,port_width => 32) PORT MAP(CLOCK => CLK, INPUT => TTOF_EFCAL_SUM, OUTPUT => TTOF_EFCAL_SUM_DLY);


-- Stage 5: Simplify Stage 4 (TTOF_EFCAL_SUM_DLY + EFCAL_EBCAL_SC => Z_SUM)
fp30_add_z: fp_add port map(dataa => EFCAL_EBCAL_SC, datab => TTOF_EFCAL_SUM_DLY, clock => CLK, result => Z_SUM);  -- latency = 10,  total = 45

-- Stage 6: Test for Trigger
fp30_cp_trig: fp_compare port map(dataa => Z_SUM, datab => THRESHOLD_Q, clock => CLK, ageb => TRIGGER_i);           -- latency = 1,  total = 46
```



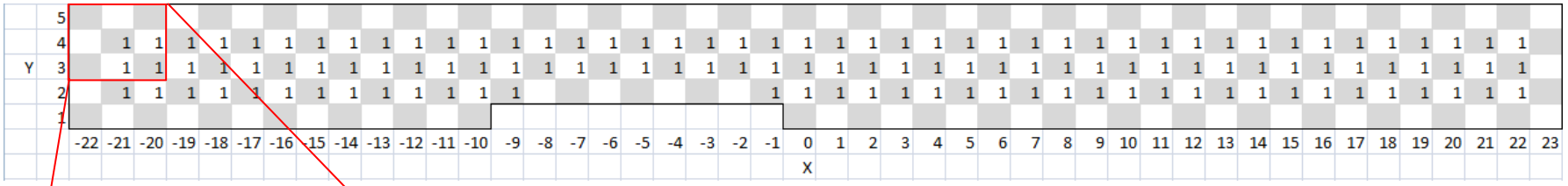
Trigger Applications

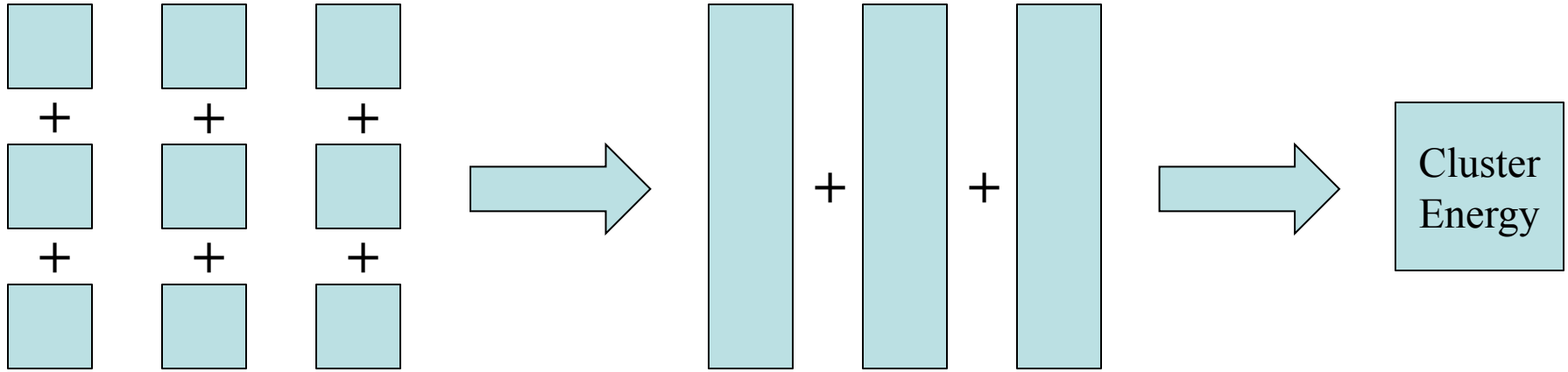
- Heavy Photon Search test run
  - Cluster finding in ECal using CTP
  - Sliding 3x3 window of crystal energies

- Calorimeter
  - 221 channels
  - 125 cluster processors



Cluster Finding Algorithm





Cluster Finding Design

- Targeted Xilinx Virtex 5 LX110T
- Significant timing issues
  - Design pushes limit of this FPGA
- Some features not implemented
  - Control of the number of crystals per cluster
  - Scalar reporting