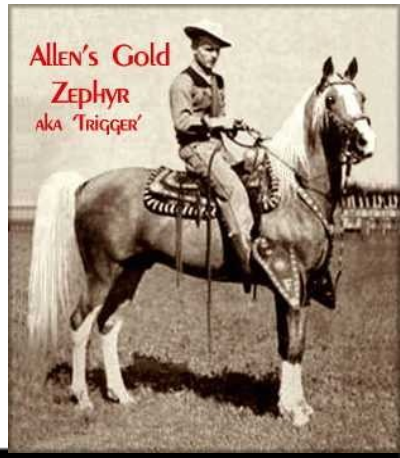
GlueX Collaboration Meeting

February 21 - 23, 2013

12GeV Trigger Electronics

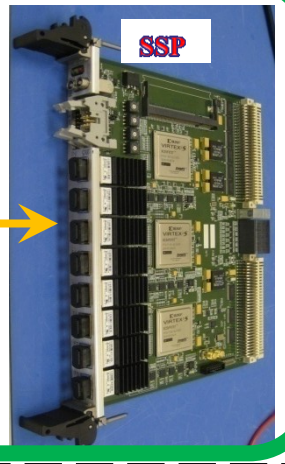
R. Chris Cuevas

1. Hardware Design Status Updates
   - Production News
   - Status
2. DAq and Trigger Testing
   - Global Trigger Hardware Update
3. Summary



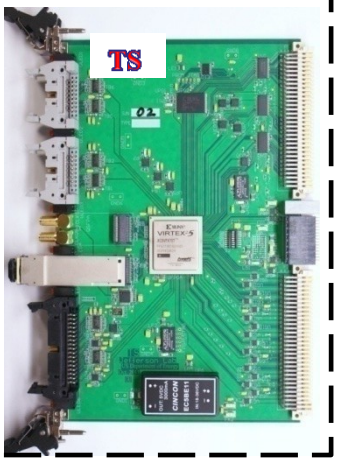
Trigger Modules In Production

L1 Trigger 'Data'
MTP Ribbon Fiber



Global Trigger Crate
- Sub-System Processor
- Global Trigger Processor

Trigger 'Link" Control
Clock, Sync
MTP Ribbon Fiber



Front End Crate
- FADC250, (FADC125), (F1TDC)
- Crate Trigger Processor
- Signal Distribution
- Trigger Interface

Trigger Control/Synchronization
- Trigger Supervisor
- Trigger Distribution

Trigger Hardware Status

- **S**ignal **D**istribution (**SD**)
  - All production modules have been delivered!
    - Nick Nganga has updated the final firmware to include:
      - Remote FPGA firmware download
      - Serial Number storage
- Acceptance test routine development will be used for long term maintenance
- Software (CODA) library routines complete and included with Full Crate Acceptance Testing (FCAT) – Bryan Moffit

- ✓ SD provides precision low jitter fan-out of 250MHz system clock, trigger and synch signals over VXS backplane to VXS payload modules
- ✓ Latest SD version includes clock jitter attenuation PLL
- ✓ Successfully used 2 SD boards during HPS experiment

Trigger Hardware Status

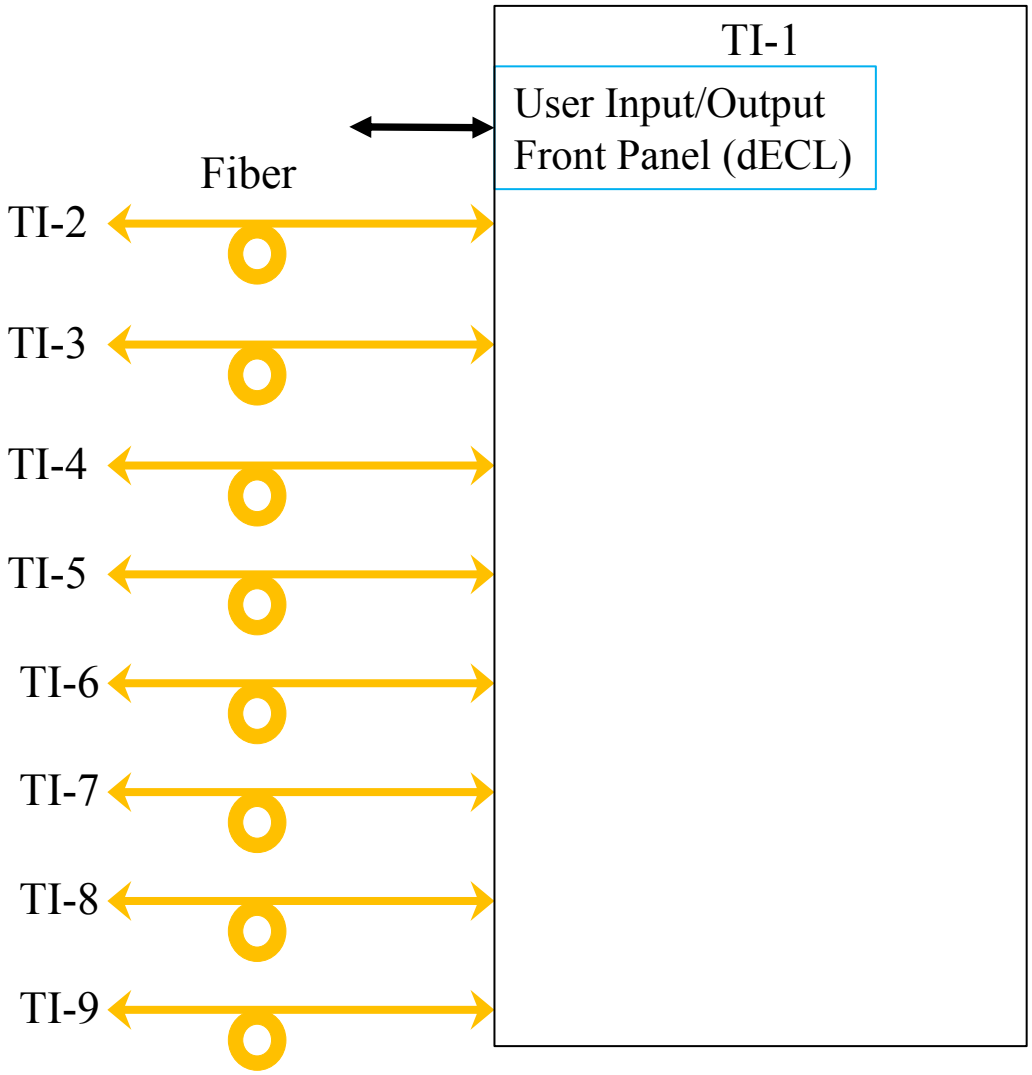
- **TI** – **TD** **T**rigger **I**nterface – **T**rigger **D**istribution
  - All production modules have been delivered!

  (Includes TI and TD boards)
    - William has updated the final firmware
      - New functions to handle high speed data from switch slots have been developed. (50Mb/s link)
        - Implementation plans in progress
        - Provides a high speed alternative to I^2C
- Acceptance test routine development will be used for long term maintenance
- Software (CODA) library routines complete and included with Full Crate Acceptance Testing (FCAT)

✓ User I/O is available at front Panel of TI
- ECL level; Use for pulsers, or other detector requirements

✓ **Single TI can function as "TS" for multiple crate (9) configuration**

TI operating in TS mode



- Trigger Interface module can be configured to control up to **9 front end crates**
- This method allows for local control of a detector Sub-system.
- TI needs to be configured for this mode with multiple FO Transceivers
- Local control of CLOCK, SYNC, and Trigger signals
- Global Trigger system signals NOT available
- Perfect for initial testing of Detector sub-systems. (FCAL, BCAL)

Trigger Hardware Status

- ❖ **F**lash **ADC** 250Msps (**FADC250**)
  - ✓ *- See Fernando's update*
  - ✓ FCAT verification software updated – B. Moffit
  - ✓ Production board delivery to JLAB groups is virtually complete

- **C**rate **T**rigger **P**rocessor (**CTP**)

Hai Dong
Jeff Wilson

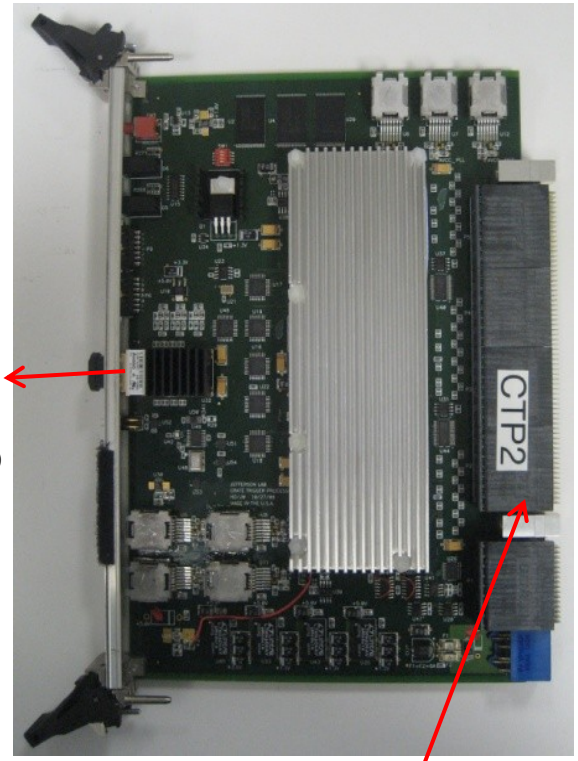
  - Hall D production quantities (32) awarded to MTEQ in Virginia!
  - Fabrication and assembly files transmitted this week
    - Upgrading to largest/fastest Virtex 5 FPGA
      - Will support 5Gb/s transfer speed with FADC250
      - Will provide additional FPGA resources for future L1 algorithms
      - Cost for highest grade included for production boards
  - Delivery in May-2013
  - ✓ Successful operation with HPS calorimeter beam test with latest cluster finding algorithm!!
  - ✓ Sixteen FADC250 boards successfully tested in full crate @2.5Gb/s!
  - ✓ Successful test with two crate system at full 200KHz trigger rate!!

Crate Trigger Processor

Hai Dong
Jeff Wilson

MTP Parallel Optics

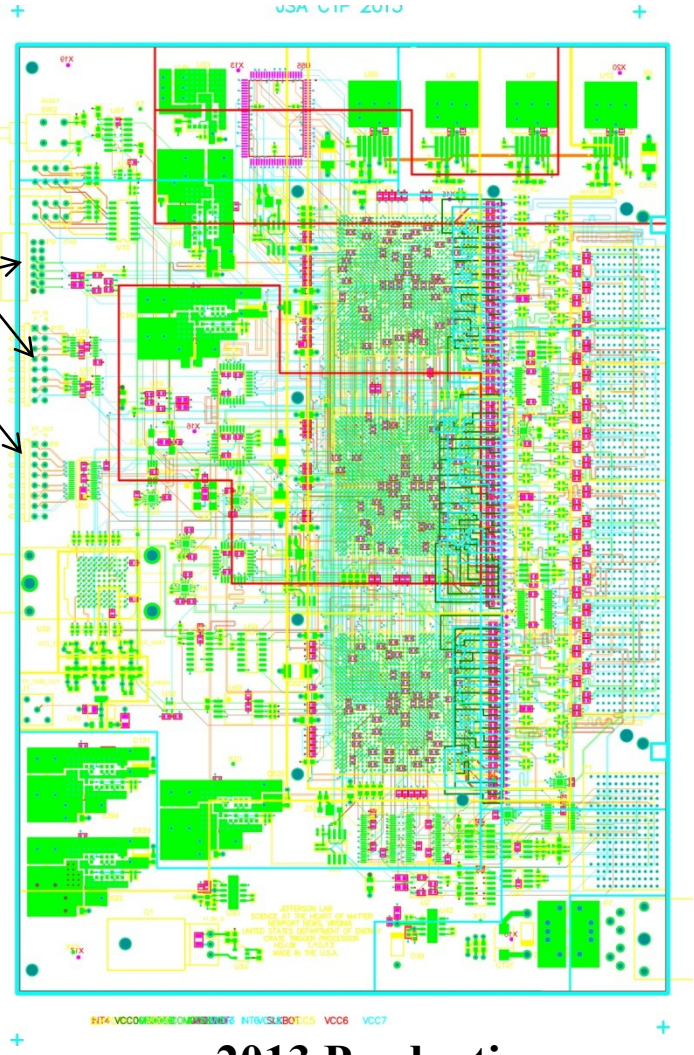
10Gb/s to SSP



CTP Prototype

VXS Connectors Collect serial data from 16 FADC-250 *(64Gb/s)*

New Front Panel I/O



2013 Production CTP

Crate Trigger Processor

- 4 Fully functional prototypes have provided a great deal of development and testing many different CTP trigger algorithm developments.

- Production version will support higher serial speeds. (5Gb/s/'lane') Matches V5-FX70T on FADC250, and cost for highest grade Virtex V FPGA is included on production boards.

- Production version will include front panel I/O (LVDS)

- Production version will include VXS connection to Cpu slot (PPT-17) for development of PCIe interface if needed. Present control/monitoring is via I^2C through Trigger Interface.

- Level 1 algorithm for Tagger hit pattern needs to be developed.
- Algorithm for full crate energy sum is stable.

- Computed crate-level energy sum value sent via 10Gb/s fiber optics to Global Trigger Crate (32bits every 4ns)

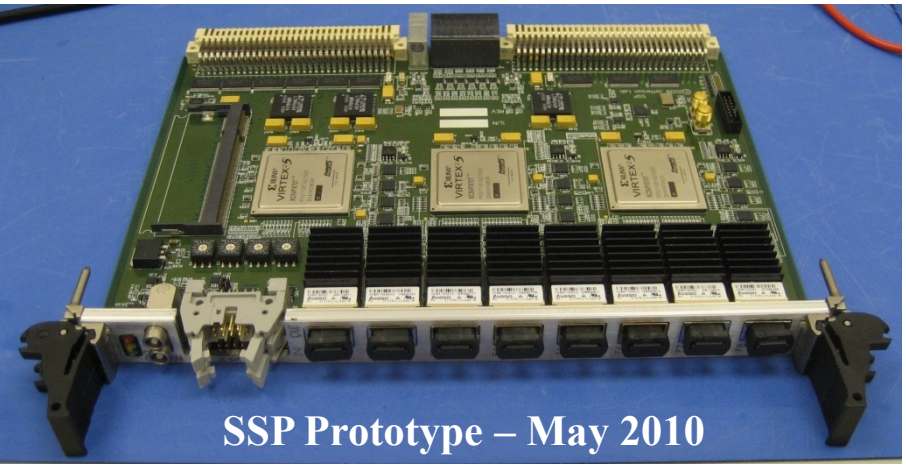
Trigger Hardware Status

- **S**ub**S**ystem **P**rocessor (**SSP**)
  - All production boards have been delivered.
  - Production contract included:
    - 10 Hall D
    - 15 Hall B
    - 1 each for Halls A & C
  - Acceptance testing is progressing and Ben's test code will be retained for long term maintenance/development.
  - New FO Transceivers (QSFP) on production boards
  - ✓ *SSP has been successfully tested with two crate HPS beam test run*
  - ✓ SSP to GTP serial link definitions have been fully specified and implemented for VXS
  - ✓ Initial testing of SSP (Xilinx) => GTP (Altera) Gigabit transceivers is successful
  - Manages trigger information from up to 8 front end crates.
    (2048 channels!)
  - Trigger data received from up to 8 front panel fiber transceivers
  - 20Gb/s input *capability* per transceiver (4 lanes @6.25Gbp/s*(8/10b))

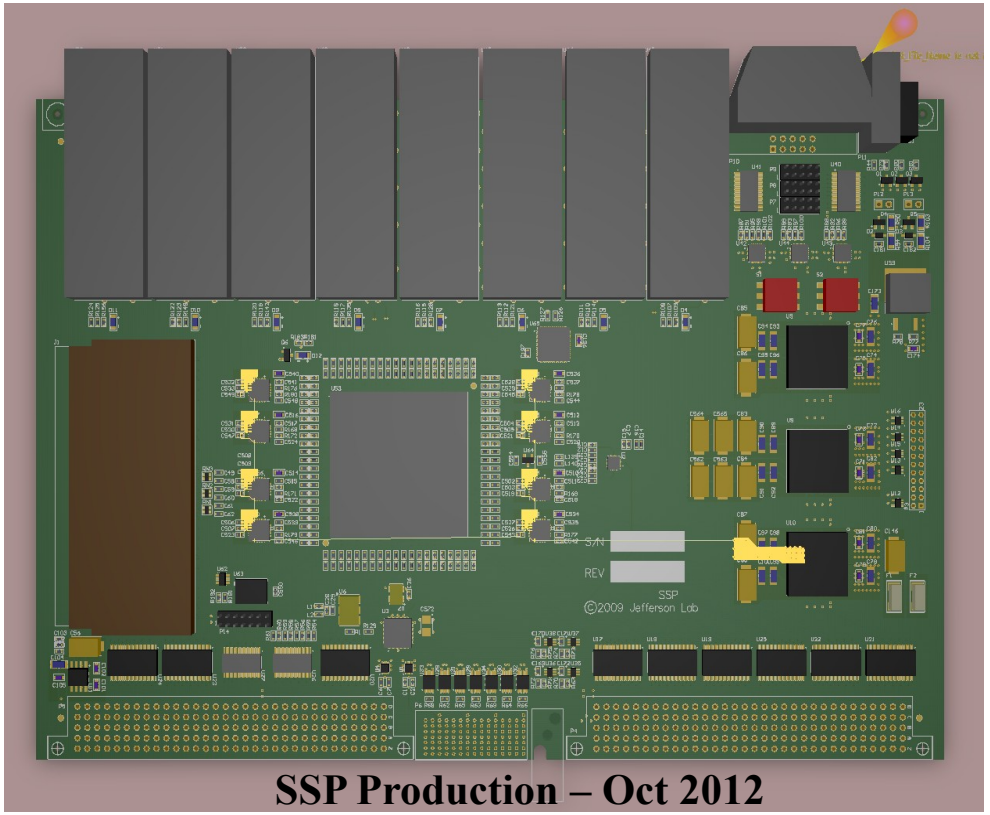
Sub-System Processor Status

Ben Raydo

Used successfully for HPS experiment!



SSP Prototype – May 2010

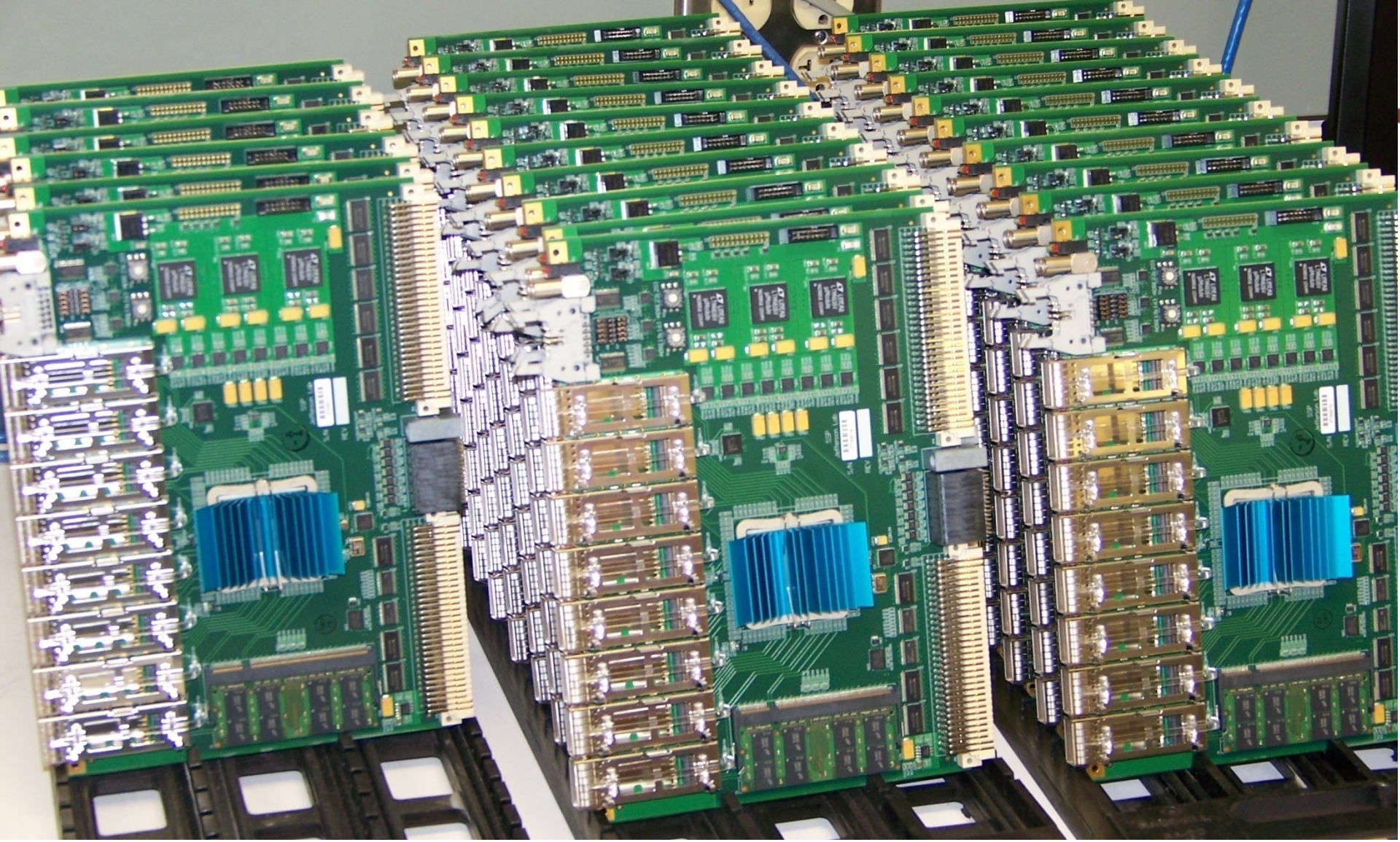


SSP Production – Oct 2012

Production Status:

1) Schematics & BOM complete
→ Single FPGA Virtex 5 TX150T
→ New Fiber Transceivers
  -- Support 10Gb/s (4 'Lanes')
  -- Significant cost savings ($40K)

A. Assembly contract awarded
B. Gerbers are ~75% complete, expecting delivery to vendor by Oct 1st.
C. Parts for 1st article arrive Oct 17, 2012…1st article shipment around end of October.



Production Sub-System Processor (SSP) Boards
Delivered 4-Feb-2013
All Halls

Trigger Hardware Status

Scott Kaneta

- **G**lobal **T**rigger **P**rocessor (**GTP**) (FY – 11/12)
  - ✓ 2 Pre-production GTP modules have been fabricated, assembled and tested.
  - ✓ Interface requirements to SSP and TS have been finalized and tested
  - ✓ The GTP transceivers (Altera) have been tested with the SSP at 5Gb/s.

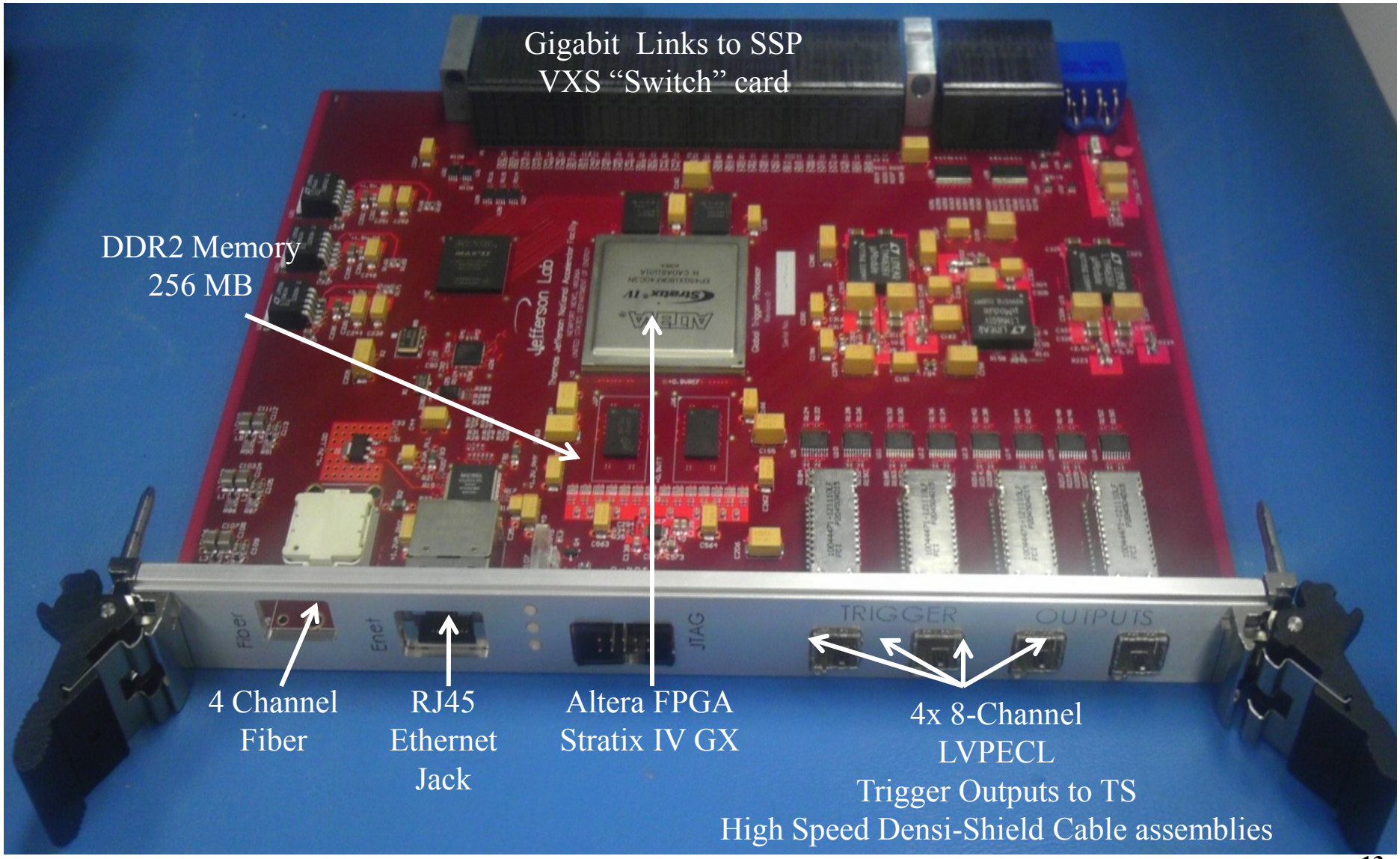
Firmware development and verification activities:

- Ethernet interface implemented successfully
  -- GUI interface using Root in development
- Implementation of final Physics Trigger equations
- Full test of Global Trigger Crate has been a significant effort
  - See Scott Kaneta's talk

- Final fabrication files for production boards ready now.
- Prepare for turnkey order soon
  - On track for Hall D

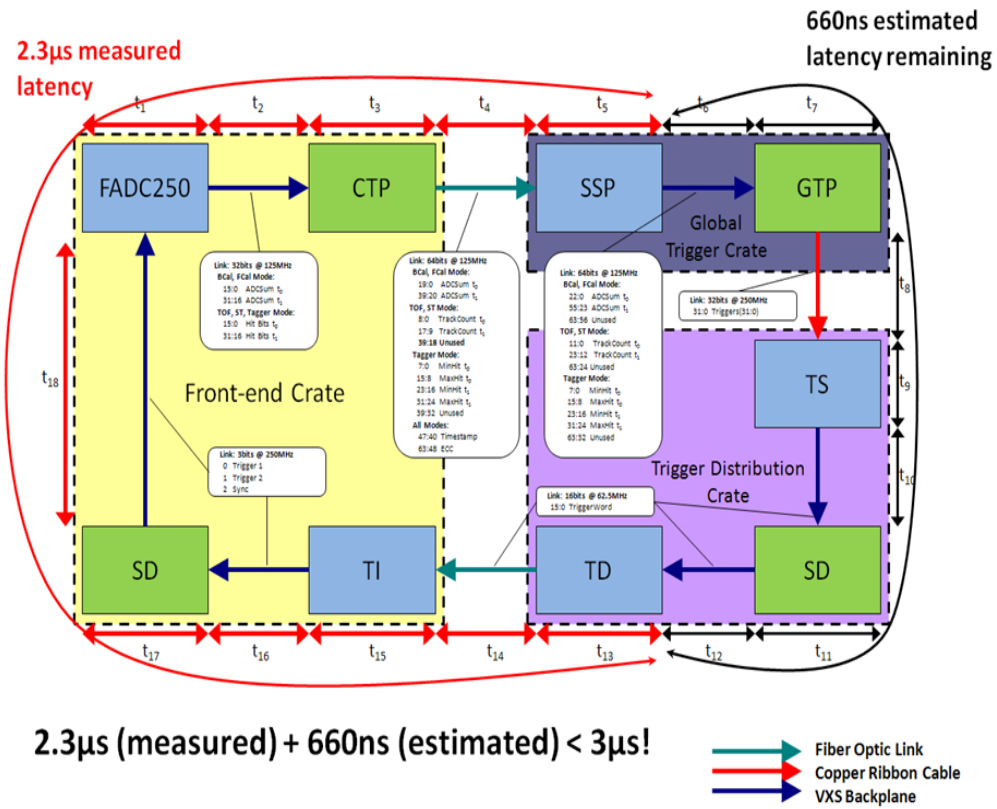
GLOBAL TRIGGER PROCESSOR
(2 Pre-production boards)

S. Kaneta



Global Crate Hardware Testing

Scott Kaneta
Ben Raydo
William Gu



Global Trigger crate/module testing progressing,,, (Scott will talk next)

- Cables from GTP to TS have been received and tested.
  - Densi-shield 8 pair x 4
  - 32 Trigger 'bits' NOT serialized to eliminate latency.

- SSP→GTP→TS→TD → TI
  - Verify full trigger system latency
  - Fully qualify SSP → GTP VXS Gigabit transmission
  - Fully qualify GTP → TS interface
  - Measure latency with different global equations
  - Overall latency must be <3.2us
  - Trigger equation development
  - Develop GTP Ethernet User Interface

Trigger Hardware Status

- **T**rigger **S**upervisor (**TS**) (FY-11/12/13 activity)
  - ✓ Two (2) Pre-production boards have been thoroughly tested
  - ✓ 1st article production version has been sent for fabrication and assembly.
  - ✓ Final CODA library drivers in development

  - Functional hardware verification with Trigger Distribution (TD) boards complete.
  - Testing with GTP module is ongoing, and virtually all functions/interfaces have been verified.
  - Production order will proceed after 1st article test
    - Total of 8 TS for ***ALL*** Halls (2 per Hall includes 1 spare)

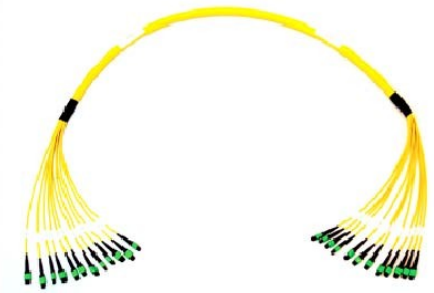
  - New board format from legacy era – VXS Payload module
  - Distributes precision clock, triggers, and sync to front end crates via the Trigger Distribution modules.
  - Manages global triggers and ReadOut Controller events
  - **G**lobal **T**rigger **P**rocessor drives 32 bit trigger word to TS over copper cables (Densi-Shield LVPECL)

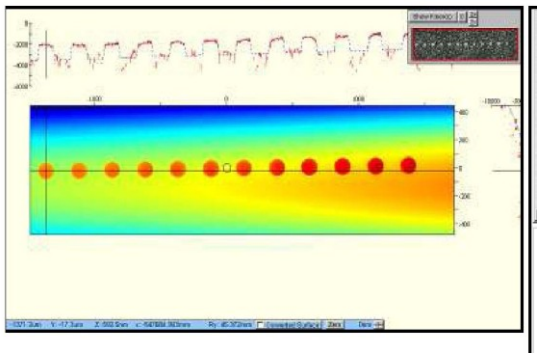
Specification Status

- ***VXS and VME64x powered card enclosures***
  - ✓ Multi-year contract awarded to W-IE-NE-R, Plein & Baus, Ltd.
  - ✓ First article crates (VXS) accepted February 2011
  - ✓ FY11 order is complete
  - ✓ FY12-13 order delivered in December, 2012
    - ALL crates for ALL Halls: Complete
    -- One backplane replaced. 2 DIN connectors reversed!

- ***Trigger System Fiber Optics*** (Q1 or Q2 – FY13 procurement)
  - System diagrams have updated for Hall D and Hall B installation
  - MTP fiber patch panels/cables received for Halls D, B, and C.

    →Final Trigger Fiber trunk lengths for Hall D & B contingent on cable tray installation





Summary

- ***12GeV Trigger Module productions are progressing nicely!***
- Final firmware for several of the trigger modules will need development
  - → Tagger “Hit Counts”
  - → SSP and GTP Global Trigger functions
  - → Final TS firmware/functions
- Plans to test Gigabit VXS transmission @5Gb/s per ‘lane’ (i.e. SSP->GTP)
- Valuable run experience with new 12GeV pipeline electronics
- Acceptance testing activities are progressing well for DAQ and Trigger modules
- Full Crate Acceptance Test (FCAT) station is developed for FADC250s
  - Verification of Gigabit serial plus other essential common VXS signaling.
- Essential CODA library development has been completed
  - New advanced trigger algorithms successfully implemented
- Check out 12GeV Trigger hardware progress:
https://halldweb1.jlab.org/wiki/index.php/Electronics_Trigger_Meetings
- ***Plenty of challenges remain but GREAT progress and accomplishments!***

Backup Slides

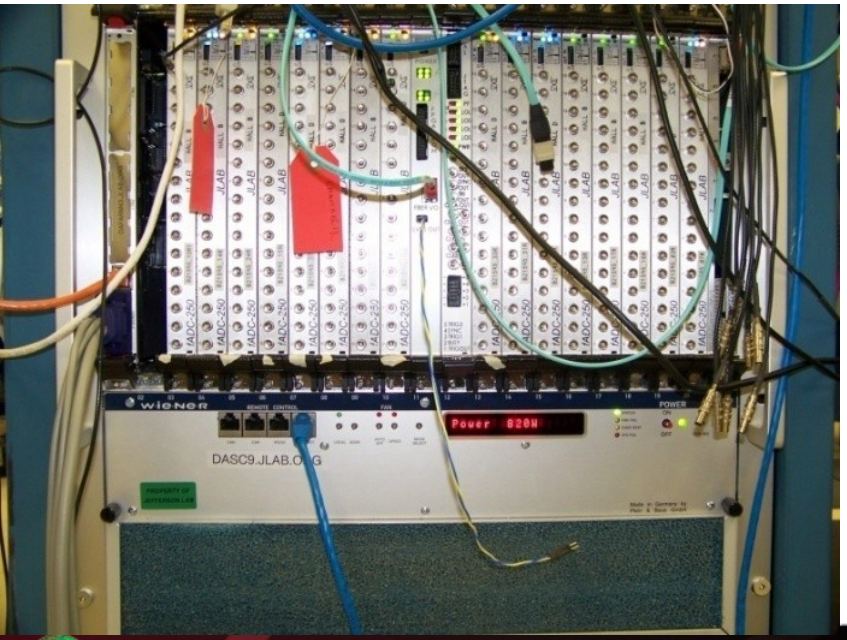
All sorts of cool stuff

Bryan Moffit
Et al.

Full DAq Crate Testing Plans

- Before deploying full crates with all required modules:
  - Will test using “Playback” mode and CODA
  - No input cables necessary; User defined signals loaded in front-end FPGA
  - Deterministic test for all channels and Gigabit serial lane alignment check
  - Verify TI → SD → Payload Board Synchronization and Clock
  - **Re-Use these tools for Hall commissioning effort**

- Test station used for FINAL firmware verification and software ‘library’ development
  - Bryan Moffit has created a preliminary plan and list of test functions
  - See wiki link → https://halldweb1.jlab.org/wiki/index.php/Full_Crate_Acceptance



This full crate test station in EEL109 is an essential infrastructure element needed to test and verify the front end and trigger hardware/software before installation in the Halls.

Discriminator/Scaler

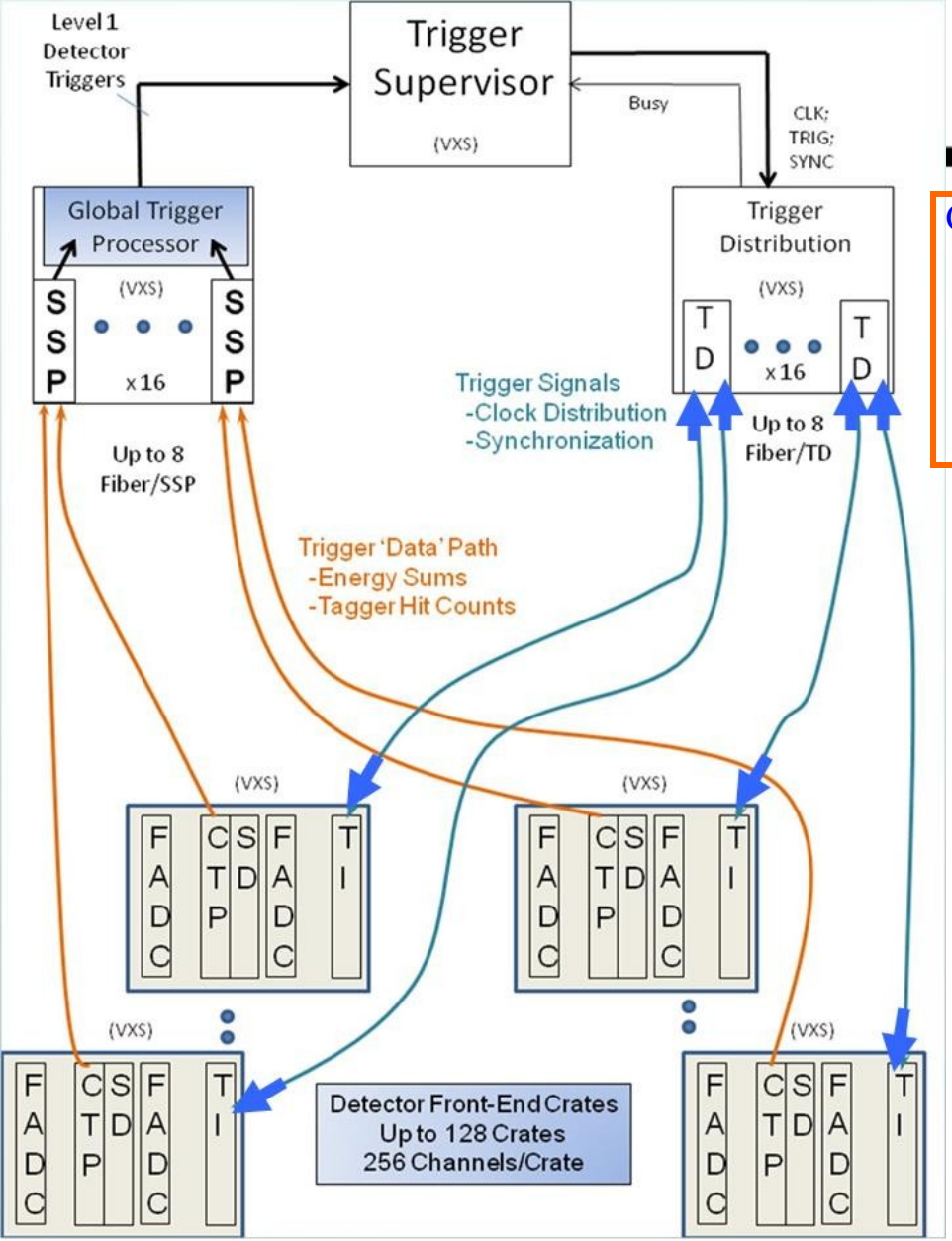
Ben Raydo

Production Status:

1) Design complete (schematics, pcb, firmware, test stand)
2) ACDI Awarded contract for ~375 units
3) First article + ~200 units have arrived and been tested
4) Assembly yield so far is:
   - 4 boards with bad component (~2%)
     - 3 boards with bad CINCON switching powers supply module
     - 1 board with bad MC100EP91
   - 2 boards assembly defect (~1%)
     - 1st defect was very first unit (probed too much causing a short)
     - 2nd defect was a bent IC pin

These failures were easily repaired.
- CINCON switching power supply failure is a concern
- Failure analysis is ongoing with CINCON, but burn-in testing of ~200 units has showed no additional failures.

System Description



CTP -> SSP -> GTP
L1 Trig_Data
Uni_Directional

Energy Sums

TS -> TD -> TI
Link
1.25Gb/s
Bi-Directional

BUSY
Trigger Sync
Trig_Comnd

Trigger
Supervisor
(Distribution)

Global Trigger
Processing
Sub-System Processing
(Multi-Crate)

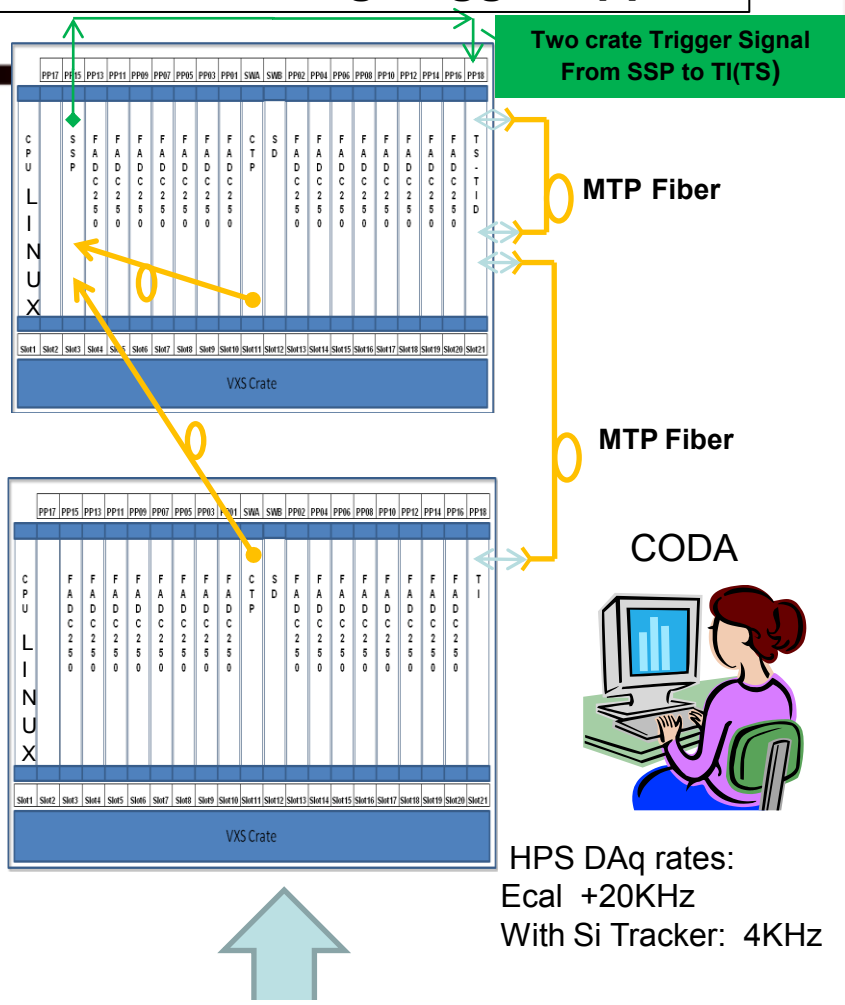
Crate Trigger Processing

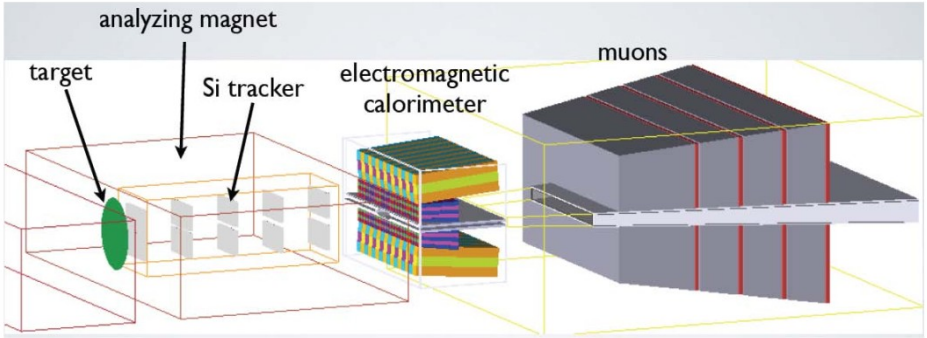
Flash ADC Modules

Detector Signals

Successful HPS Beam Test with New 12GeV Cluster Finding Trigger App

- HPS Test Run in Hall B used two full VXS crates
- 432 APD channels → 27 FADC250
- Cluster finding algorithm in Crate Trigger Processor -- Pushing the resource limit!
- New firmware to encode individual channel sums
- CTP firmware will report cluster centroid to SSP
- SSP will create trigger from CTP output
- Exploits the use of the 4Gb/s VXS bandwidth from each FADC250 module
- New technique to report signal threshold crossing with 4ns resolution and 5bit amplitude for every channel
- Experiment shows that Hall D L1 Energy Sum algorithm for Calorimetry will clearly 'fit' into CTP



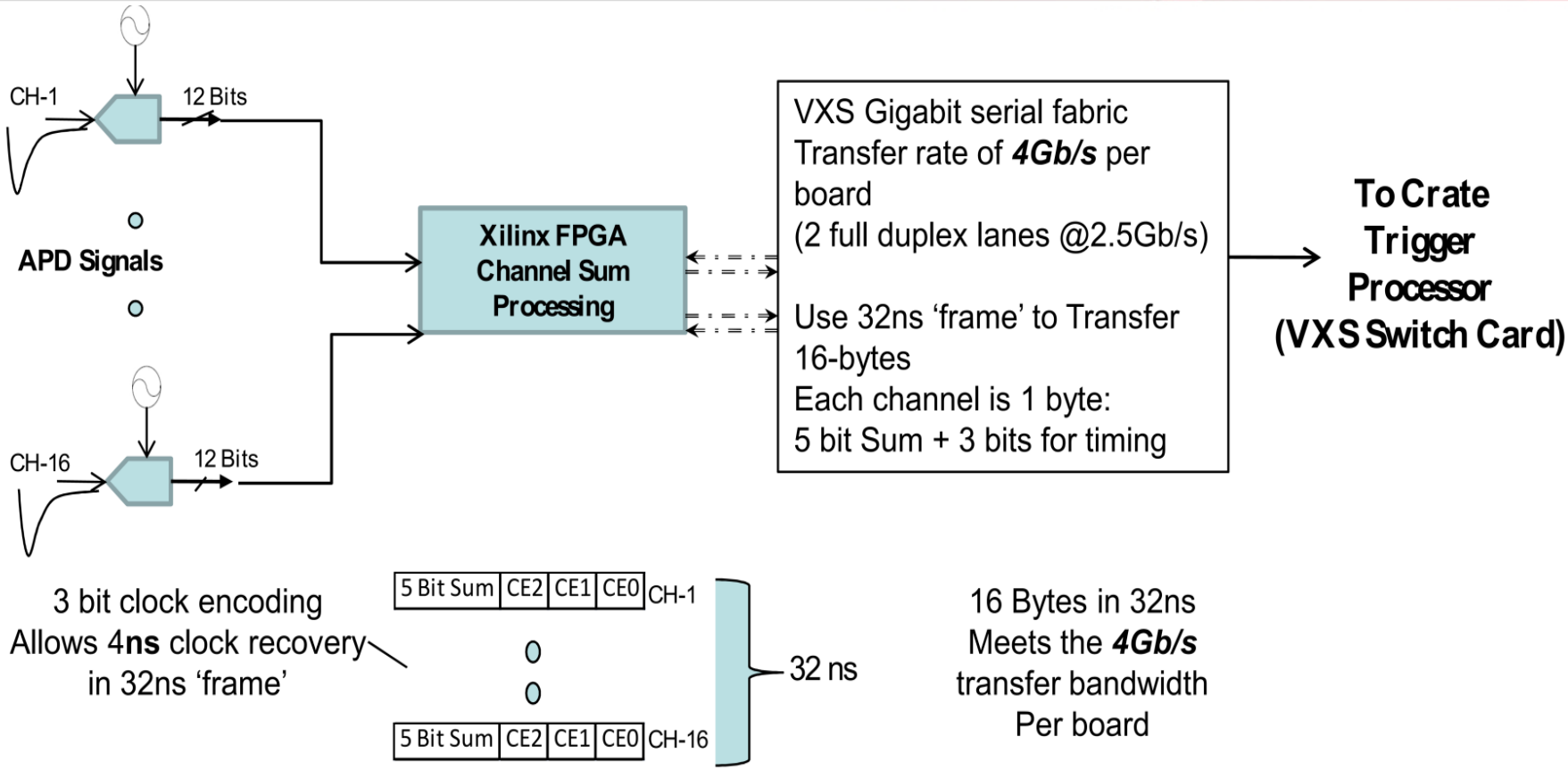


- **Ebeam 5.55 GeV**

Radiator 10^{-4} r.l. Au
Collimator 6.4 mm
Pair spectrometer convertor 1.8×10^{-3}, 4.5×10^{-3} and 1.6×10^{-2} r.l.
Pair spectrometer field - -760A and +760A

Heavy Photon Search Collaboration

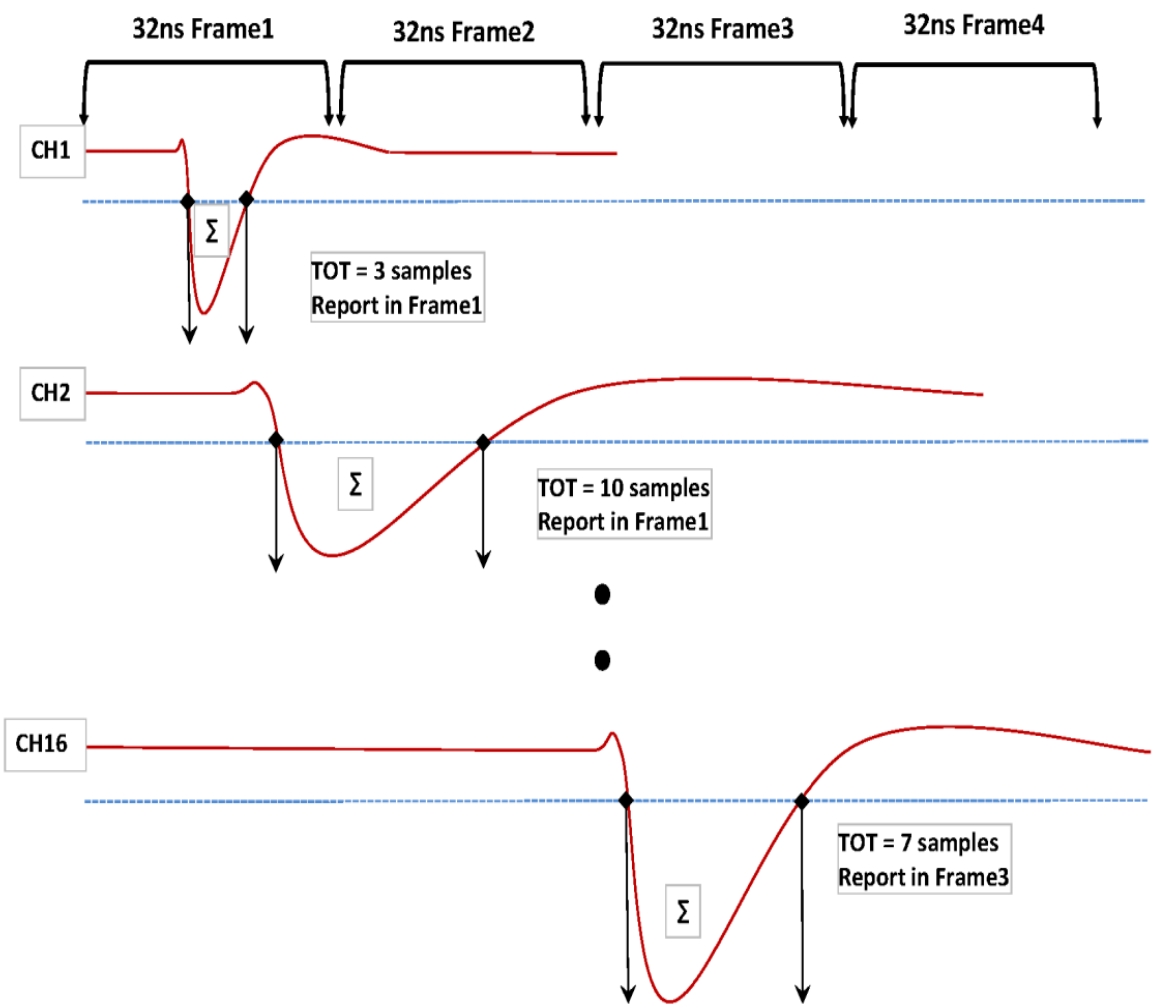
Individual Channel Summing Technique on FADC250



Exploits the use of the existing Gigabit bandwidth to transfer individual energy sums.
The CTP will collect the information and resolve clusters from PbWO4 calorimeter crystal blocks.

4ns cluster hit time is resolved by encoding sample clock for each channel

Individual Channel Summing Technique on FADC250

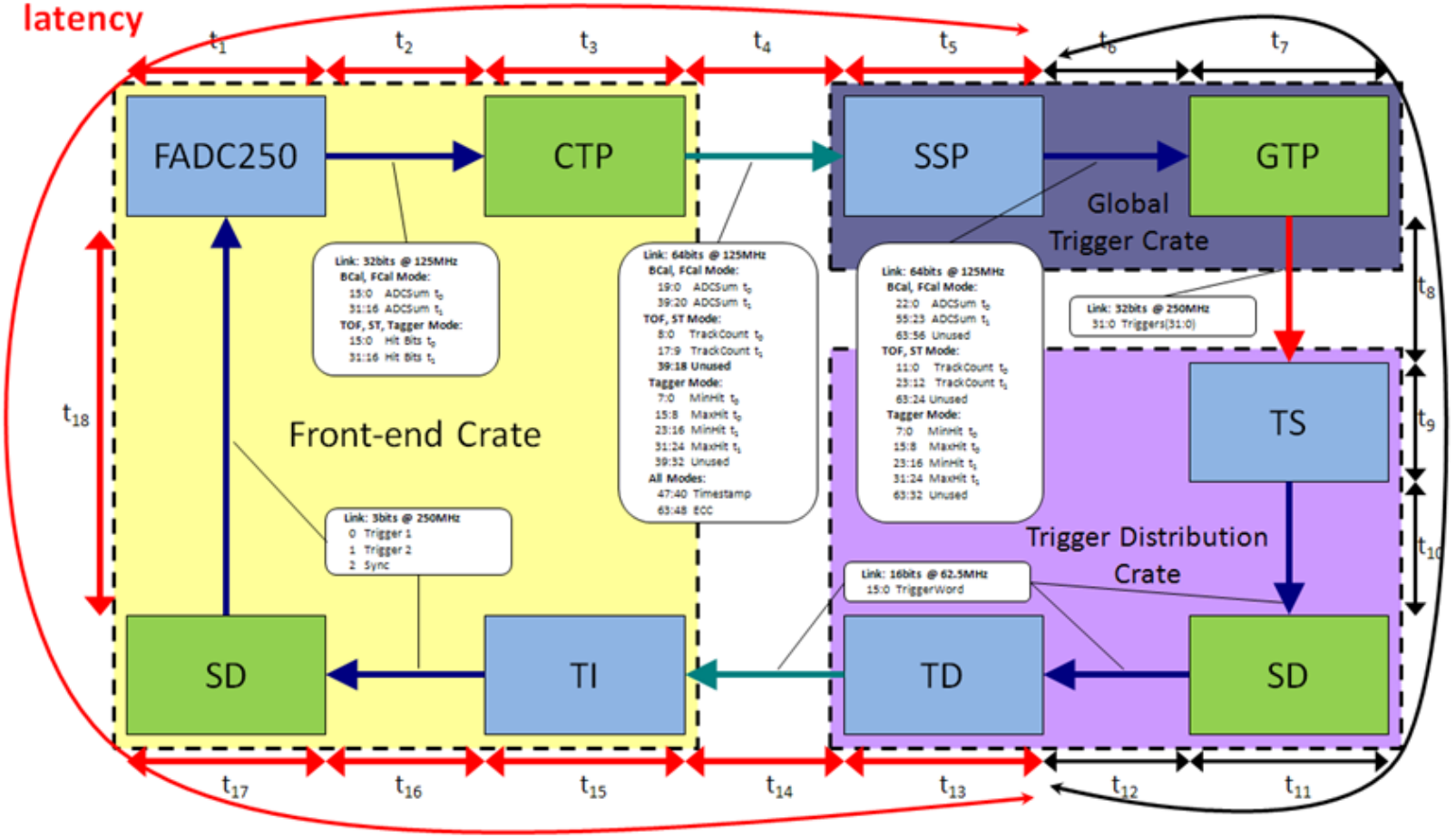


- Use synchronous pipeline to keep track of calorimeter signals by using a 32ns ‘frame’
- ALL channels are collected by the CTP and clusters can be located and reported to the SSP after multiple frames.
- Scalers provide hit counts and nice monitoring results for cluster counts, etc.
- ***See Scott Kaneta’s talk***

GlueX Level 1 Timing

2.3µs measured latency

660ns estimated latency remaining

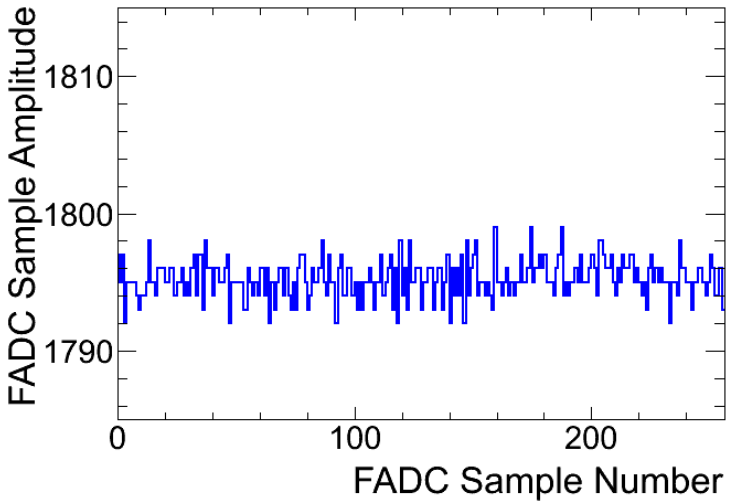


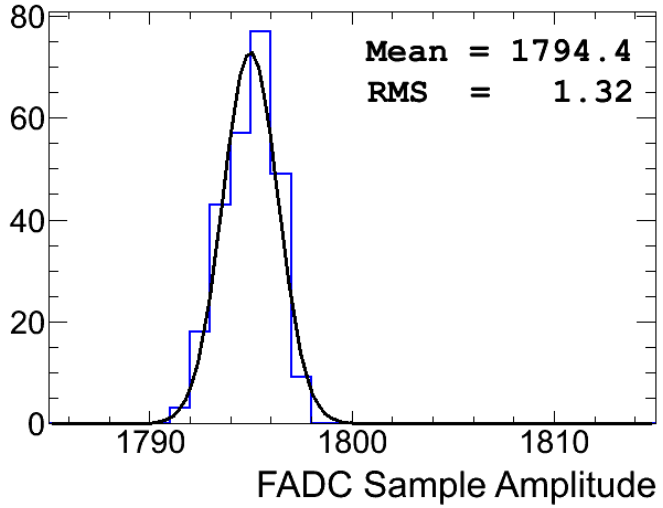
2.3µs (measured) + 660ns (estimated) < 3µs!

Fiber Optic Link
Copper Ribbon Cable
VXS Backplane

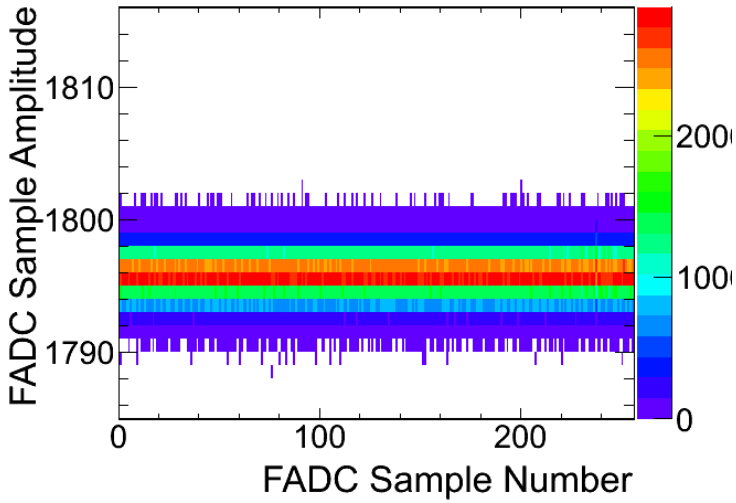
Noise in the FADC (No Readout during data taking)

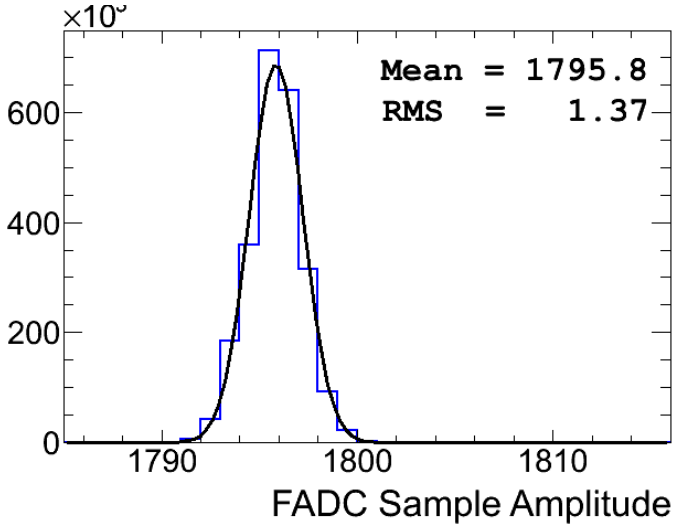
Single Event





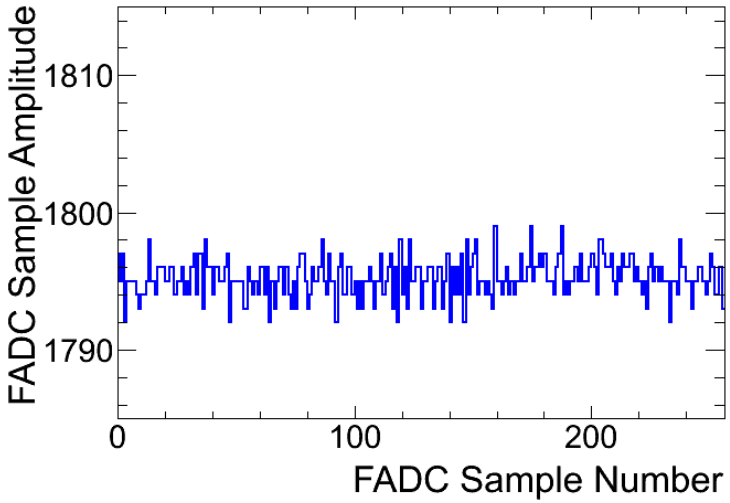
All Events

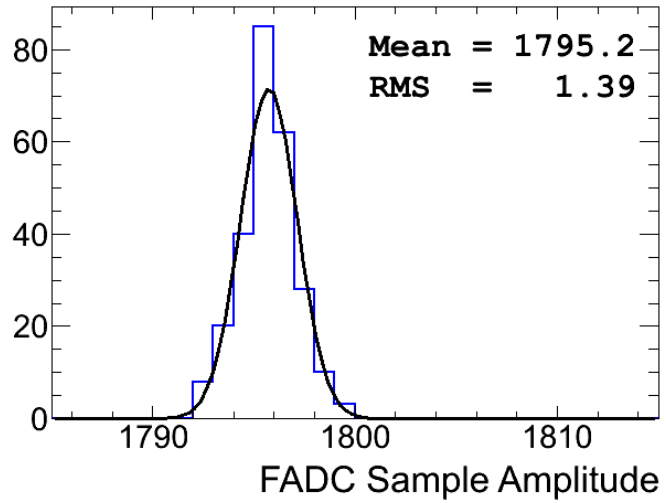




Noise in the FADC (Readout during data taking)

Single Event





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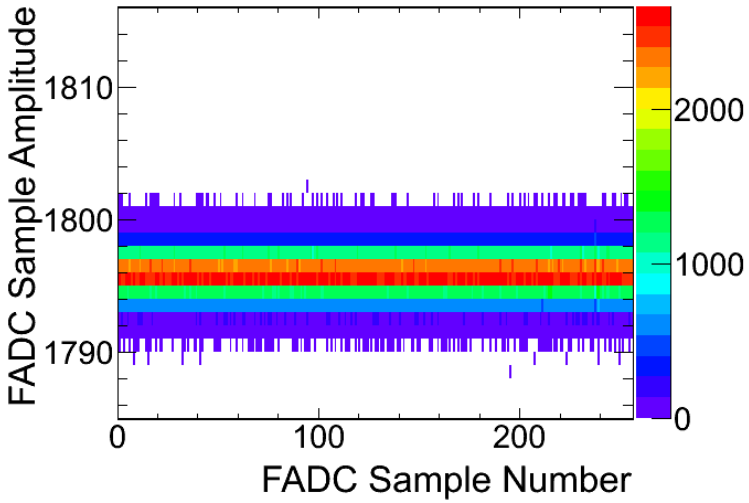
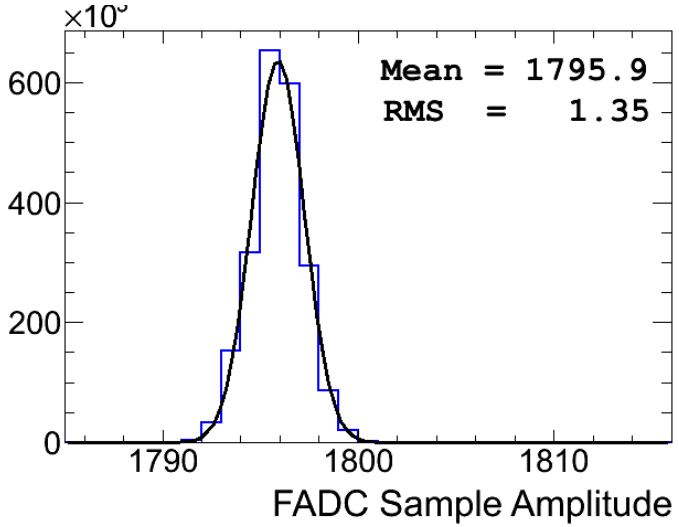
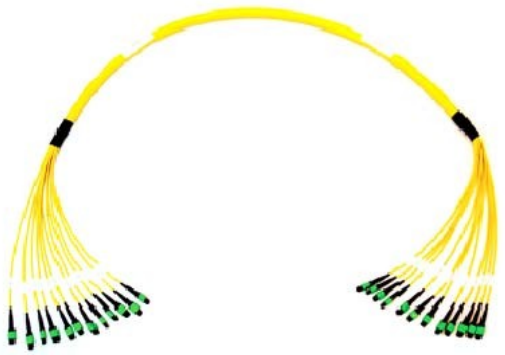




POP4 Avago Transceivers and MTP parallel fiber cable



-Fiber optic cable has been tested at 150m length

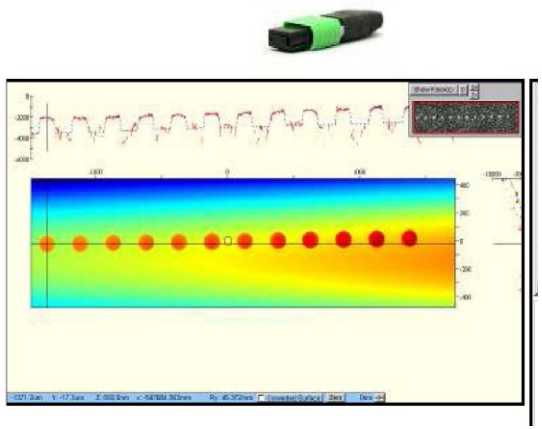
-Longest optic link is from Hall D to Hall D Tagger Is ~100m

-Trunk lines will have 12 parallel ribbon fibers

-144 total fibers

-Multi-mode 50/125um

-MTP connectors to transceivers and patch panels



Specifications:

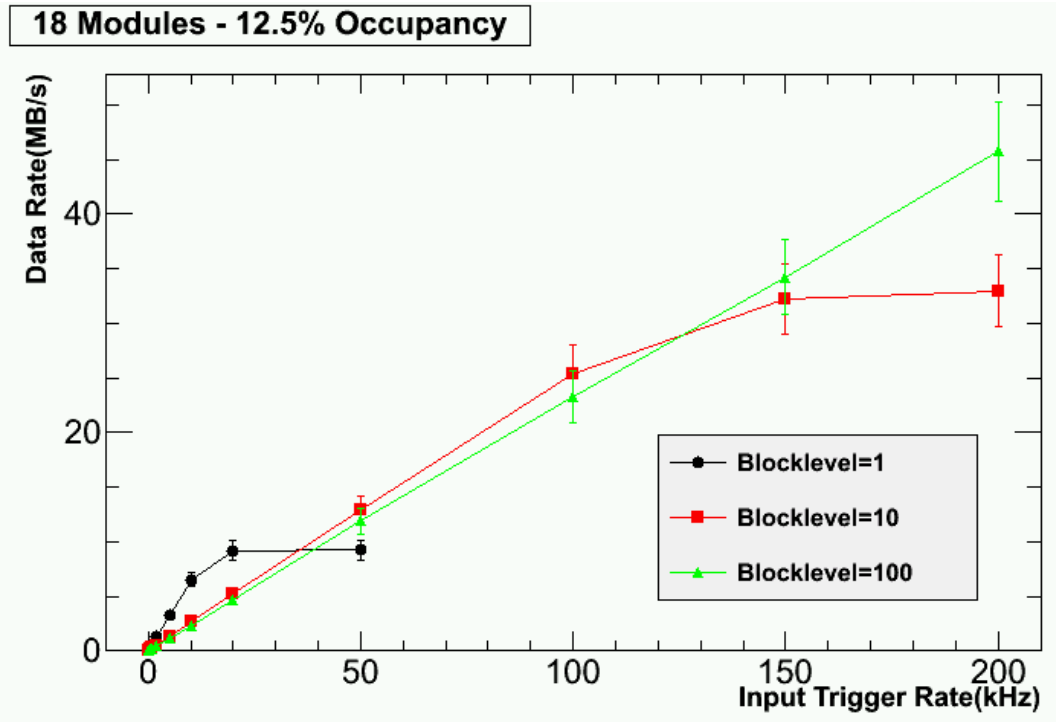
System drawings complete: Hall D – Hall B

Min insertion loss <0.60db
Wavelength 850nm (Avago POP4 Transceiver 3.125Gb/s)
Attenuation (db/km) - 3.5/1.5
Temperature range: -40C- 80C
Low Smoke Zero Halogen jacket – Non-Plenum tray approved

Specifications include installation and testing requirements
Each Hall will require different quantities and specific lengths
Patch panel hardware has been specified and tested

Two DAQ Crate Testing: FY11

- Pre-Production and 1st article boards have been received and tested
- Significant effort for circuit board fabrication, assembly and acceptance testing
- System testing includes:
  - Gigabit serial data alignment
    - ✓ 4Gb/s from each slot
    - ✓ 64Gb/s to switch slot
    - ✓ Crate sum to Global crate @8Gb/s
  - Low jitter clock, synchronization
    - ✓ ~1.5ps clock jitter at crate level
    - ✓ 4ns Synchronization
  - Trigger rate testing
  - Readout Data rate testing
  - Bit-Error-Rate testing
    - -Need long term test (24 - 48 hrs)
  - Overall Trigger Signal Latency
    - ✓ ~2.3us (Without GTP and TS)



200KHz Trigger Rate!

Readout Controller Capable of 110MB/s
- Testing shows we are well within limits

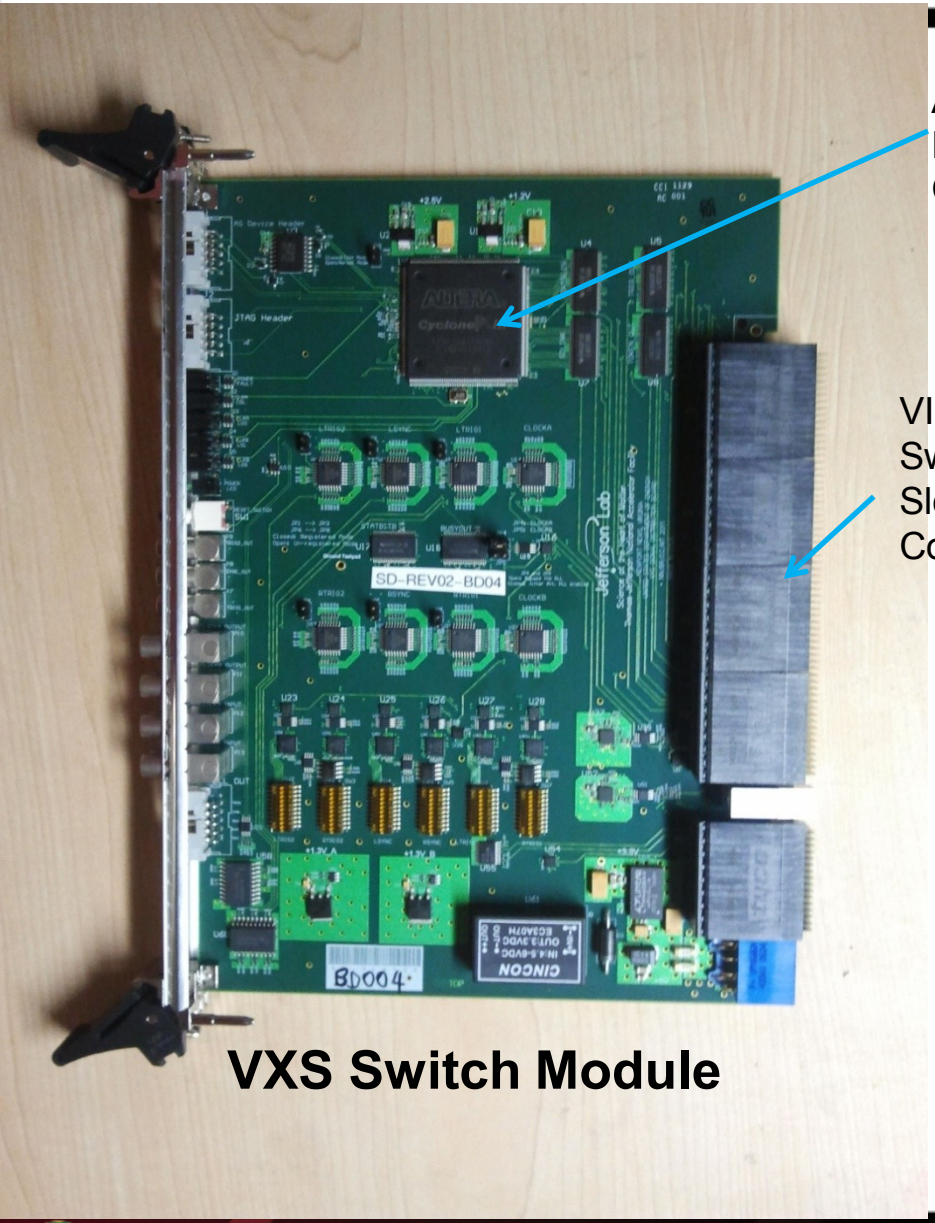
Trigger Hardware Status - TD

W. Gu
DAQ Group
23-Sept-2011

- Distributes from Trigger Supervisor crate to front end crates (TI)
- Distributes precision clock, triggers, and sync to crate TI modules
- Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
- Manages crate triggers and ReadOut Controller events

Crate Level – Signal Distribution (SD)

N. Nganga
23-Sept-2011



VXS Switch Module

- The effect of Jitter attenuation has been tested and found to be most effective when clock signal jitter is >5ps and(or) when the input signal is >100MHz.
- SD boards have been used in the two-crate tests since the beginning of Summer 2011 without glitches.
- PCB manufacture and Board assembly was ~$1000 per board
- SD components are estimated at $1200 per board (price break dependent).

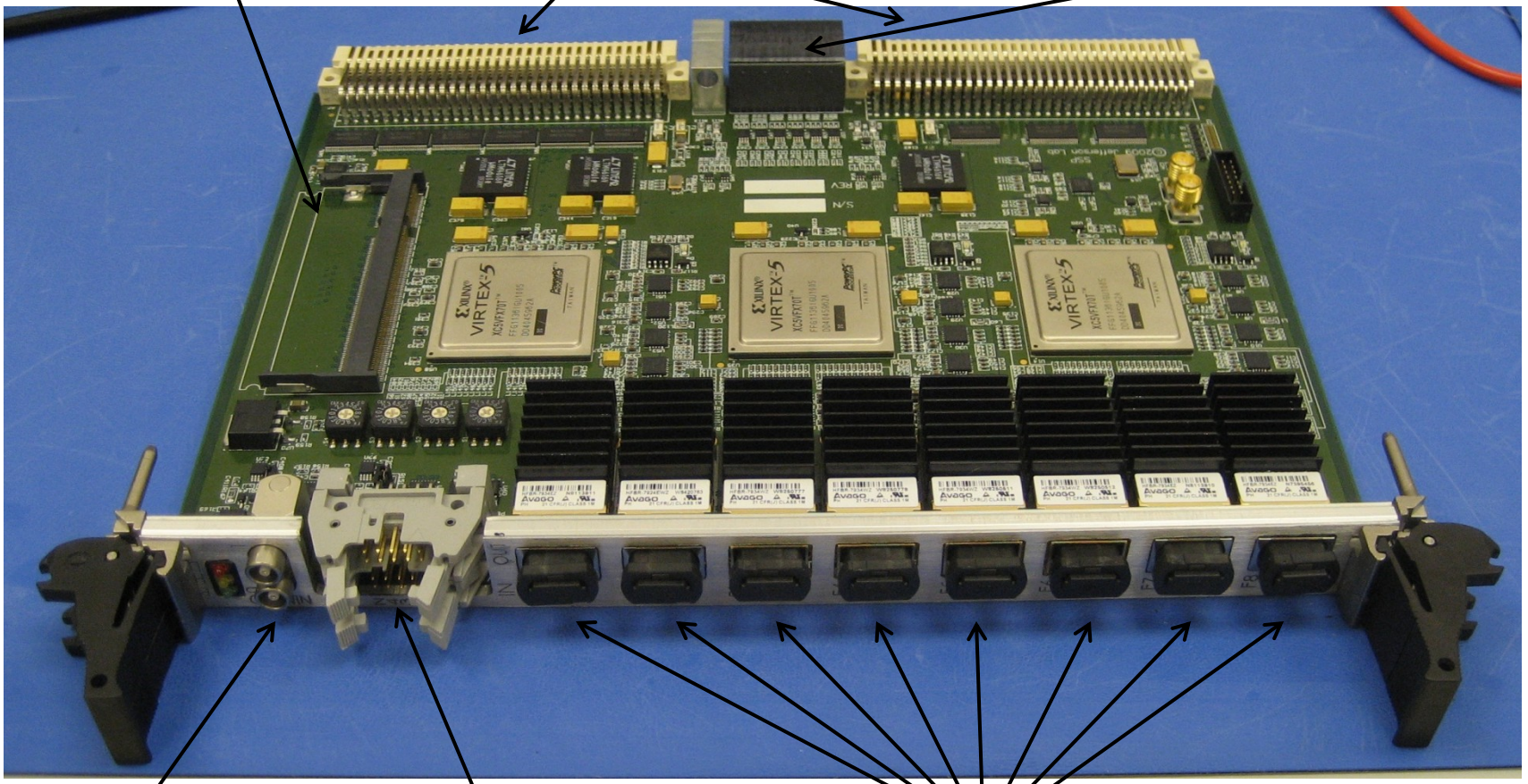
SSP Prototype

Ben Raydo
9-Sept-2010

Optional DDR2 Memory Module (up to 4GByte)

VME64x (2eSST support)

VXS-P0 (up to 16Gbps to each GTP)



2x NIM (bidirectional)

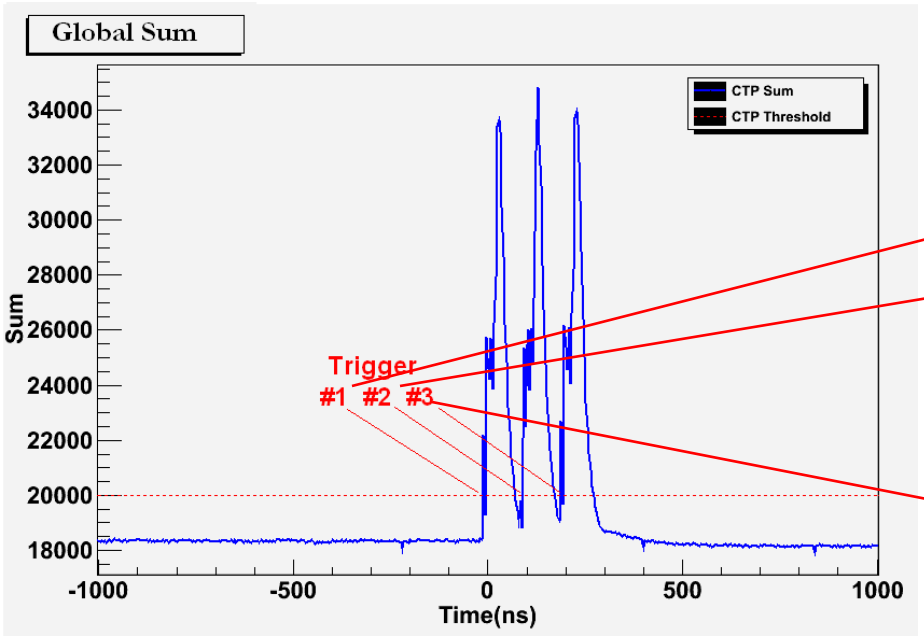
4x ECL/PECL/LVDS In
4x LVDS Out

8x Fiber Ports (10Gbps each to CTP)

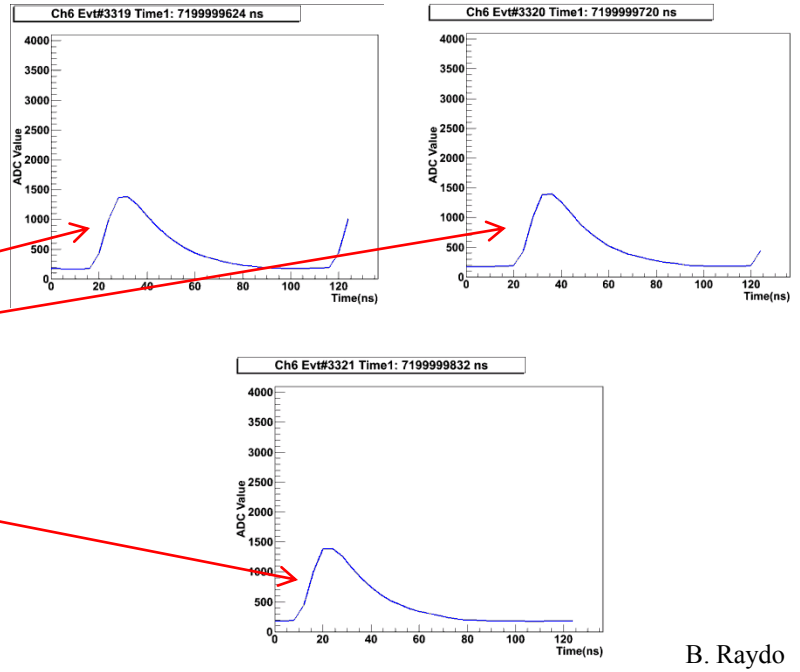
Synchronized Multi-Crate Readout

- CTP #2 is also acting as an SSP (by summing the local crate + CTP#1 sum over fiber
- A programmable threshold is set in CTP, which creates a trigger when the global sum (6 FADC boards => 96 channels) is over threshold.
- Example test with a burst of 3 pulses into 16 channels across 2 crates/6 FADC modules

A 2µs global sum window is recorded around the trigger to see how the trigger was formed:



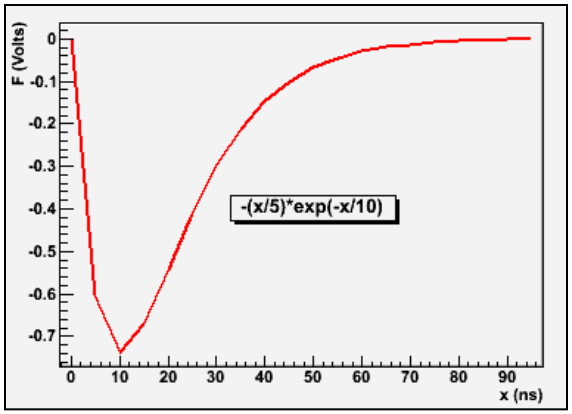
Example Raw Event Data for 1 FADC Channel:



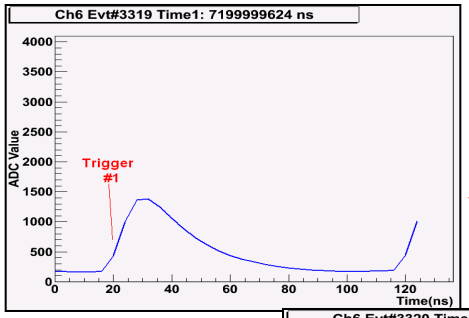
B. Raydo

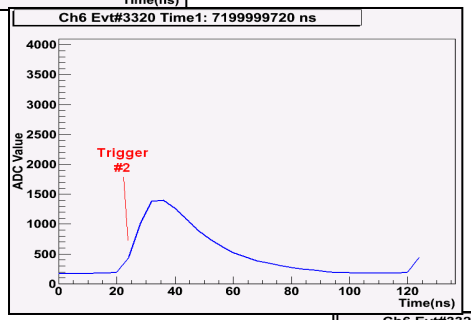
2 Crate Energy Sum Testing

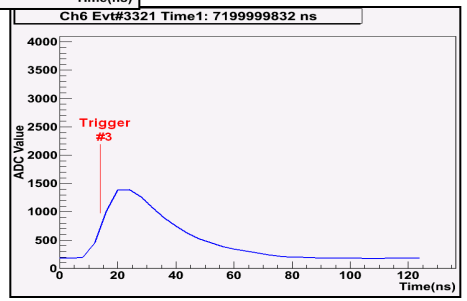
Input Signal to 16 FADC250 Channels:



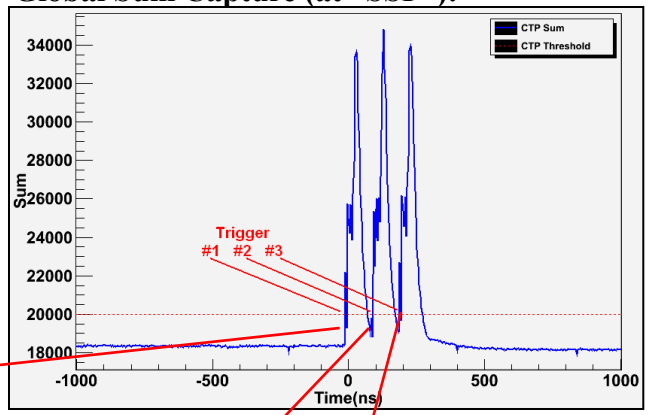
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- **Threshold applied to global sum (96 digitized channels) produces 3 triggers.**
- **Raw channel samples extracted from pipeline shown for 1 channel.**
- **Runs at 250kHz in charge mode**
- ***Latency: 2.3μs(measured) + 660ns(GTP estimate) < 3μs***

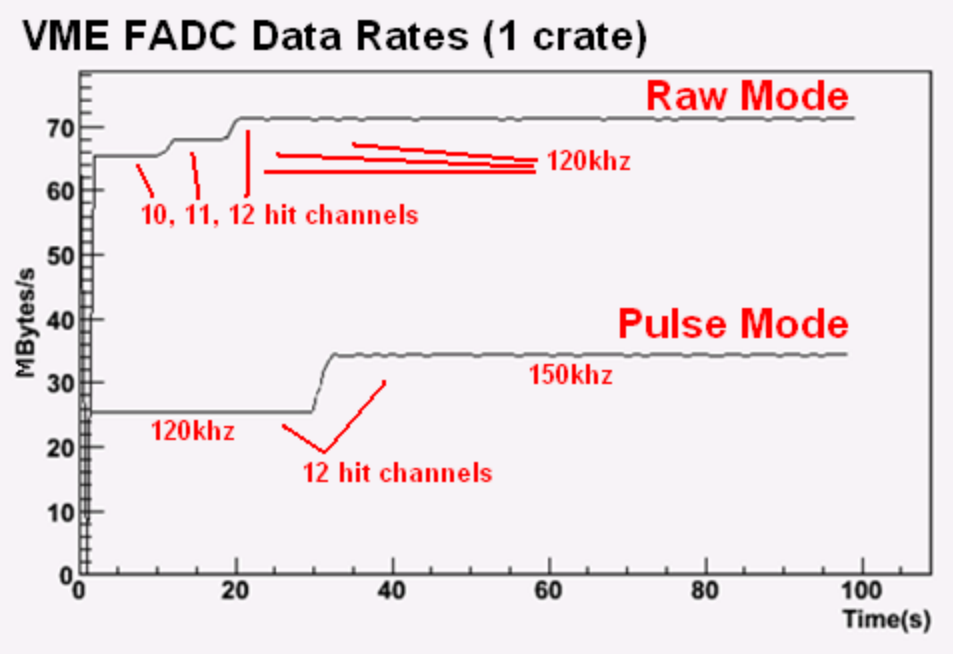
B. Raydo

Synchronized Multi-Crate Readout Rates

• FADC event synchronization has been stable for several billion events @ ~150kHz trigger rate.

• Have run up to 140kHz trigger rate in raw window mode, up to 170kHz in Pulse/Time mode.

• Ed Jastrzembski has completed the 2eSST VME Interface on FADC allowing ~200MB/s readout



Single Crate
12 signals distributed to four FADC250

18% Occupancy

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