Jefferson Lab

GlueX-doc-2515

Electronics Overview
Technical Construction Report

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1 Overview

The GlueX electronics implements signal conditioning, digitization, processing and read out of the detector signals for level 1 trigger rates of up to 200 kHz without incurring deadtime. A fully pipelined architecture is implemented where the digitized information is stored for several μs while the level 1 trigger is formed. Multiple events are buffered within the digitizer modules and read out while new events are acquired.

A summary of the characteristics of the GlueX detector subsystems from an electronics viewpoint is shown in figure 1.

A fully integrated development was implemented to instrument the various particle detectors in a systematic and common infrastructure, which considered grounding, electro-magnetic interference (EMI), cabling, power distribution, detector electronics, digitizing modules, packaging, installation and servicing. Guiding the system architecture in such a manner has considerable advantages in minimizing the number of design variants, conserving resources while taking full advantage of the expertise available within the collaboration and JLab, addressing electrical safety per code requirements, and improving performance, reliability and servicing of the installed instrumentation.

There are three classes of sensors in use with GlueX detectors: PMTs, SiPMs and drift chambers. PMTs are typically powered from commercially available HV power supplies and readout via coaxial cables; SiPMs (Silicon Photo-Multipliers) are optical sensors which have been developed recently, produced in large quantities for GlueX by Hamamatsu , require custom designed frontend electronics and require bias supplies of less than 80V; the GlueX drift chambers are instrumented with ASICs and preamp cards specifically designed for the CDC and FDC.

2 ASIC and Preamps for the Drift Chambers

An Application Specific Integrated Circuit (ASIC) was developed for application in both the FDC and CDC drift chambers. This was necessitated because of the geometrical constraints presented by the packaging into the FDC with the limited space of 5mm between the detector layers and within the solenoid volume.

The ASIC (GASS-II) is configurable for the specific application and includes a charge preamplifier, shaping with tail cancellation, switch, driver and discriminator. Configuration is effected at the PCB level during assembly to conform to the FDC and CDC requirements. Figure 2 shows the block diagram and of the fully differential GASS-II.The GASS-II is characterized by CR-RC^2 with the following behavioral Laplace transfer function:

$$\mathfrak{L} = \frac{R1}{1 + sR1C1}\left(\frac{R3}{R2}\right)\frac{\frac{1}{sR2C2}}{1 + sR3C2}\,\frac{1}{(1 + sR4C3)^2}$$

Where R1=9.5kΩ, R2=100kΩ, R3=R4=16kΩ, C1=0.65pF, C2=C3=0.3pF. This function together with the transfer functions of the signal cable and of the fADC125 input shaping circuitry fully describe the transfer function of the readout chain of the drift chambers and can be employed to devise algorithms for data processing. The GAS-II equivalent noise charge is less than 5,000 electrons at 50pF of detector capacitance with a characteristic slope of 45e^-/pF. The output level, when in discriminator mode, is LVDS and readily interfaces to the F1TDCV3. Typical characteristics of the GASS-II are:

ASIC ID	GASS-II
Number of Channels	8, differential with input protection
Type	Charge amplifier
Configuration	Gain, peaking time, discriminator
Peaking time	11ns
Discrimination	20ns pulse width, common threshold input
Noise (ENC)	5,000 e^- @50pF
Package	64 pins, 10mm X 10mm, QFN, *ipac*
Process	0.25µm, CMOS
Manufacturer	MOSIS
Die ID, size	V13L-AA design 80773, 7.04mm X 4.8mm

A 24-channel preamp card (GPC-II) was also developed to serve both the FDC and the CDC so that only a single ASIC design and a single preamp card design are needed. This common infrastructure extends to supporting systems such as signal cabling, the low voltage and the high voltage supplies and distribution, as well as controls. Figure 3 shows the top side of GPC-II; the bottom side has one additional ASIC and the configuration resistors, which are placed according to the requirements of the CDC and the FDC. Polarity configuration is also set via resistors during assembly, a benefit of the differential topology. The configuration of the 24-Ch GPC-II is as follows:

Application	Assembly Variant	Input Signal Polarity	Gain (mV/fC)	Dynamic Range (fC)	Peaking Time (ns)	Power (mW/Ch)
CDC Anode Wires	Type I	Negative	0.57	380	12.0	49
FDC Cathode Strips	Type II	Positive	2.6	130	13.8	49
FDC Anode Wires	Type III	Negative	0.77; LVDS Discriminator	260	9.6	49

The preamp card is less than 5mm thick in its installed position to meet the FDC layer spacing requirements. Due to the limited space, cooling of the preamps on the FDC is effected via heat spreader brackets attached to cooling loop pipes and with Fluorinert liquid flow; forced convection is implemented on the CDC due to less restrictive geometrical conditions.

Cabling for the 24 differential output signals consists of 0.025” pitch 50 wire, twisted and shielded cable, low profile and high density 50-pin ERNI connectors for the preamp side and robust 50-

pin 3M shielded connectors for the readout side; the 25th pair is used to capacitively pulse all the 24 channels from signal pulsers designed into the fADC125s and the F1TDCV3s.

The preamp cards are plugged into PCBs laminated into the FDC, again due to geometrical constraints; the CDC benefits from the same design a nd employs an interposer board, the High Voltage Board (HVB), which also provides high voltage distribution to 24 straw tubes from a single high voltage supply channel. Straw tube connections to the HVB, which are AC-coupled, are effected via coaxial cables with their shields connected to the high voltage input and decoupled to ground for good noise performance. Due to the high input charge from the CDC, divide-by-2 charge division is implemented at the input of every preamp channel. The HVB is shown in fig. 4.

Application	Assembly Variant	Input Signal Polarity	Effective Gain (mV/fC)	Effective Dynamic Range (fC)	Peaking Time (ns)	Power (mW/Ch)
CDC Anode Wires	Type I with HVB	Negative	0.30	740	12.0	49

3 SiPM Readout

SiPMs are semiconductor optical sensors which replace PMTs in applications requiring insensitivity to magnetic fields. The BCAL, PS, ST and TAGM detectors employ SiPMs in various configurations, all with 3mm x 3mm cells and 50μm pixels manufactured by Hamamatsu.

The BCAL SiPM ceramic package was developed jointly with Kyocera to address the thermal and geometrical requirements of the BCAL modules, which require good temperature regulation at 5°C for lower sensor noise. The rear of the package allows for contact to a cooling plate and a two-stage regulation is implemented to maintain the SiPM gain constant: liquid cooling flows through a pipe embedded into the cooling plate to effect cooling of the SiPMs in a BCAL module; a thermistor-resistor network, matched to the SiPM temperature characteristic but with a positive +56mV/°C slope, compensates each SiPM bias voltage against further temperature non-uniformities. The 4x4 SiPM array is shown in fig. 5 (front) and fig. 6 (rear). The PS, ST and TAGM employ the same single cell SiPM S10931 from Hamamatsu.

Fig 7 is a diagram of the cooling and readout implementation on the BCAL. Thermal mats are employed to effect low thermal impedance connections between the SiPM and the cooling plate and the readout electronics and the heat spreader, which eventually dissipates excess heat to ambient. The “U” PCB holds the SiPM, implements a 16 cell sum and provides bias distribution; electrical connections are implemented with miniature coax cables. The light guide from the BCAL detector couples light to the SiPMs through a 1mm gap and the module is permeated with nitrogen to prevent condensation.

The BCAL, PS and ST share similar readout architectures with bias temperature compensation and where several sensors are biased from a single bias supply channel; the TAGM includes temperature compensation through direct bias setting to each SiPM from DACs. Fig. 8 shows a diagram of the SiPM readout architecture: the thermistor, R1 and R2 are chosen to have a +56mV/°C slope and, therefore, maintain the SiPM gain invariant to temperature changes and provide the required SiPM bias; the anodes of the sensors, pixels or cells, are connected, via a shaping network, to the transimpedance preamps, which are referenced to ground potential. The shaping network, which is unique to each of the BCAL, PS and ST detectors, optimizes the signal response for the characteristically large SiPM capacitance. The

buffer and driver outputs are then coupled to 50 Ohm coaxial cables of the RG-58 type. In the case of the PS, which does not require a TDC, the high gain driver is not implemented. The gain specifications, not including cable losses, are as follows:

Detector	SiPM Cells per Channel	Transimpedance Gains (mV/μA)	Gains wrt 50Ohm (V/V)
BCAL	16, 32, 48, 64	0.081, 0.405	1.6, 8.1
PS	1	0.987	19.7
ST	1	0.685, 6.85	13.7, 137

SiPMs share directly controlled bias supplies channels as follows:

Detector	SiPM Cells per Supply Channel
BCAL	160
PS	5
ST	4
TAGM	1

4 Readout Modules

Readout modules were developed within a fully pipelined framework and to take full advantage of the VME standard and associated infrastructure, widely used at Jlab. A large and fully pipelined and synchronized data acquisition system benefits from a compact and robust distribution of high-speed timing signals: this is made possible by the use of newly developed extension to the VME64x standard (ANSI/VITA 1.5), which resulted into the VXS standard (ANSI/VITA 41.0). The VXS standard allows for distribution of serial data through the backplane PCB between readout modules located on payload slots and processing or distribution modules located on switch slots. VXS is backward compatible with VME64x so that standard VME modules can be installed on the VXS payload slots. Fig. 9 shows the JLab VXS crate. The black connectors seen on the backplane are part of the newly developed VXS with the centrally located two slots, the switch slots, allowing for serial communications to each of the other slots in the crate for a total of 21 slots.

Differential pairings enable high-speed communication and signaling between each slot's VXS connector (P0) and the connectors on the two centrally located switch slots. All of our VXS-compliant readout modules use this feature for clock distribution and synchronization; the fADC250 further utilizes this feature to enable collection of trigger data from all the installed modules in a crate and subsequent processing and trigger forming.

The VXS crate is manufactured by Wiener, occupies 11U of rack space and accepts modules with a 6U form factor. The high-power, low noise, plug-in power supplies are easily serviceable from the rear of the unit. The fan unit carries three high-speed fans capable of reaching 6,000 rpm, includes controls and monitoring via Ethernet and local switches and it is easily serviceable through the front of the unit. A filter and plenum at the bottom of the unit provide for front filtered air intake, cooling of the readout modules and with the air exiting at the top and rear of the unit. The power supply unit contains its own thermal management.

Five readout modules are used in Hall D and their functionality will be briefly described below: fADC250, fADC125, F1TDCV2, F1TDCV3 and Discriminator. Other modules, which are widely used as part of the trigger and the signal distribution, such as the TI/TD, the SD and the CTP will be described under the trigger section.

4.1 fADC250

The fADC250 is a 12-bit flash Analog-to-Digital Converter, 6U VXS-compliant module primarily used with detectors that participate in the trigger formation. It employs ADC chips with pipeline architectures for high sample rates at reduced power consumption: the Analog Devices AD9230 forms the core of the fADC250 with its rich feature set which includes advanced test vector generation. The backend of the module is enhanced with the use of Xilinx XC5VLX110 and XC5VFX70 FPGAs which, by virtue of their vast resources, allow for tailoring the functionality of the module with firmware updates via VME. Fig. 10 shows the architecture of the fADC250.

Each of the 16 inputs is DC-coupled through a settable attenuator, via jumper, which allows for operation with bipolar signals at full-scale ranges of 0.5V, 1.0V and 2.0V, while maintaining 50 Ohm impedance. The input circuitry is fully differential with individually programmable DACs for setting the offsets and signal conditioning is implemented with anti-aliasing filters. Process variations are handled by an active common-mode correction bias derived from the ADC chip.

The first FPGA handles data processing duties, including the trigger sums with user-defined thresholds; the second FPGA handles VME communications through the standard VME P1 and P2 connectors and VXS signal handling through the P0 connector, which includes clock and synchronization signals and trigger data with the two switch slots. A JTAG port is available for various testing and configuration protocols.

The sampling, data readout and trigger formation characteristics of the fADC250 are illustrated in fig. 11. Data is sampled at 250MHz with a distributed low jitter, less than 15ps, clock. Signals present at the input of a channel are sampled every 4 ns and stored. This data can be readout via VME or it can be further processed to select hits or energy sums for inputs to the trigger at the 4 ns sampling interval. Hit bits from the 16 channels in a fADC250 are asserted for samples that exceed a programmed threshold. For the case of triggers based on energy sums, the samples from each of the 16 channels are summed together, resulting in a 16-bit word. The choice of data processing, hit bit or energy sum depends on the type of detector.

Once a trigger signal is formed by the global trigger system and distributed back to the fADC250 modules, the data within a selected trigger window is readout through VME. The window is selected relative to a programmable look-back delay specified by the trigger latency. The trigger latency and trigger window quantities are chosen based on the characteristics of the detectors and the various delays and will be determined empirically with great accuracy. Triggers are also pipelined.

The data to be readout is available through VME under control of the read-out controller (ROC) as raw data from sampling at 250 MSPS, as raw data of N samples in the vicinity of a pulse or as the sum of N samples in the vicinity of a pulse. The number of samples, N, is programmable by the user. The time information, based on the sampling rate, is obtained by looking for samples forming a rising edge of a pulse and a linear interpolation algorithm provides an estimate of the time the pulse would have crossed a programmable threshold.

The second data path pertains to the trigger formation and is output through the P0 connector and VXS backplane. This serial data stream consists of either the sum of samples or hit bit patterns processed at 250 MSPS. In order to maintain line balancing, the Aurora protocol is implemented over two lanes of the VXS backplane fabric for an aggregate data transfer rate of 4 Gbps. The fADC250 module is shown in Fig. 12 and a summary of its specifications in fig. 13.

4.2 fADC125

The fADC125 is a 12-bit flash Analog-to-Digital Converter, 6U VXS-compliant module used with the tracking detectors, FDC and CDC. It employs ADC chips with pipeline architectures for high sample rates at reduced power consumption from Linear Technology: the LTC2283, a two channel device, forms the core of the fADC125. The backend of the module is enhanced with the use of Xilinx XC6SLX25, XC3SD3400 and XCS500 FPGAs which, by virtue of their vast resources, allow for tailoring the functionality of the module with firmware updates via VME. Fig. 14 shows the architecture of the fADC125.

The fADC125 module consists of two PCBs: main and mezzanine. Each of XC6SLX25 FPGAs handles six input channels or three ADC chips and data is transferred through serial daisy-chain busses to the processor FPGA, the XC3SD3400. Data is first processed through the algorithm loaded onto the frontend FPGAs and buffered into FIFOs for further processing and event building onto the processor FPGA. Communications, clocking and synchronization through VME and the VXS P0 is then handled by the XCS500 FPGA. Firmware and data processing architectures followed the development of the fADC250 and were adapted to this ADC module. The fADC125 module is shown in Fig. 15 and a summary of its specifications in fig. 16.

4.3 TDCs

The first development of a pipelined module at JLab was the F1TDCV1, which was based on the F1 ASIC developed for the Compass experiment at CERN. Its block diagram in fig. 17 shows the F1TDC chip as the core functional element of the F1 series of TDC modules. Newer versions of this TDC were developed to address the needs of Hall D and serving as a single TDC development platform: the F1TDCV2 with 32 ECL-compliant input channels and less than 60ps resolution; the F1TDCV3 with 48 LVDS-compliant input channels and less than 100ps resolution for the FDC tracking detector, wires only. Each of the modules consists of main and mezzanine PCBs. The TOF detector, with its higher resolution requirements, employs the commercially available VX1290A TDC from CAEN with 32 ECL-compliant input channels and less than 35ps resolution.

The core of our TDC modules is the F1 TDC chip. A functional block diagram of the F1 ASIC chip is shown in fig. 18. This chip uses purely digital delay techniques to measure time by means of a 19-tap asymmetric ring oscillator with delay-locked loop (DLL) control. Each of the pipelined F1 chips provides eight channels nominally at 120 pS LSB or four channels at 60 pS LSB. Internal FIFOs allow for storage of 16 hits per channel in leading and/or trailing edge modes.

A key feature of the F1 chip is a Trigger Matching processing unit, which allows for selection of hits within a programmable time window and latency from the occurrence of a valid trigger input. Hits that fall outside of the window and latency settings are suppressed from the output buffer and cleared from the hit FIFO. The trigger matching feature is used in common start/stop and synchronous measurement modes. In common start/stop mode, a ***Start*** signal resets the internal measurement counter

and a ***Trigger*** signal sets the measurement window. Hits falling within these two signals will always be accepted by the trigger matching unit. In synchronous mode, a ***Synch-Reset*** signal is used to reset the internal measurement counter and thus synchronize all TDCs in an experiment. Internal start signals are automatically generated at a programmable rate. The trigger matching unit validates hits within the programmed window and latency. Headers and trailers identifying the channel, chip, trigger time and event number can be output to delineate events. The dynamic range is 7.8 uS at 120 pS LSB and 3.9 uS at 60 pS.

To ensure stability and measurement reliability, each F1 chip is DLL-regulated against temperature drifts and manufacturing tolerances. The feedback loop employs a phase-frequency detector, a loop filter and a voltage regulator, which drives the substrate or core of the F1 chip. In this manner, delays within the internal Delay Locked Loop (DLL) are kept constant which translates into a stable LSB resolution or bin size. The F1 chip is configured via a serial interface port, which accesses 16 registers.

Data from each F1 chip is readout via a 24-bit parallel port into a 4Mbit FIFO. An Altera EP3C80F780 FPGA with over 2.5Mbit memory processes data into event building, VME interfacing and VXS clock and synchronization tasks. The clock frequency for the F1TDCs is 31.25MHz, which is derived and synchronized from the master 250MHz clock through the TI and the SD modules. Figs. 19 and 20 show the F1TDCV2 module and its specifications, respectively; figs. 21 and 22 show the F1TDCV3 module and its specifications, respectively.

4.4 Discriminator

The 16-Channel Discriminator/Scaler Board contains 16 non-updating dual-threshold discriminators, programmable digital delays, and two 32-bit scalers per discriminator and threshold and it is VME64x compliant. The discriminator pulses are output as differential ECL logic levels through two front-panel headers. One group of outputs will connect to a TDC and the other group can be used as input to trigger logic. Both TDC and trigger output channels can individually be enabled/disabled with outputs widths and delays being user programmable. All programming is done through VME registers. Fig. 23 shows the block diagram of the JLab discriminator.

All discriminators and logic reside on a 6U standard VME mainboard. Each channel contains two analog receiver fast comparators (discriminator), and pulsers. Each discriminator channel has 2 programmable thresholds which can be programmed from VME. The output pulse width is also programmable from VME, but is common to the TDC and trigger discriminator channels separately. The digital delay circuit delays each discriminator pulse up to 512ns in 4ns steps (used for trigger output path and scaler input path when using external gate input). It is implemented with a high-speed (250MHz) FIFO for each discriminator channel. The delay is software selectable for the trigger output, trigger scaler input, and TDC scaler input. Each discriminator output pulse is recorded by a 32 bit counter (scaler) which can be gated with the external Gate (NIM) input. Scalers can be latched, read, and cleared through VME. There is a “OR” (NIM level) ouput that is the logical OR of all the unmasked discriminator outputs. Discriminator outputs are provided as dECL levels on the front panel for interfacing with TDCs and trigger logic. The VME interface is A32/A24/D32 with support for interrupts. The Discriminator module is shown in Fig. 24 and its specifications are shown on fi. 25.

5 Grounding, Shielding & EMI

A systematic approach to grounding and shielding of equipment was implemented to ensure good performance from the detectors and the electronics. The single-point ground topology provides superior characteristics compared to any other approaches and must be considered as extended bonding, which relies on a grounding grid built into the floor of the experimental areas and as shown in fig. 26.

Grounding is effected by properly segregating and managing different types of sources, loads and their interconnections. Fig. 27 illustrates the grounding implementation diagrammatically.

Low noise susceptibility and emissions from the readout of all the detector sub-systems provide the necessary basis for good resolution. Bonding attachments are designated to be used with specific detectors which require very low noise while other bonding pads on the grid are designated to be used with devices which are characteristically noisy, such as pumps and the high power solenoid power supply for example. Wide bandwidth and low impedance bonding is implemented by means of thick cable (4/0). The FDC, for example and noted as A in the figure, has all of its four packages' grounds connected together at the detector and then bonded to a "clean" ground pad on the grid; single-point shielding is also bonded to a pad on the grid, separate from noisy loads; structures, such as the platform, are also bonded to the grid, but separate from the "clean" detector grounds. Proper AC power distribution with its associated grounds follows a similar approach in segregating equipment based on application. Ground loops are also minimized, except where interconnections are made through coaxial cables.

Electro-Magnetic Interference (EMI & RFI) is a major cause of noise observed in the readout of particle detectors due to their required high sensitivity to low-level signals. Good grounding and shielding techniques is complemented by employing equipment with low EMI/RFI characteristics and by proper placement in the experimental area. In view of such demanding requirements, a sufficiently stringent plan that manages the deployment of equipment in the hall is necessary to ensure good overall performance and limit the sources of interference. The following commercial standards are adopted in Hall D: FCC part 15 Class B, CISPR 11/ EN 55011 Class B, CISPR 22/ EN 55022 Class B and EN 61000-6-3. It should be noted that some equipment, notably control hardware, do not generally conform to class B and their placement is segregated from sensitive detectors and electronics.

6 HV and LV Systems

The high voltage (HV) and low voltage (LV) systems, including distribution hardware, were implemented to take full advantage of the grounding and shielding architecture described earlier and in keeping with low noise requirements for good performance of the detectors and readout electronics. As such, all the supplies, with the exception of small modules used with the FCAL, are of the floating type and referenced to the detector ground and ground grid in the experimental hall. The HV and LV systems are based on commercially available units from CAEN and Wiener, respectively.

The HV system consists of the CAEN SY1527 chassis with modules A1550P, A1550N and A1535SN. These modules have floating outputs or returns, clamped to ground and interlocks for safety. HV channels are distributed on the CDC HVB and on the FDC PCBs; each channel from the A1535SN modules feeds one PMT.

Module	Type	Range	Connector	No. Channels	Detectors
A1550P	Positive	+5kV, 1mA	Radiall	24	CDC, FDC
A1550N	Negative	-5kV, 1mA	Radiall	24	CDC, FDC
A1535SN	Negative	-3.5kV, 3mA	SHV	24	TAGH,PSC,TOF

The LV system consists of the Wiener MPOD chassis with low noise modules MPV8008, MPV8030, MPV8120 and ISEG EHS F201x_106 F. These modules have floating outputs clamped to ground and interlocks for safety. All the LV channels are distributed appropriately by detector subsystem

and employ custom distribution chassis or are integrated into the detector readout boards. Bipolar supply requirements are implemented at the hardware level by connecting supply channels in series and referencing the mid-point to the detector ground.

Module	Type	Range	Connector	No. Channels	Detectors	Usage
MPV8008	Floating	8V, 5A	D-sub	8	TAGM,PS,ST,CDC,FDC,BCAL	Power
MPV8030	Floating	30V, 2.5A	D-sub	8	FDC, BP	Disc. Vth, Power
MPV8120	Floating	120V, 100mA	D-sub	8	TAGM	SiPM Bias
ISEG	Floating	100V, 10mA	Redel	16	PS,ST,BCAL	SiPM Bias

A BCAL distribution chassis is shown in fig. 28 and others are similar.

7 Cabling & Racks

Various cable types are employed in Hall D, including RG-58 coaxial for signal transmission, RG-59 coaxial for HV, twisted-pair for signal transmission and multi-wire for HV and LV power distribution and control. Regardless of type, all the cables are shielded with their shields referenced to ground to minimize common-mode noise pickup and emissions and for safety.

An important consideration in large installations is to ensure that there is a good level of fire safety in limiting the propagation of fire by employing appropriately rated cables. Hall D follows the standard National Electrical Code for fire safety (NEC NFPA 70, 2011 Edition) enforced in the USA and UL listing of CL2 cables, or better. Installation is guided by the NECA/NEMA 105-2007 standard for installation of cable tray systems, which is extensively applied throughout the experimental area.

Racks hold the various chassis and crates throughout the experimental areas and are commercial-off-the-shelf (COTS) items. The Hammond C4F247736 is the standard rack in use and was chosen for its welded construction, with grounding studs, robust construction and enough usable height (44U) to hold three chassis while fitting under the platforms. Vertical and horizontal cable managers facilitate cabling and allow for a clean and safe installation. Fig. 29 shows the location of the racks in Hall D and fig. 30 shows a section of the electronics installation.

8 Summary of Gluex Electronics

A summary of the required electronics for GlueX is shown in fig. 31.

Summary of GlueX Detector Subsystems

Detector →	Photon Tagger (TAGH/TAGM)	Pair Spectrometer (PS/PSC)	Start Counter (ST)	Central Drift (CDC)	Forward Drift (FDC)	Time-of-Flight (TOF)	Barrel Calorimeter (BCAL)	Forward Calorimeter (FCAL)
Type	Scintillator	Scintillator	Scintillator	Straw Tube	Planar Chamber	Scintillator	Sci Fibers	Lead Glass
Channel Count	233 Fixed Array 120 movable	Hodo – 290 Counter – 16	30	3500	2304 anodes 10368 cathodes	176	2304 inner (768) 1536 outer (384)	2800
Signal Source	Fixed – PMT Movable – SiPM 3x3 mm	Hodo – 290 SiPM 3x3 mm Counter - PMT	120 SiPM, 3x3 mm, 4:1 Sum	Anode wires (dE/dx)	Anode wires Cathode Strips	PMT	SiPM Array Sum 1,2,3,4:1	PMT w/ CW
Physics Signal	100 pe	100 pe	100 pe	225 e	94 e	500 pe	250 pe/GeV	250 pe/GeV
Energy Resolution	0.1% (segment)	N/A	N/A	15%	15%	N/A	2% + 5%/√E	3.6% + 7.3%√E
Single Channel Time Resolution	100 ps	100 ps	350 ps	2 ns	1 ns anodes 5 ns cathodes	140 ps	150 + 50/√E ps	2 ns
Gain in Detector	10^6	10^6	10^6	2×10^4	4×10^4	10^6	1×10^6	8×10^5
Typical Charge	16 pC	16 pC	16 pC	1 pC	1.5 pC anodes 0.3 pC cathodes	80 pC	32 pC/GeV	32 pC/GeV
Dynamic Range	10	10	10	100 fC → 3 pC	Anodes: 300 fC → 3 pC Cathodes: 10 fC → 1pC	10	160 pC max 1.6 pC min 0.16 pC LSB	160 pC max 1.6 pC min 0.16 pC LSB
Preamp Gain	no	no	no	2 mV/fC	Anodes: 2 mV/fC Cathodes: 10 mV/fC	no	0.2 mV/uA	no
Maximum Single Channel Rate	5 MHz	1 MHz	10 MHz	3 kHz – 100 kHz	Anodes: < 280 kHz Cathodes: < 600 kHz	6 MHz	1.4 MHz	2 MHz
Discrimination	LE	LE	LE	no	Anodes: yes Cathodes: no	LE	Inner - LE	no
Scaler*	yes*	yes	yes*	no	no	no	no	no
FADC	12 bits 250 MSPS	12 bits 250 MSPS	12 bits 250 MSPS	12 bits 125 MSPS 1V diff FS	12 bits 125 MSPS cathodes	12 bits 250 MSPS	12 bits 250 MSPS 2.0V FS	12 bits 250 MSPS 0.5V FS
TDC	60 ps	60 ps	60 ps	no	115 ps anodes	60 ps	60 ps inner	no
Level 1 Trigger	Yes (low rate runs)	no	Track count	no	no	Track count	Energy sum	Energy sum

**Scalers are included in the fADC250*

Figure 1: Detector Subsystems

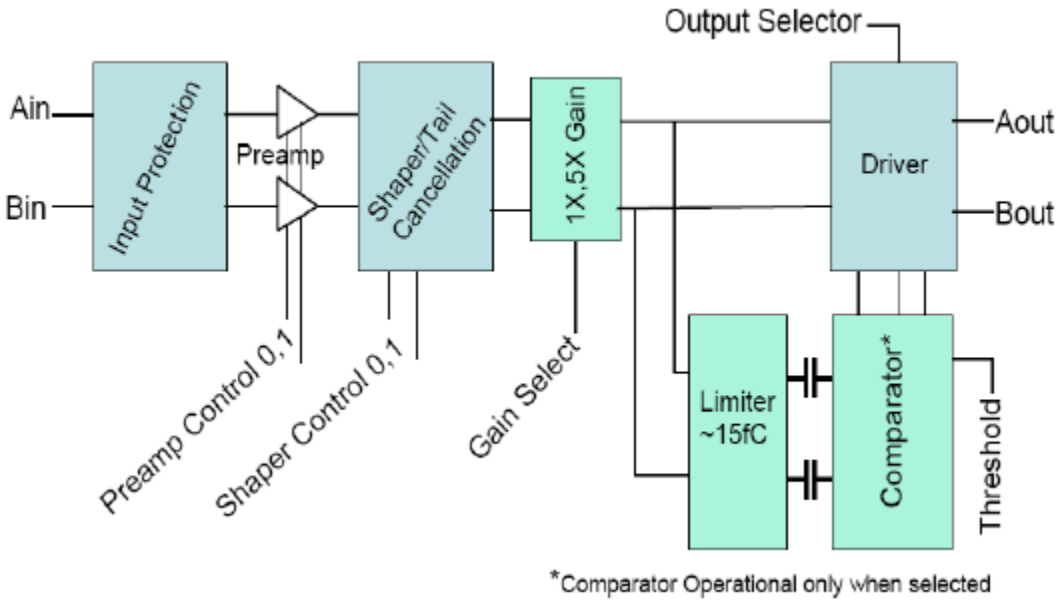


Figure 2: ASIC GASS-II Block Diagram

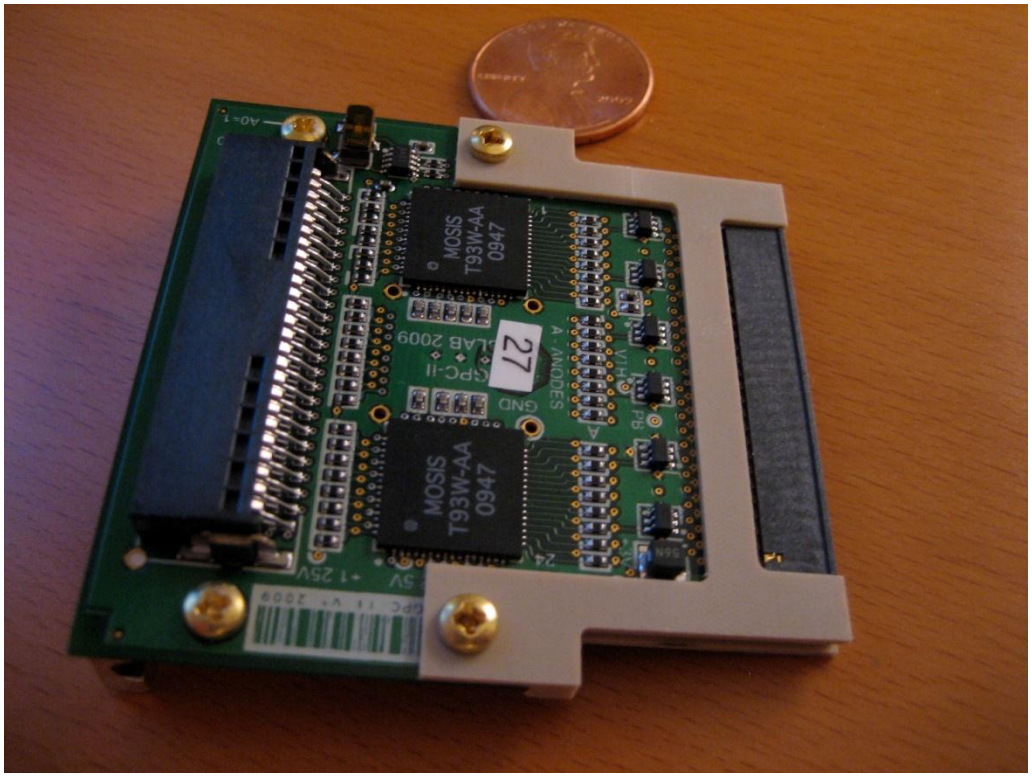


Figure 3: The GPC-II preamplifier card for the CDC and the FDC

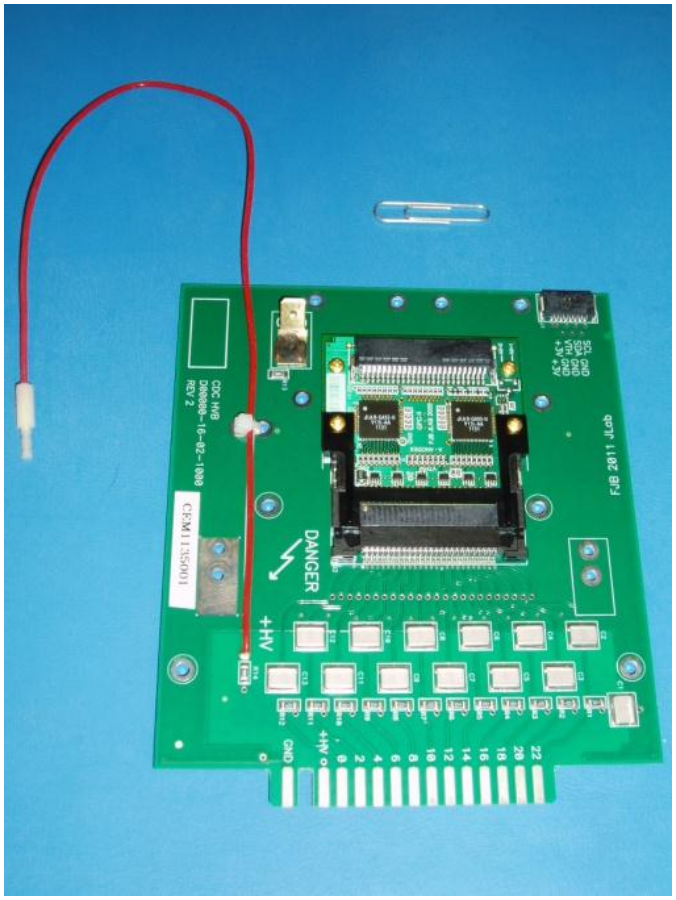


Figure 4: The CDC HVB with a preamp card installed

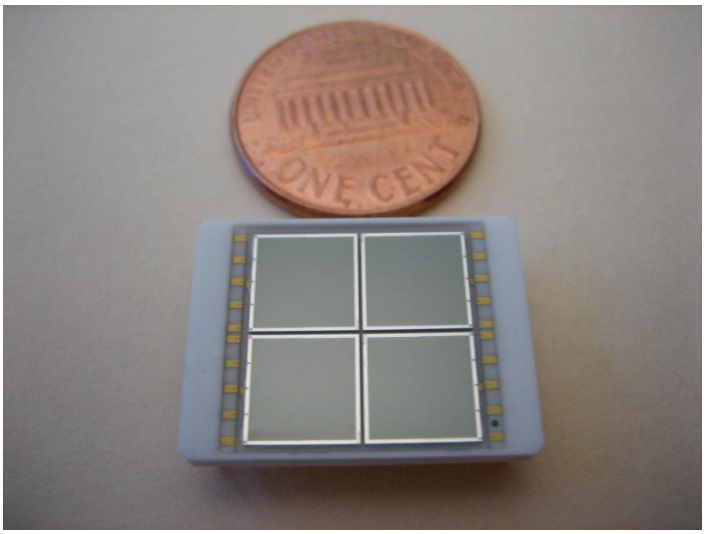


Figure 5: BCAL 4x4 SiPM array front view

Figure 6: BCAL 4x4 SiPM array rear view

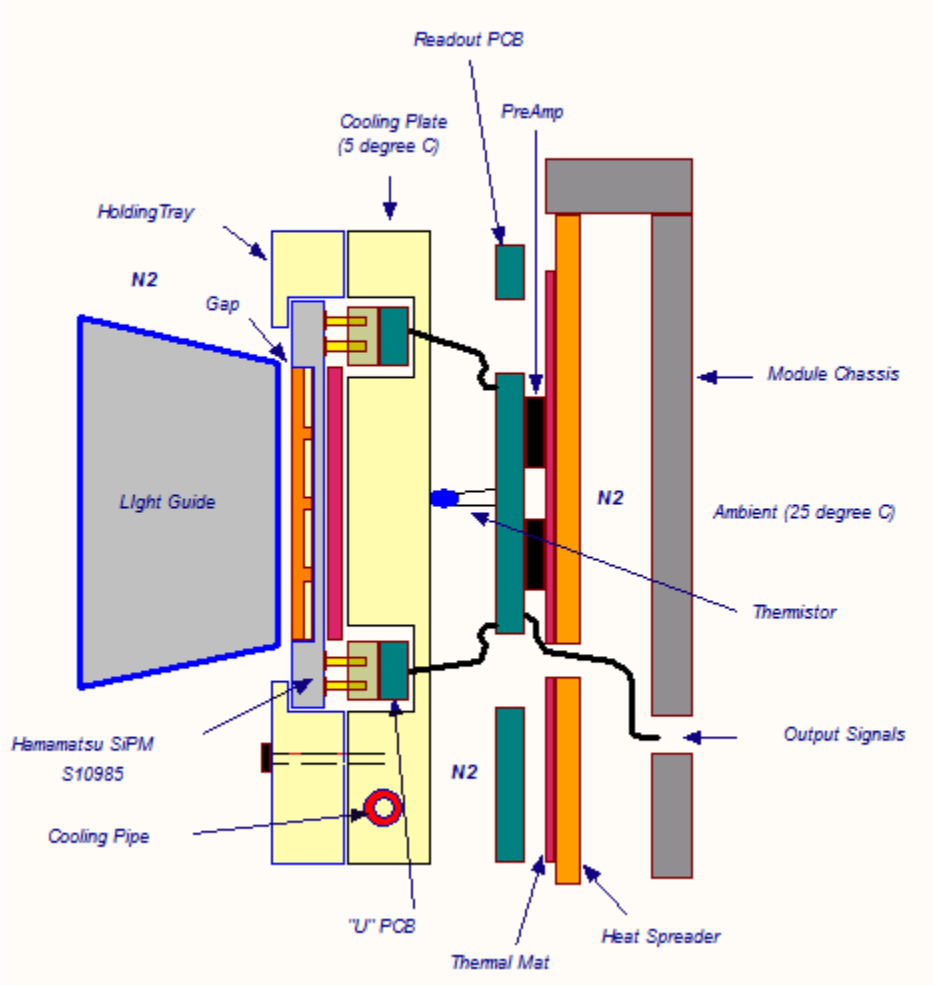


Figure 7: Diagram of cooling and readout implementation on the BCAL

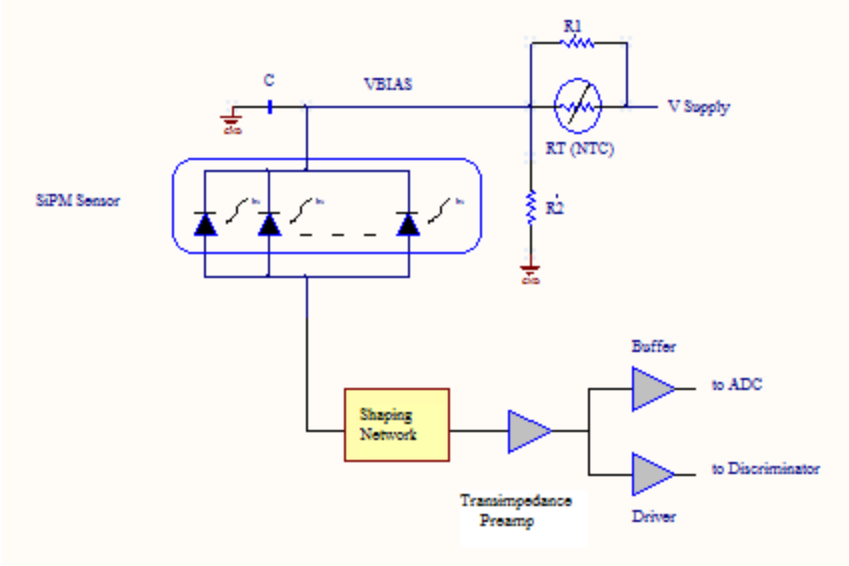


Figure 8: The SiPM readout architecture

Figure 9: The JLab VXS crate

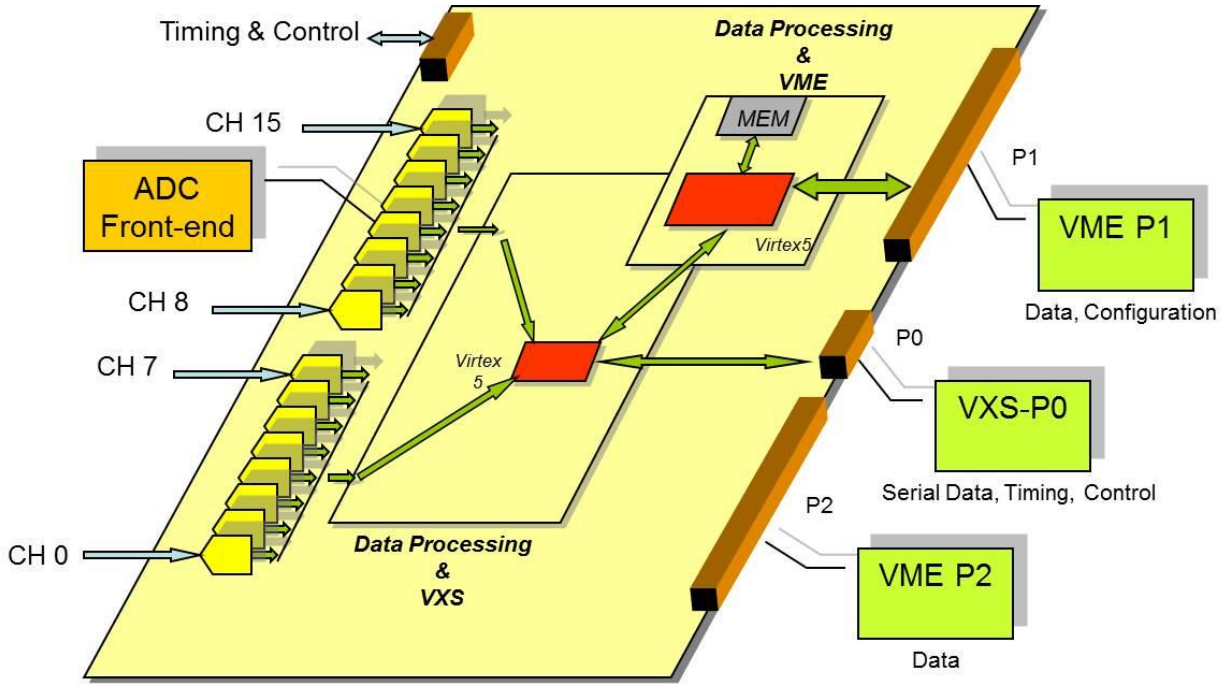


Figure 10: The fADC250 architecture

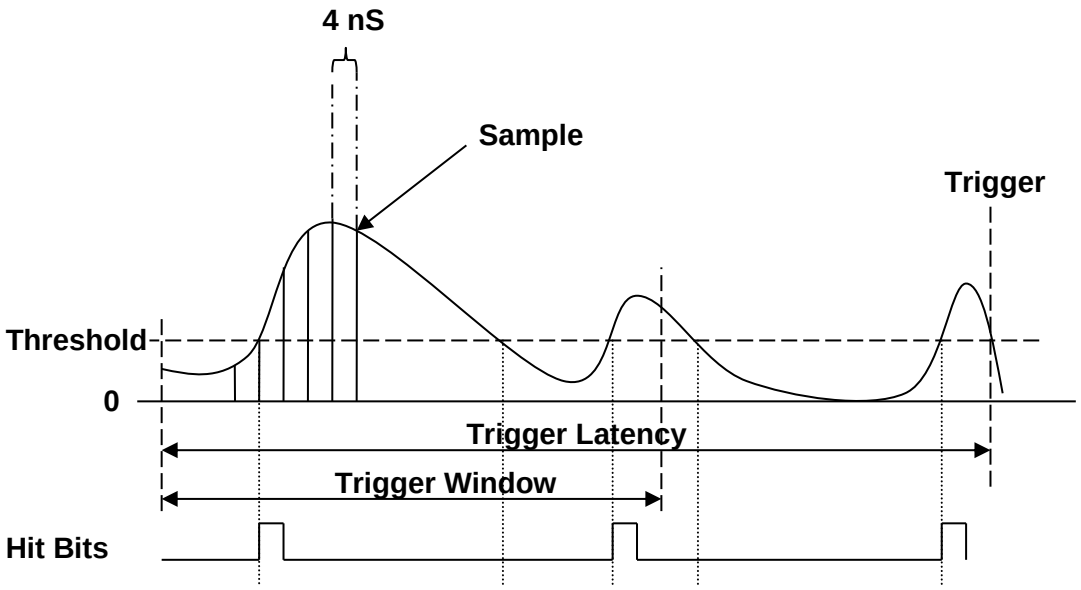
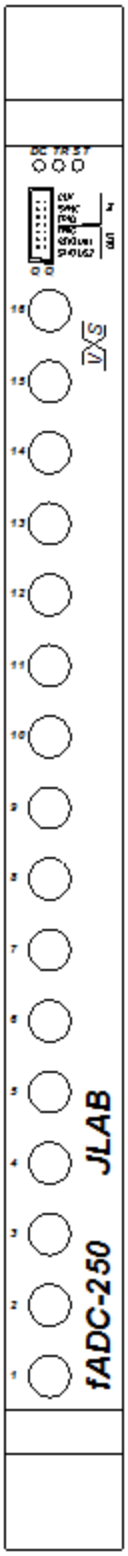


Figure 11: Sampling and triggering on the fADC250

Figure 12: The fADC250



fADC250

12-bit VXS flash ADC Module Specifications

Signal Inputs	Number	16 (50 Ohm, LEMO)
	Range	0.5V, 1V & 2V, Bipolar, User Selectable
	Offset	100% FS per channel via DACs
	Shaping	Anti-aliasing
	Crosstalk	<0.1%
Conversion Characteristics	Resolution	12-bit
	INL	± 0.5 LSB
	DNL	± 0.3 LSB
	SNR	64.9 dB @ 70 MHz Input, 250MSPS
	Data Latency	28 nS
Clock	Sampling	250 MSPS, Differential
	Jitter	0.5 ps RMS (internal)
	Source	Internal and External
Control Inputs/Outputs	Clock	IN – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe (Internal)
Trigger Latency	8 µS	
Data Memory	8 µS	
Data Processing	Algorithm dependent: Sparcification Windowing Raw Data, Charge, Pedestal Time (Linear Interpolation) Output (Backplane, VXS)	
Interface	VME64x – 2eSST Data Transfer Cycles 200 MB/sec	
Packaging	6U VXS	
Power	56W (+3.3V, +5V, +12V, -12V)	

FJB, JLAB, FADC_SPEC.DOC

Figure 13: Specifications Summary for the fADC250

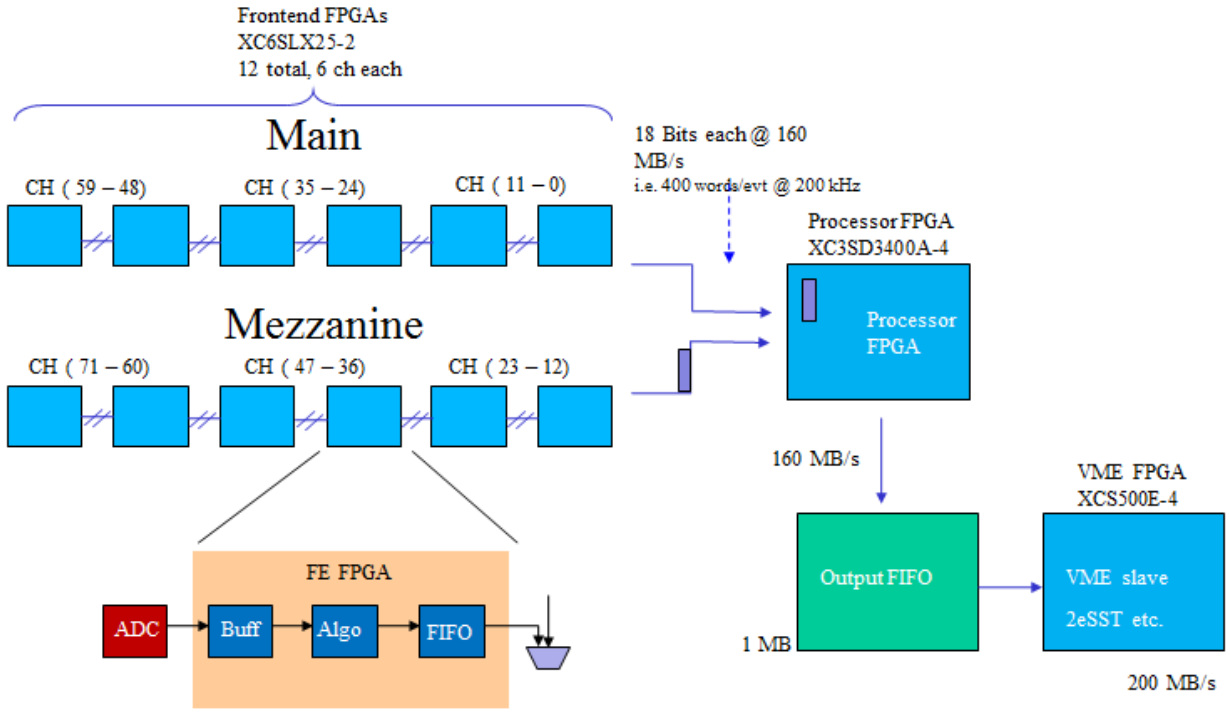


Figure 14: The fADC125 architecture

Figure 15: The fADC125

fADC125

12-bit VXS flash ADC Module Specifications

Signal Inputs	Number	72 (113 Ohm, Hi-Z CM, 3M 10250-1210PE connectors)
	Range	± 300 mV differential
	Offset	± 10% FS per channel via 12-bit DACs
	CMR	-1.75 V to +4.25V
	Shaping	Optimized for cable equalization, preamp characteristics and anti-aliasing.
	Crosstalk	<1%
Conversion Characteristics	Resolution	12-bit
	INL	± 0.4 LSB typical
	DNL	± 0.2 LSB typical
	SNR	70 dB @ 20 MHz Input
	Data Latency	64 nS
Clock	Sampling	125 MSPS, differential
	Jitter	< 4.5 pS RMS (internal)
	Source	Internal and External
Preamp Pulser	Number	3 (one per input connector onto 25th pair)
	Output	Current-mode, ± 10 mA differential
	Waveform	Conforms to preamp requirements
Control Inputs/Outputs	Clock	IN - Differential, CML, P2 (Backplane)
	Trigger	IN - Differential, CML, P2 (Backplane)
	Sync	IN - Differential, CML, P2 (Backplane)
	Busy	OUT – Active-low, open-collector, P2 (Backplane)
Trigger Latency	Up to 13.5 µS	
Data Memory	16.4 µS acquisition buffer; 1 MByte output data FIFO	
Data Processing	Algorithm dependent: Sparcification, Windowing, Raw Data, Charge, Pedestal Time (Over Threshold, Relative to trigger), Filtering	
Interface	VME 64x – 2eSST Data Transfer Cycles 200 MB/sec	
Packaging	6U VXS	
Power	67W (+3.3V, +5V, +12V, -12V)	

FIR, JLAB FADC125_SPEC.DOC

Figure 16: Specifications Summary for the fADC125

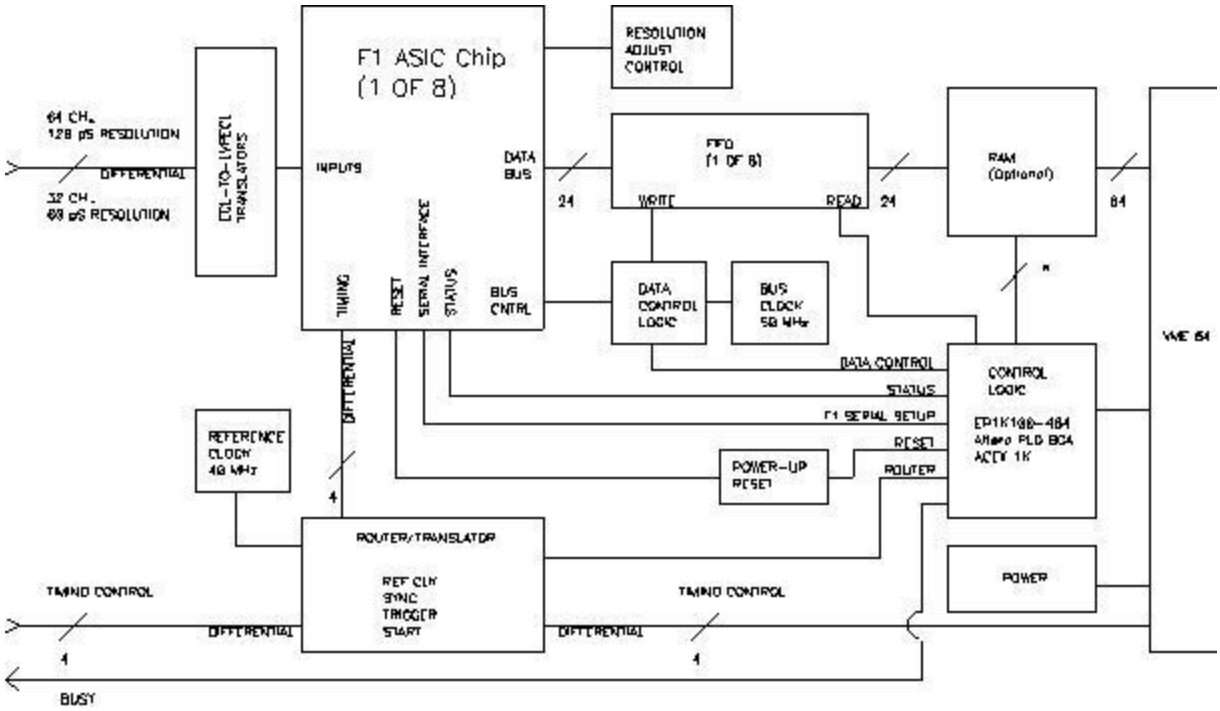


Figure 17: Block diagram of the early F1TDCV1

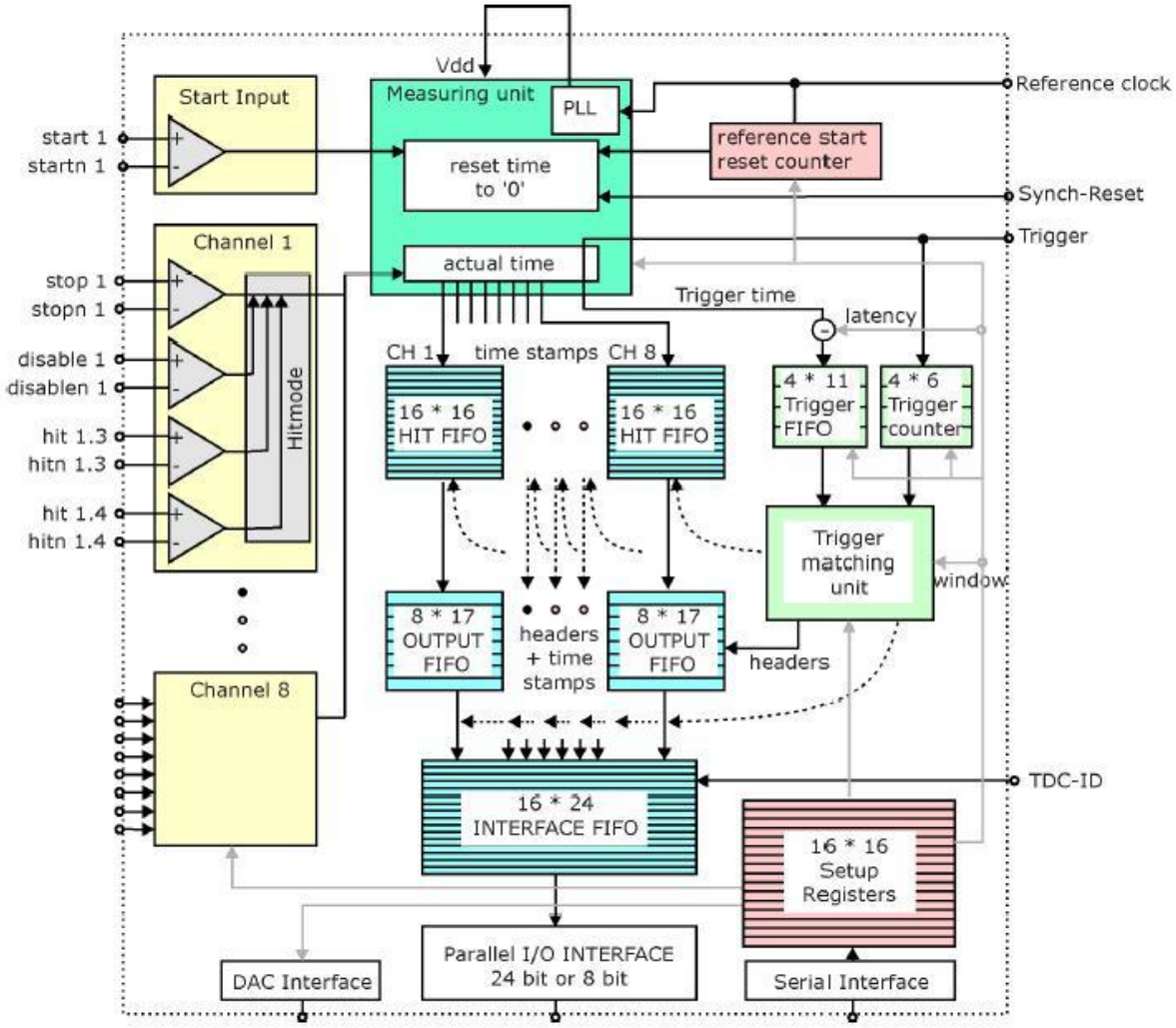


Figure 18: F1 ASIC block diagram

Figure 19: F1TDCV2

F1TDCV2

High Resolution VXS flash TDC Module Specifications

Signal Inputs	Number	32 (110 Ohm, 0.1" header connectors)
	Range	ECL, Differential
Conversion Characteristics	Resolution	60ps
	INL	0 LSB
	DNL	10-50% LSB
	Sigma	1.1 LSB, typical
	Dynamic Range	3.6µs @ 56ps LSB
Clock	Frequency	31.25MHz external, 32MHz internal
	Stability	100ppm (internal)
	Source	Internal and External, differential
Control Inputs/Outputs	Clock	LVPECL, Differential
	Trigger	ECL, Differential
	Syncres	ECL, Differential
	Start	ECL, Differential (test mode only)
	Busy	ECL, Differential
Acquisition	Trigger matching with zero suppression Programmable trigger window and latency	
Data Memory	1 M TDC data words	
Interface	VME64x – 2eSST Data Transfer Cycles 200 MB/sec	
Packaging	6U VXS	
Power	45W (+3.3V, +5V, +12V, -12V)	

F1B, JLAB, F1TDCV2_SPEC.DOC

Figure 20: F1TDCV2 specifications

Figure 21: F1TDCV3

F1TDCV3

Low Resolution VXS flash TDC Module Specifications

Signal Inputs	Number	48 (110 Ohm, 3M 10250-1210PE connectors)
	Range	LVDS
Conversion Characteristics	Resolution	100ps
	INL	0 LSB
	DNL	10-50% LSB
	Sigma	0.9 LSB, typical
	Dynamic Range	7.2µs @ 112ps LSB
Clock	Frequency	31.25MHz external, 32MHz internal
	Stability	100ppm (internal)
	Source	Internal and External, differential
Preamp Pulser	Number	2 (one per input connector onto 25th pair)
	Output	Current-mode, ± 10 mA differential
	Waveform	Conforms to preamp requirements
Control Inputs/Outputs	Clock	LVPECL, Differential
	Trigger	ECL, Differential
	Syncres	ECL, Differential
	Start	ECL, Differential (test mode only)
	Busy	ECL, Differential
Acquisition	Trigger matching with zero suppression Programmable trigger window and latency	
Data Memory	0.8 M TDC data words	
Interface	VME64x – 2eSST Data Transfer Cycles 200 MB/sec	
Packaging	6U VXS	
Power	37W (+3.3V, +5V, +12V, -12V)	

Figure 22: F1TDCV3 specifications

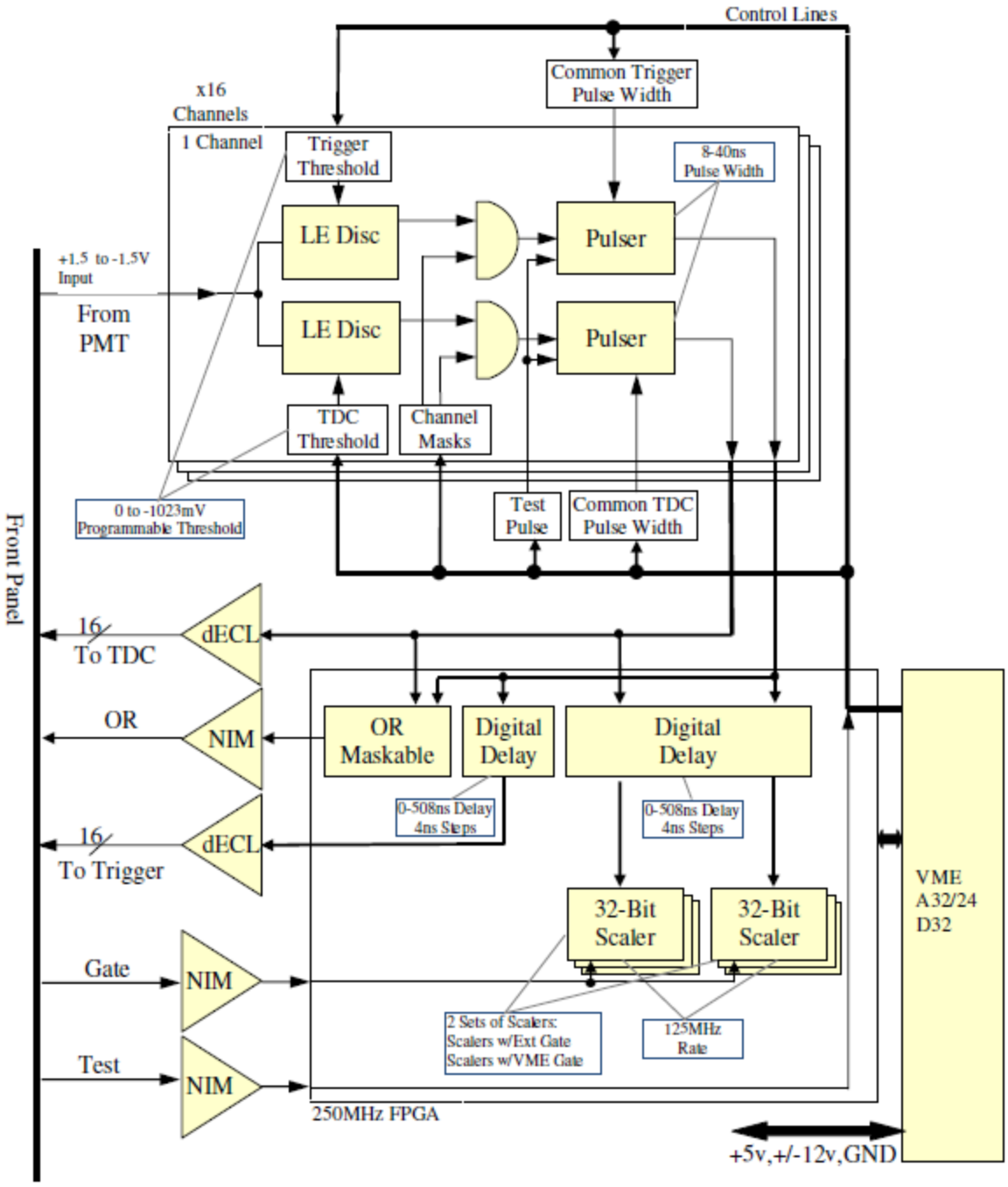
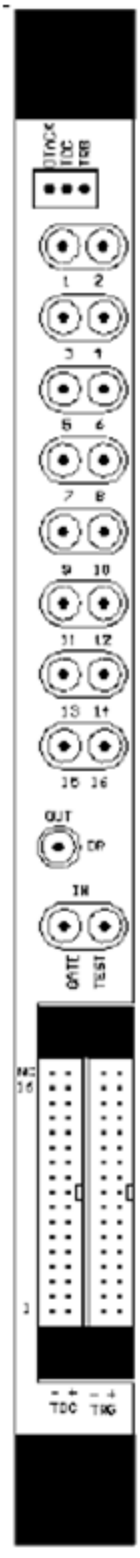


Figure 23: JLab Discriminator block diagram

Figure 24: The JLab 16-ch Discriminator



Discriminator

VME64x, 16-ch Module Specifications

Signal Inputs	Number	16 (50 Ohm, LEMO)
	Range	1.5V, Bipolar, DC-coupled, clamped
	Crosstalk	<0.1%
Characteristics	Threshold	0 to -1023mV, 10-bit, Dual
	Type	Non-updating
	Dispersion	<50ps
	Rate	80MHz with 8ns pulse width
	Width	8ns to 40ns
	Deadtime	4ns to 10ns
	Hysterisis	5mV
	Noise	<2mV RMS
	Offset Err	<1mV typical
Outputs	Range	ECL, Differential, Dual
	Connector	34-pin, 0.1" headers
	TDC Out	8ns to 40ns common width, programmable mask
	TRG Out	4ns to 60ns common width, programmable mask
	Delays	IN to TDC Out <6ns
		IN to TRG Out - 15ns
Scalers	Number	2 per threshold, 1 gated and 1 free running
	Width	32-bit
	Input	Digital delay
	Gating	External and free running
	Rate	125MHz
	Control	VME latch, read, clear, overflow
Control Inputs/Outputs	Gate	IN, Gates scalers, NIM, LEMO
	Test	IN, pulses discriminator outputs, NIM, LEMO
	OR	OUT, NIM, LEMO
Interface	VME A32/A24, D32	
Packaging	6U VXS	
Power	30W (+5V, +12V, -12V)	

Figure 25: JLab Discriminator specifications

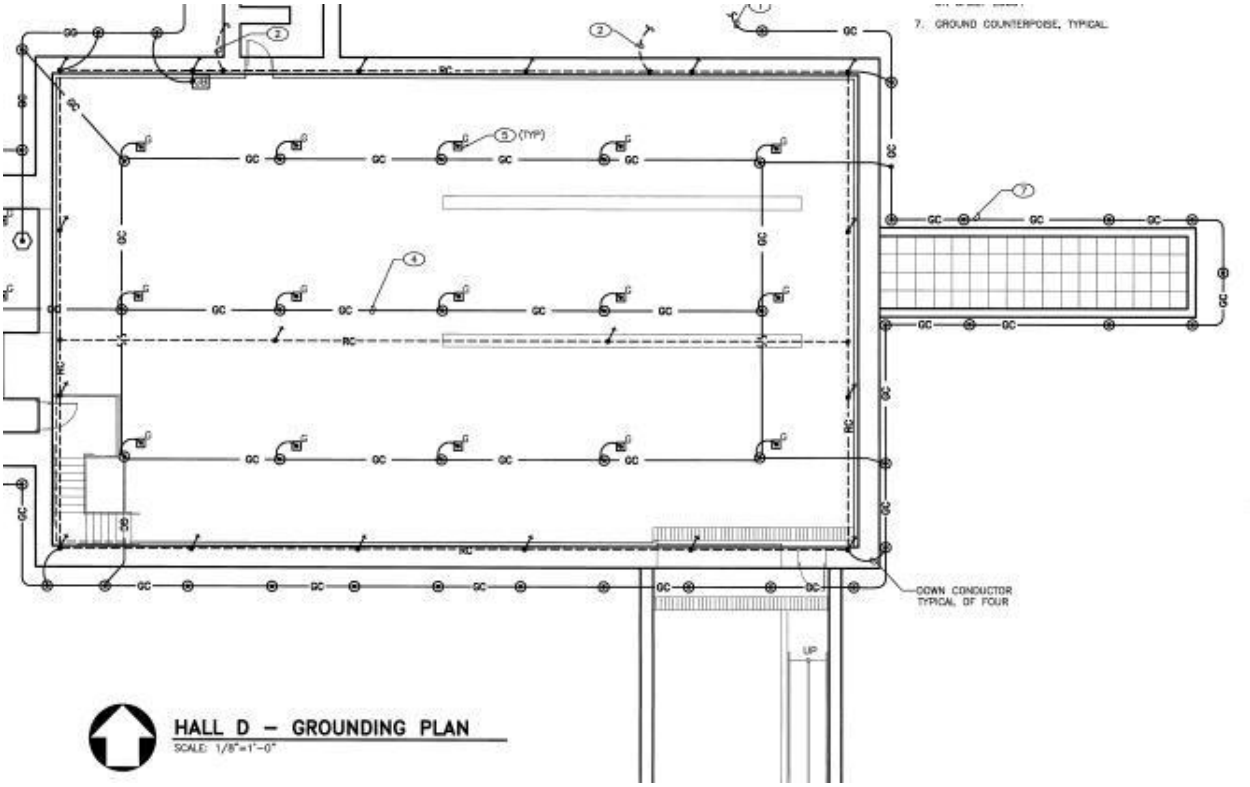


Figure 26: Grounding grid in Hall D

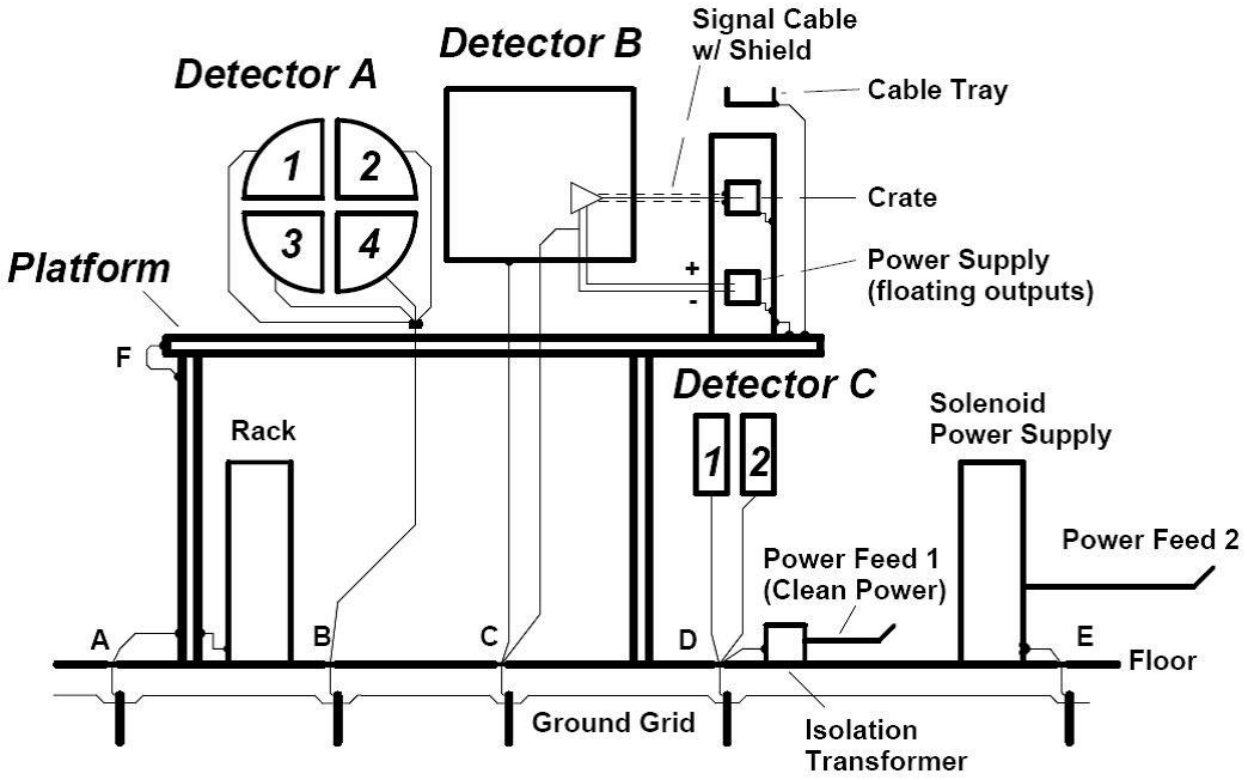


Figure 27: Grounding implementation

Figure 28: LV distribution chassis

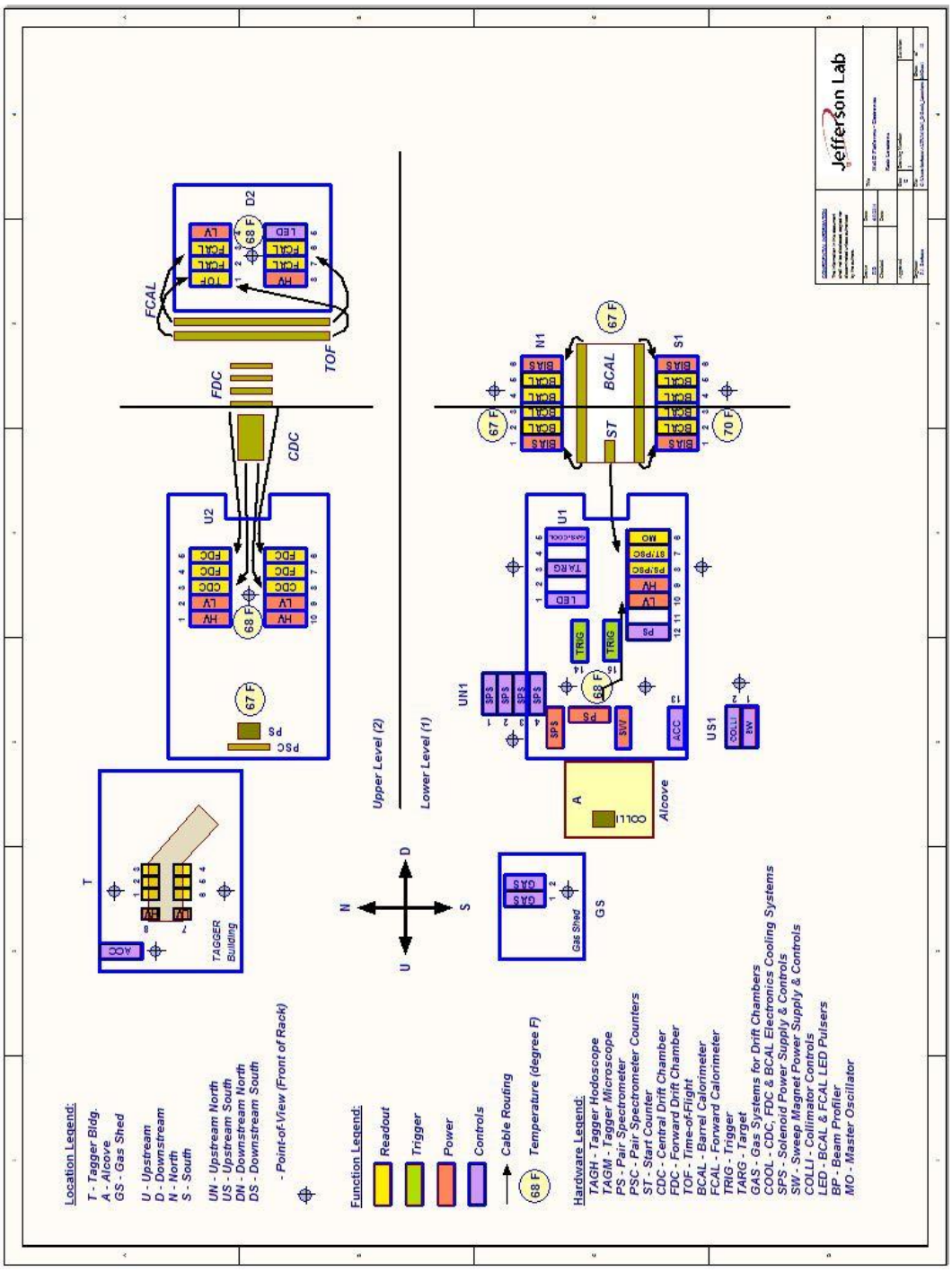


Figure 29: Rack locations

Figure 30: Electronics installation

Summary of GlueX Electronics

Detector →	Photon Tagger (TAGH/TAGM)	Pair Spectrometer (PS/PSC)	Start Counter (ST)	Central Drift (CDC)	Forward Drift (FDC)	Time-of-Flight (TOF)	Barrel Calorimeter (BCAL)	Forward Calorimeter (FCAL)	TOTAL
GueX ASIC *8 Channel, ASD* *0.25 µm CMOS*	no	no	no	450	1584	no	no	no	2034
Preamp Card *24-Ch*	no	no	no	149	528	no	no	no	677
fADC125 V2 *72 Ch, VXS* *12-bit, 125 MSPS*	no	no	no	50	144	no	no	no	194
fADC250 V2 *16 Ch, VXS* *12-bit, 250 MSPS*	23	20	2	no	no	11	96	176	328
F1TDC V2 *32 Ch, VXS, 57 ps*	12	1	1	no	no	no	36	no	50
F1TDC V3 *48 Ch, VXS, 97 ps*	no	no	no	no	48	no	no	no	48
CAEN VX1290A TDC *32 Ch, VME64X, 25 ps*	no	no	no	no	no	6	no	no	6
Discriminator *16 Ch, VME64x, LE*	23	1	2	no	no	11	72	no	109
VME Crate	2	1	←	no	no	1	4	no	8
VXS Crate	3	2	2	4	14	2	12	12	53
HV - A1550P *24 Ch, +5 Kv, 1 mA*	no	no	no	6	4	no	no	no	10
HV – A1550N *24 Ch, -5 kV, 1 mA*	no	no	no	no	4	no	no	no	4
HV – A1535SN *24 Ch, -3.5 kV, 3 mA*	10	1	no	no	no	8	no	no	19
HV Mainframe *SY1527LC*	2	1	no	1	1	1	no	no	6
LV- MPOD MPV8xxx *DC, SiPM*	1(8V) 1(120V)	1(8V)	1(8V)	3(8V)	9(8V) 1(30V)	no	8(8V)	no	25
LV- MPOD ISEG *SiPM Bias*	no	5(100V)	2(100V)	no	no	no	24(100V)	no	31
LV Mainframe *MPOD*	1(mini)	1	←	1	1	no	4	no	7+1
LV-FCAL *24V*	no	no	no	no	no	no	no	Custom 1U chassis	4
Racks Total	8 (short)								47+8

Figure 31: Summary of installed electronics in Hall D