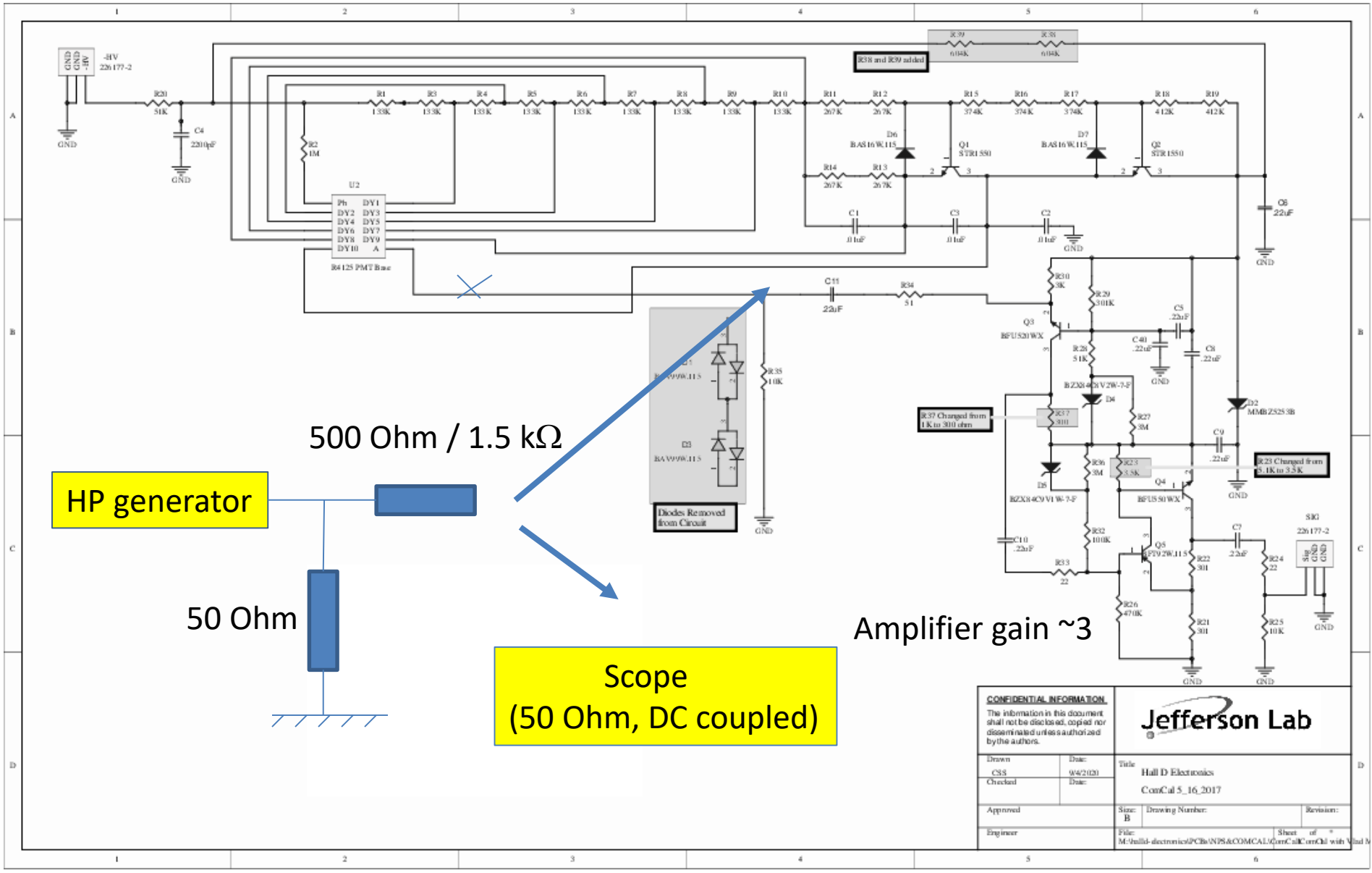
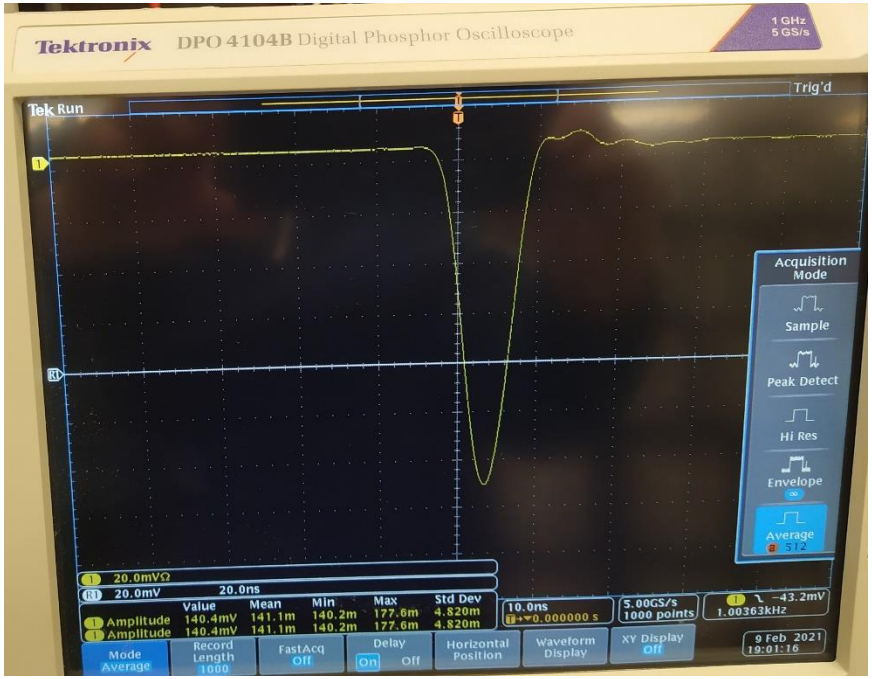
Active base designed for NPS (Hall C)

V, Popov

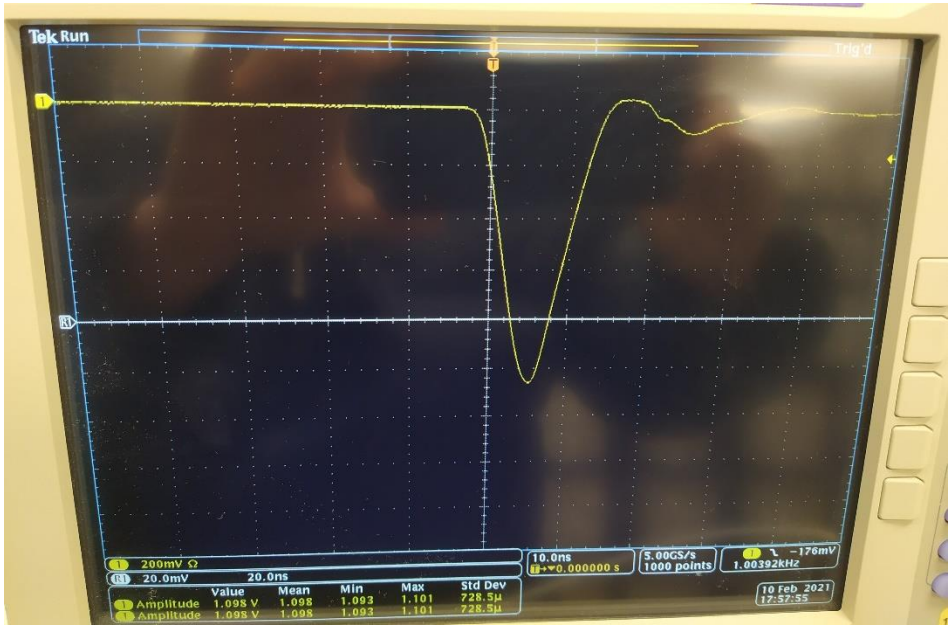


Possible bias/systematics of measurements (?)

Signal pulse from generator

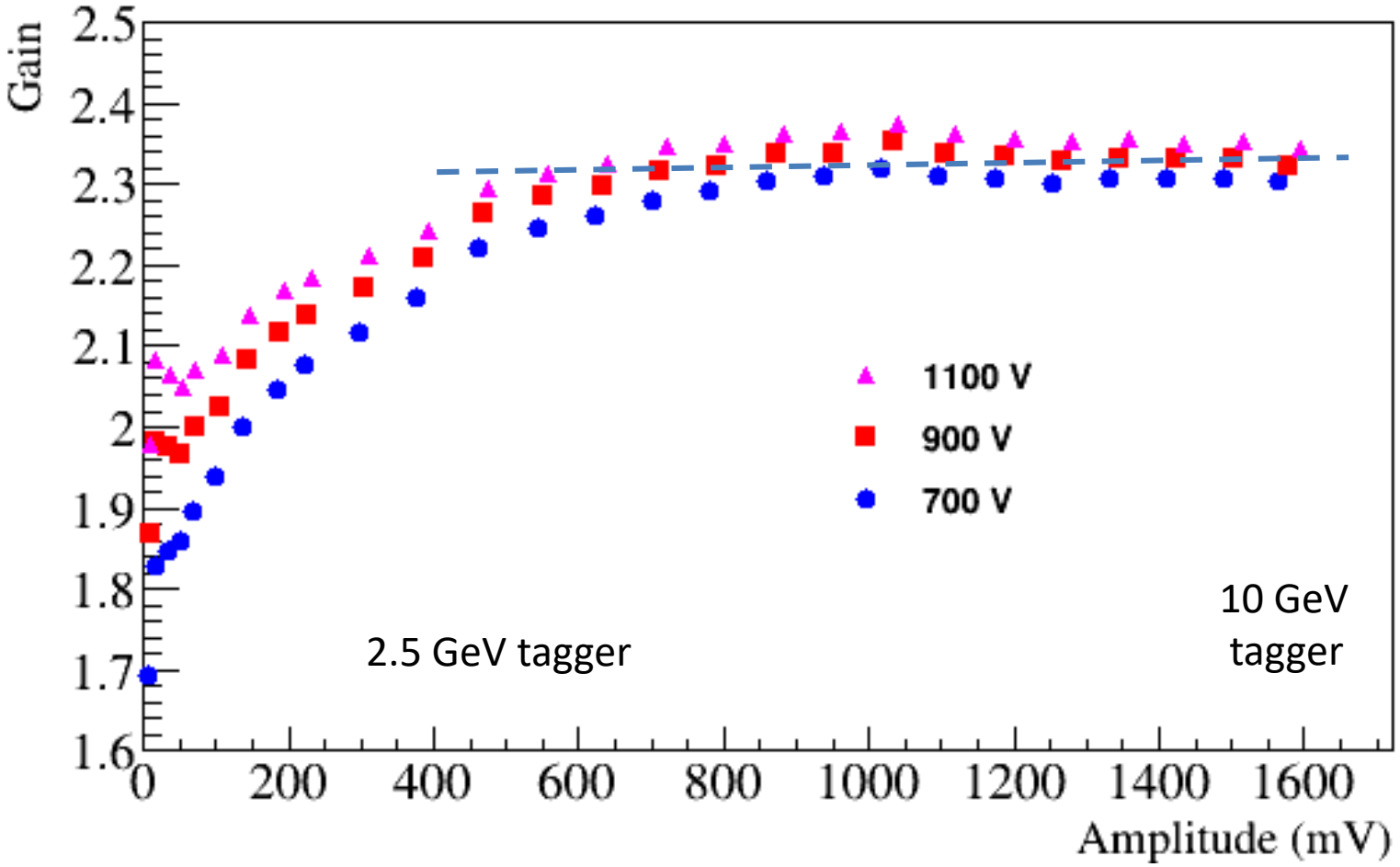


Amplified signal pulse



full width ~10 ns

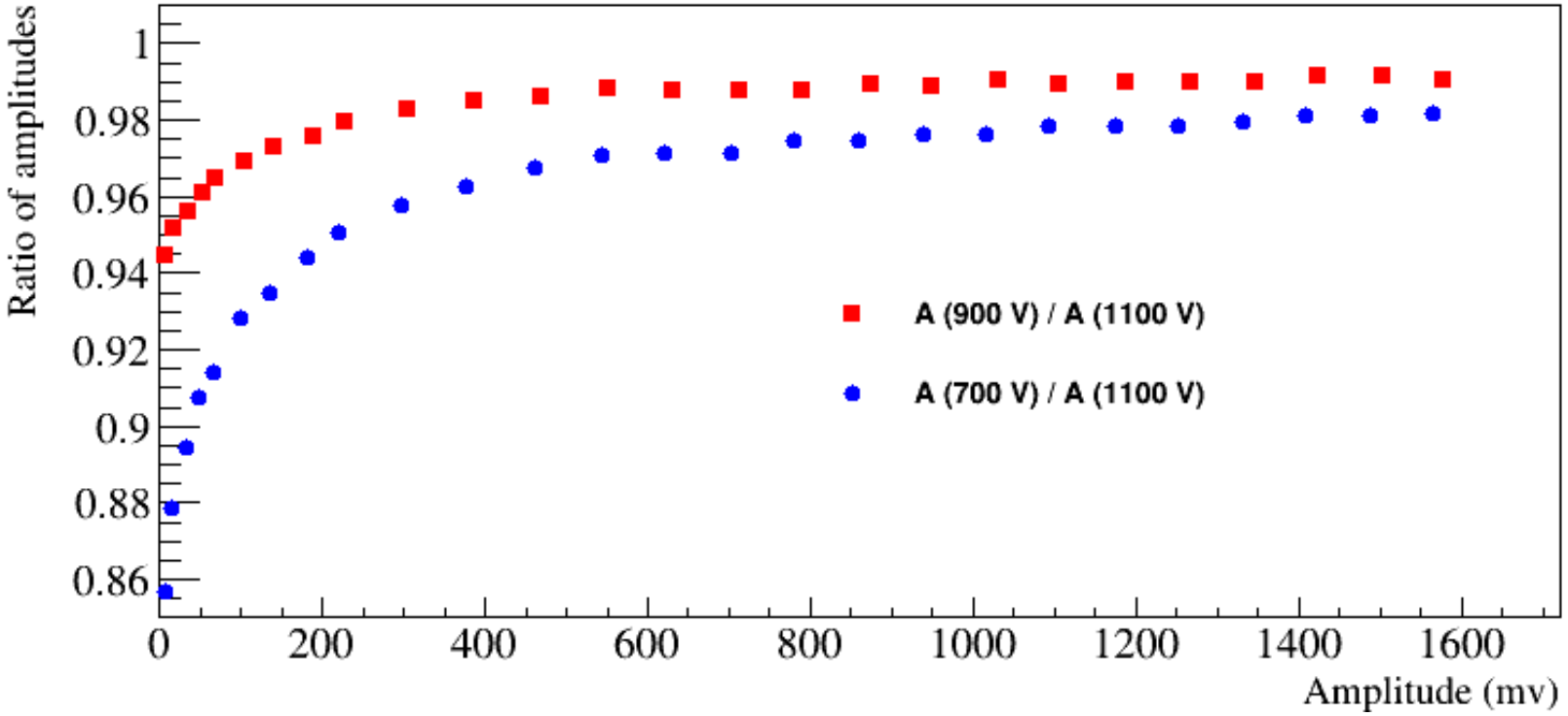
Amplifier Gain (A_{amp} / A_{HP})



- Relatively stable gain for large amplitudes between 0.5 V and 1.6 V
- Non linearity on the level of 10 % below 0.5 V

Non linearity for different divider current

700 V - 700 μ A
900 V - 900 μ A
1100 V - 1.1 mA



- Better linearity at larger divider currents

Discussion

Measured gain verified our beam tests results
(if measured the gain correctly . . .)

FCAL:

- An amplifier will be needed for inner FCAL insert layers, though with a relatively small gain between 3 and 6.

- Possible solutions to improve the amplifier:

  - use on-board amplifier, provide additional power to the amplifier (decouple power for divider and amplifier), use one extra cable to each PCB

  - use external amplifiers for modules in inner layers (place inside dark room ?)

  - apply non-linearity corrections for already existing bases

Discussion

CCAL:

- Estimated the anode current to be relatively small for PrimEx runs, a few micro amps. We can operate the base without an amplifier
  (use an amplifier with a small gain x3 as a backup) .

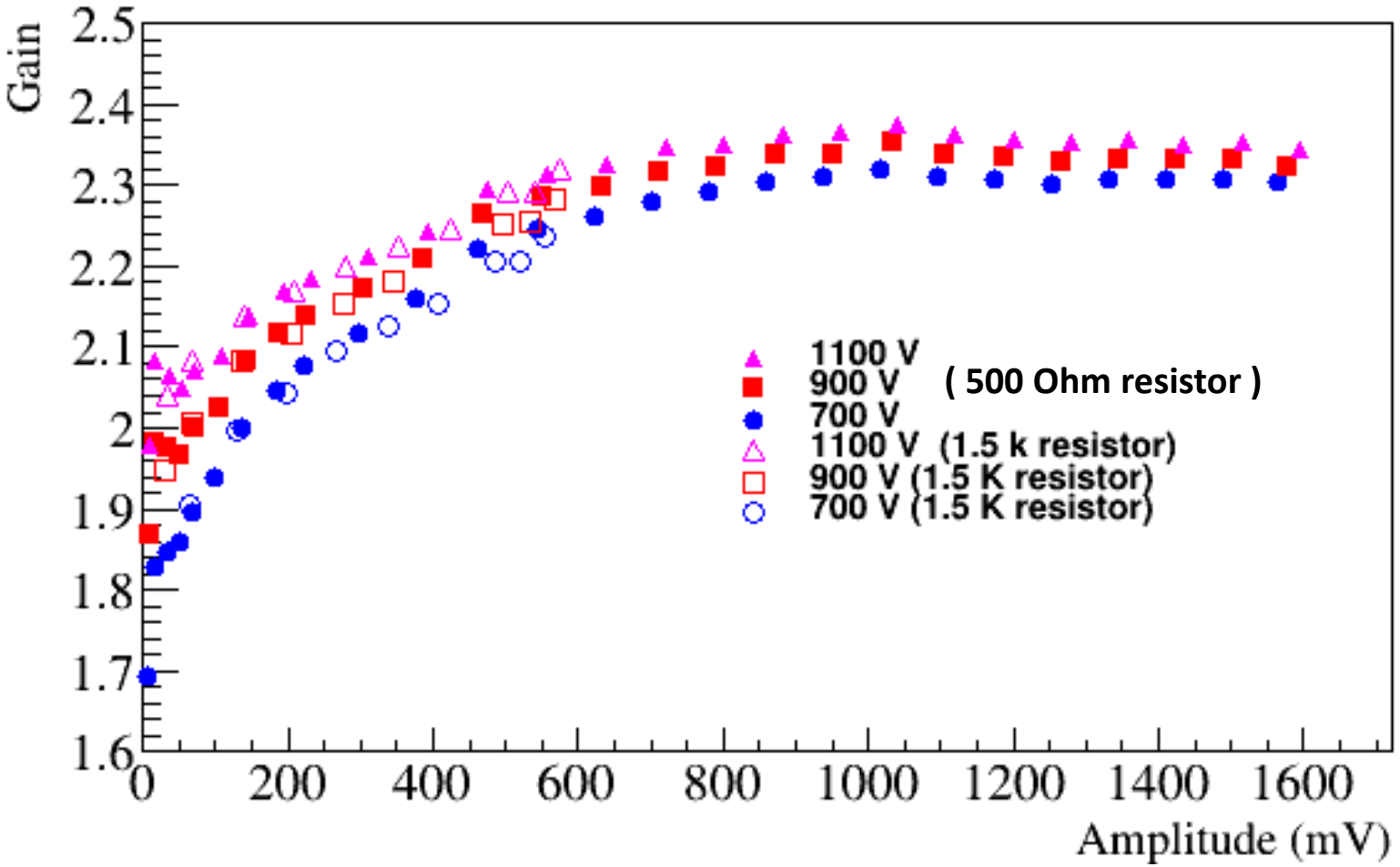
Note, we can change the ADC voltage range from 2 V to 0.5 V, if really needed

- Performance of the modified divider with the stabilization on last dynodes is good (checked)

- Order dividers for the CCAL with a switchable gain
  bypassed (default) / gain of 3 (optional, exists on the PCB)

Amplifier Gain (A_{amp} / A_{HP})

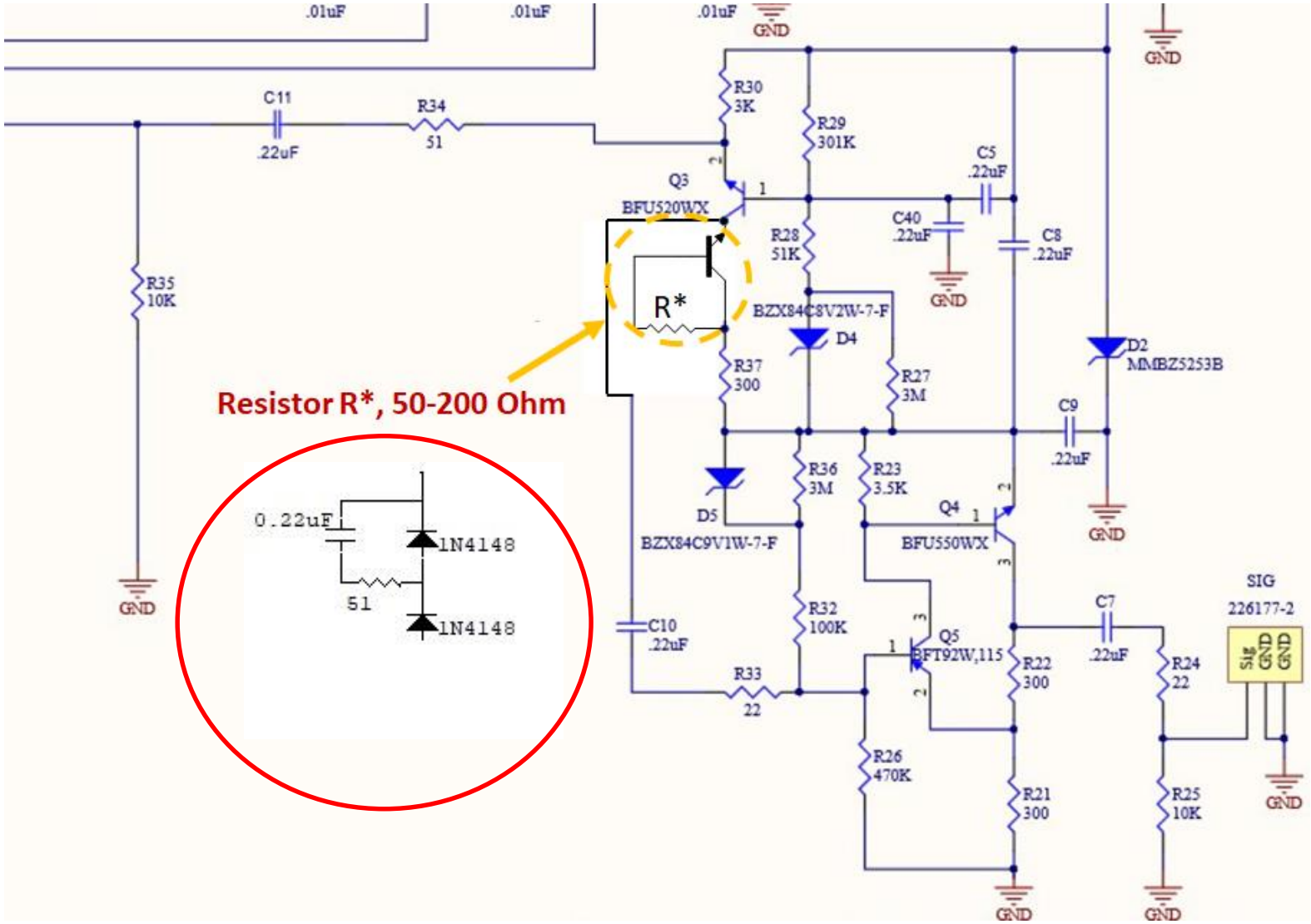
Use different 'injection' resistors.
compare measurements for 500 Ohm and 1.5 kΩ



Modifications of the base

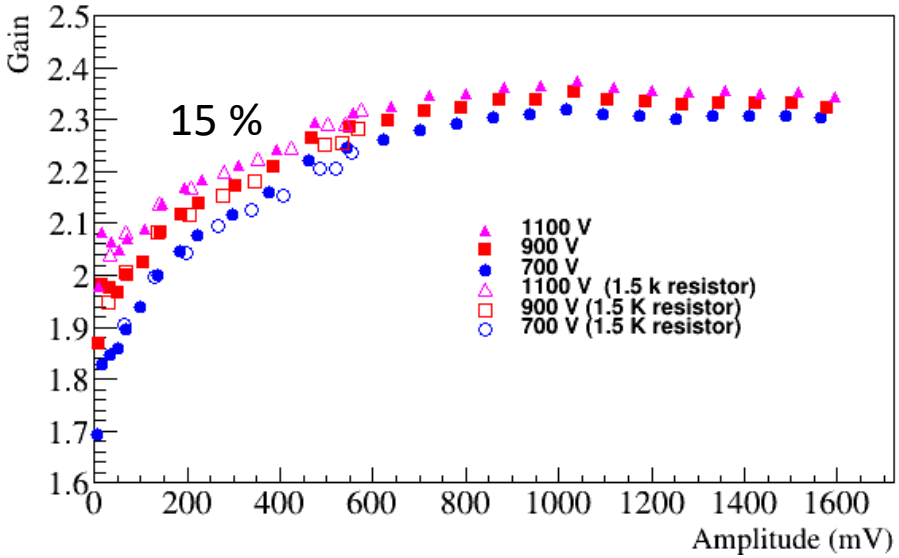
V, Popov

Some attempts to linearize performance

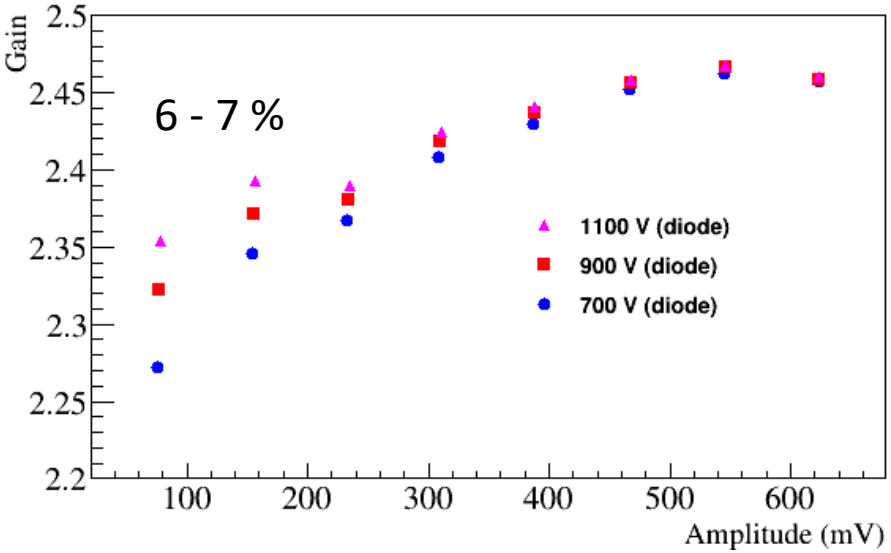


Amplifier Gain (A_{amp} / A_{HP})

Default amplifier

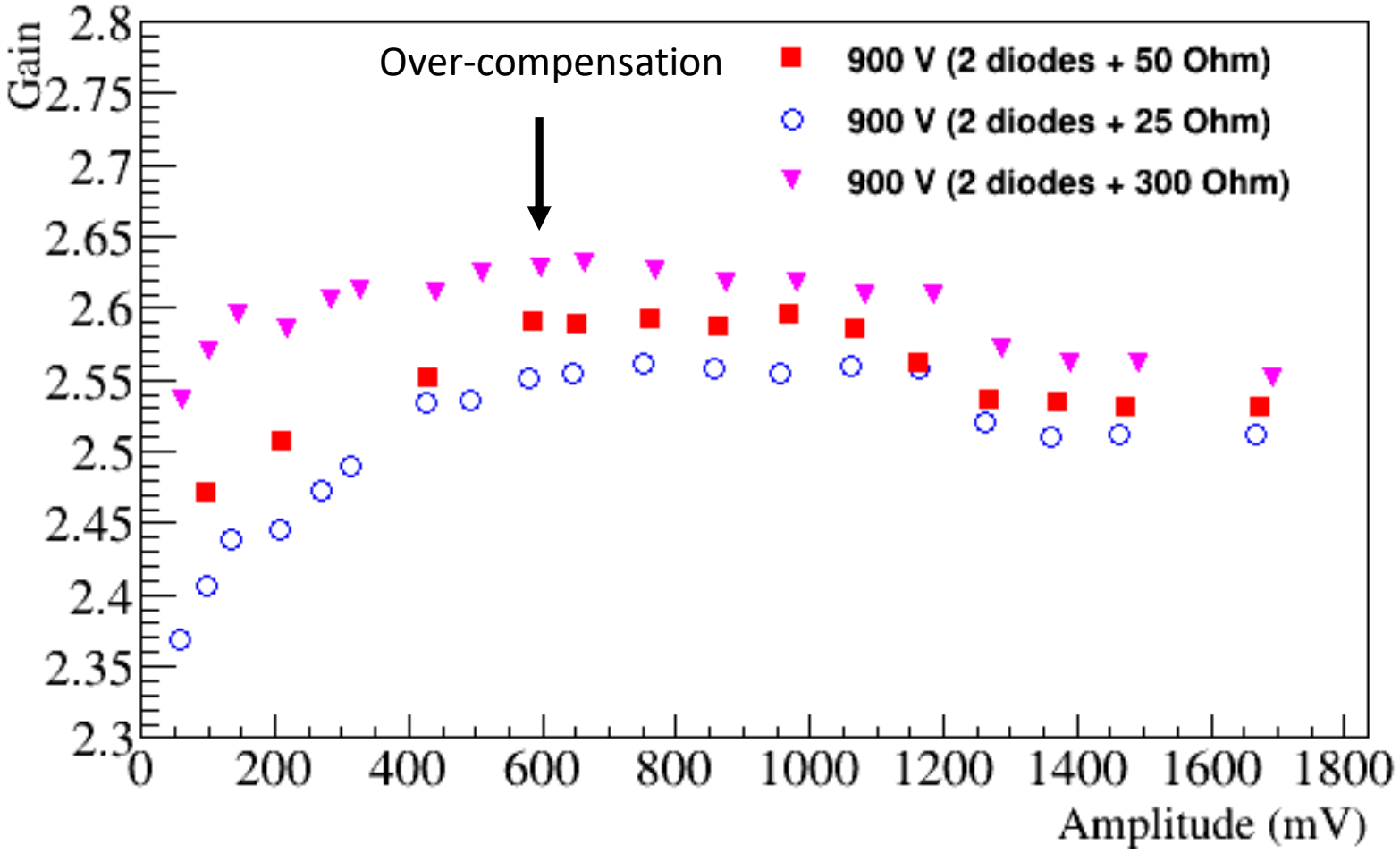


Add a diode



Two diodes

HP resistor 1 kΩ



Discussion

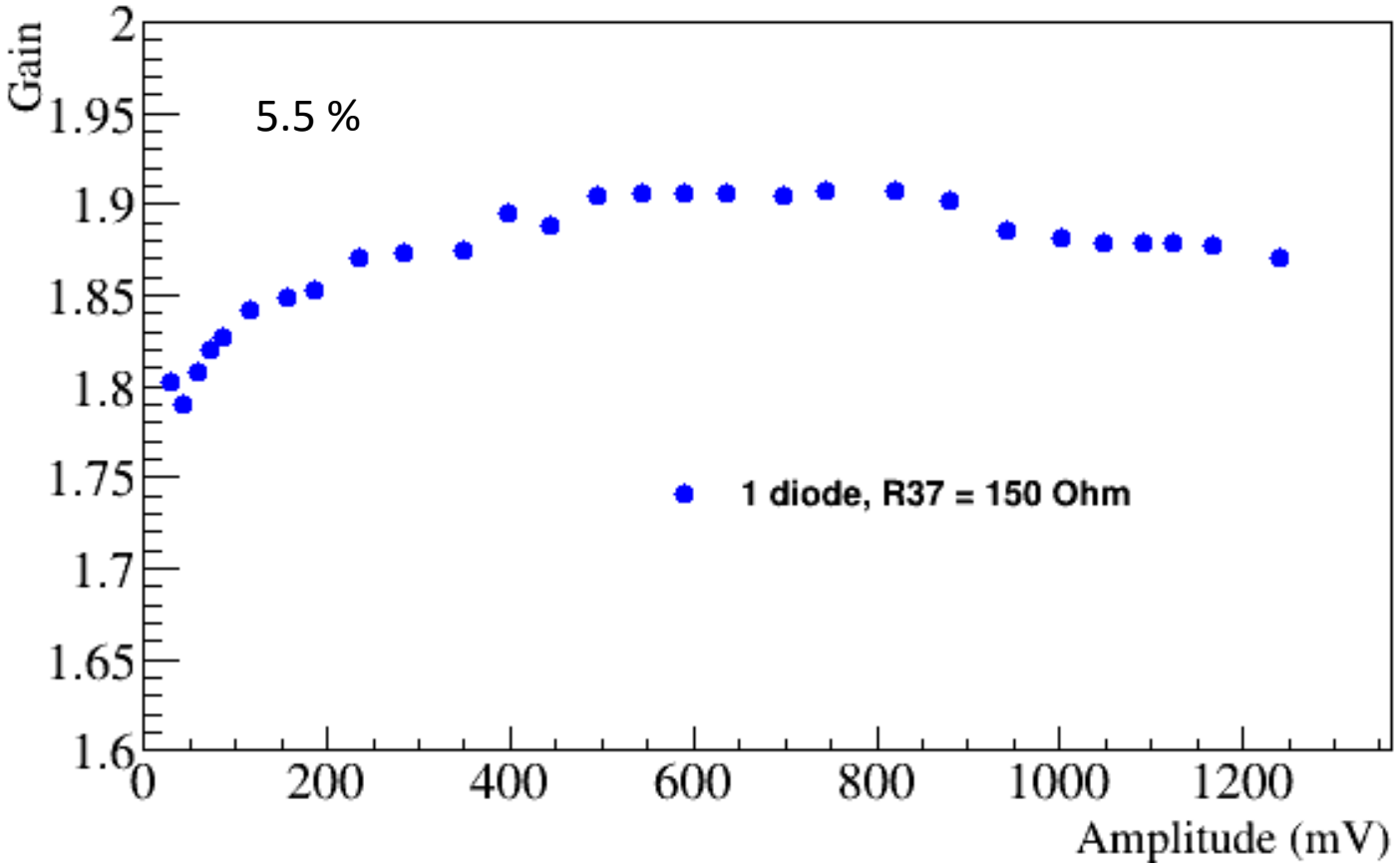
- Test 1 – 2 options
- Start redoing dividers for CCAL.

  Default: bypassed amplifier

  Optional: gain of 3, the best we can get
  no space on the existing PCB for the 2-diode scheme
- May continue with the divider optimization when the lab is re-opened
- Consider on-board OPS bases amplifier (Fernando's design)
  - perform tests in the lab
- Prepare new dividers and install them after the PrimEx run
  - test with the SRC experiment during this year

Single Diode

$R_{HP} = 1\ k\Omega$



Latest measurements:

- single diode

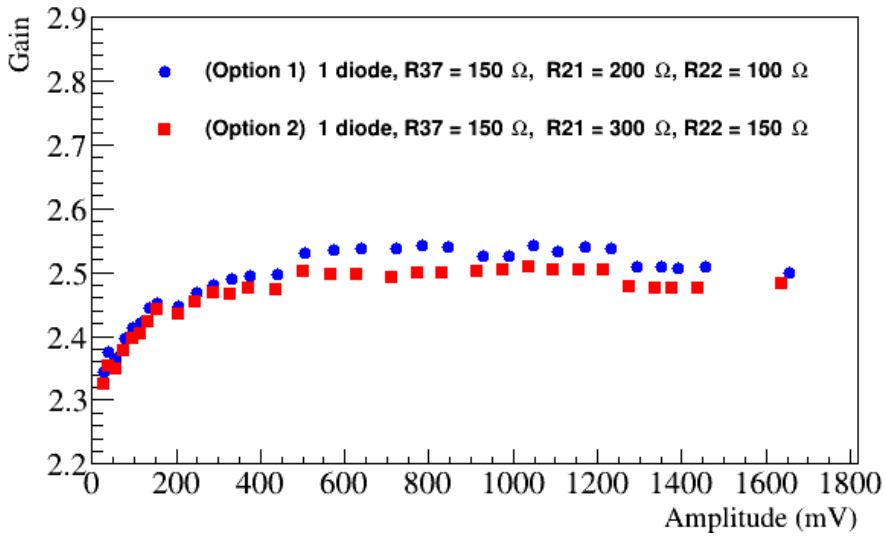
- change R37 from 200 Ohm to 150 Ohm
  (reduce gain on the first cascade)

- modify R21/R22
  (gain compensation on the second stage)

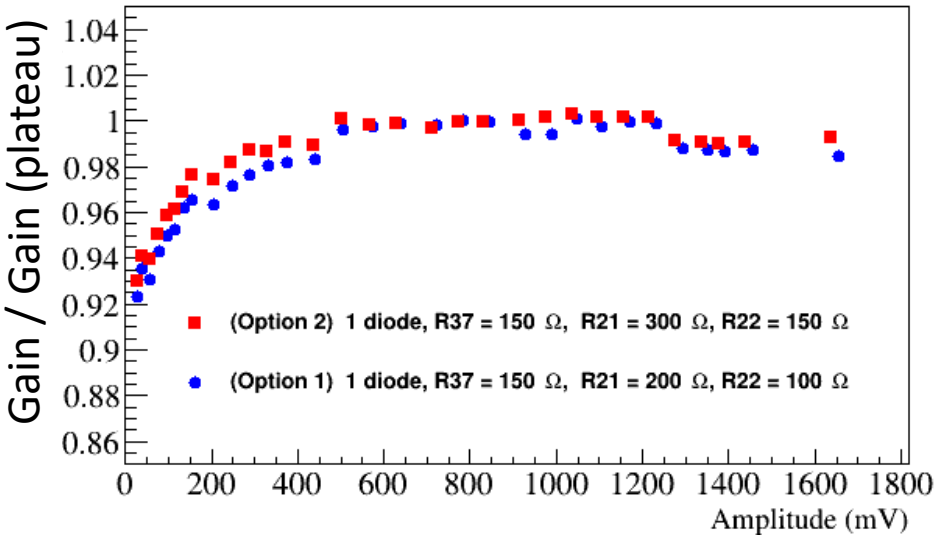
Gain

$R_{HP} = 1\ k\Omega$

Gain

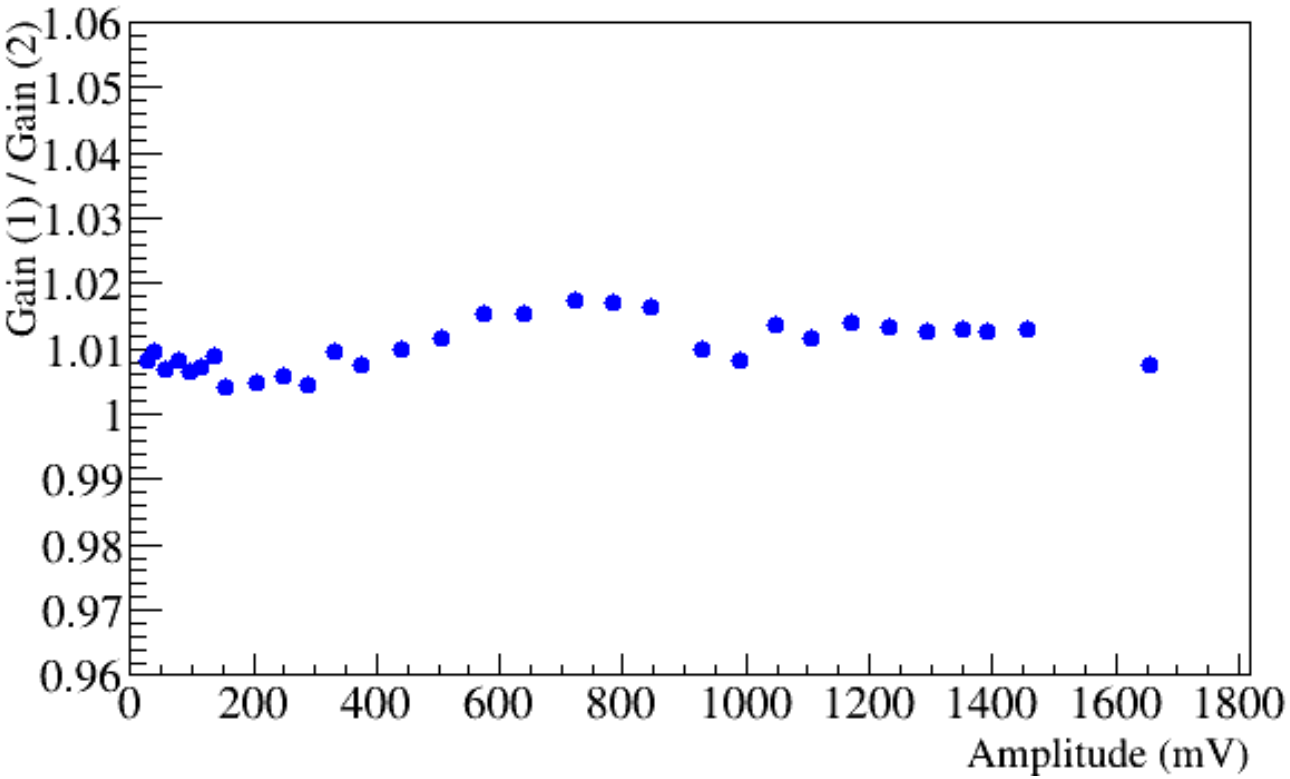


Normalized gain



Gain Ratio

Gain ratio (Option 1 / Option 2)



Checked Dividers (no amplifier) using an LED

Divider originally installed on CCAL

- checked with beam (operated at about 1 kV)

- 400 μA at 1 kV

Divider from Vlad's column 4 (increase voltages on the first dynodes)

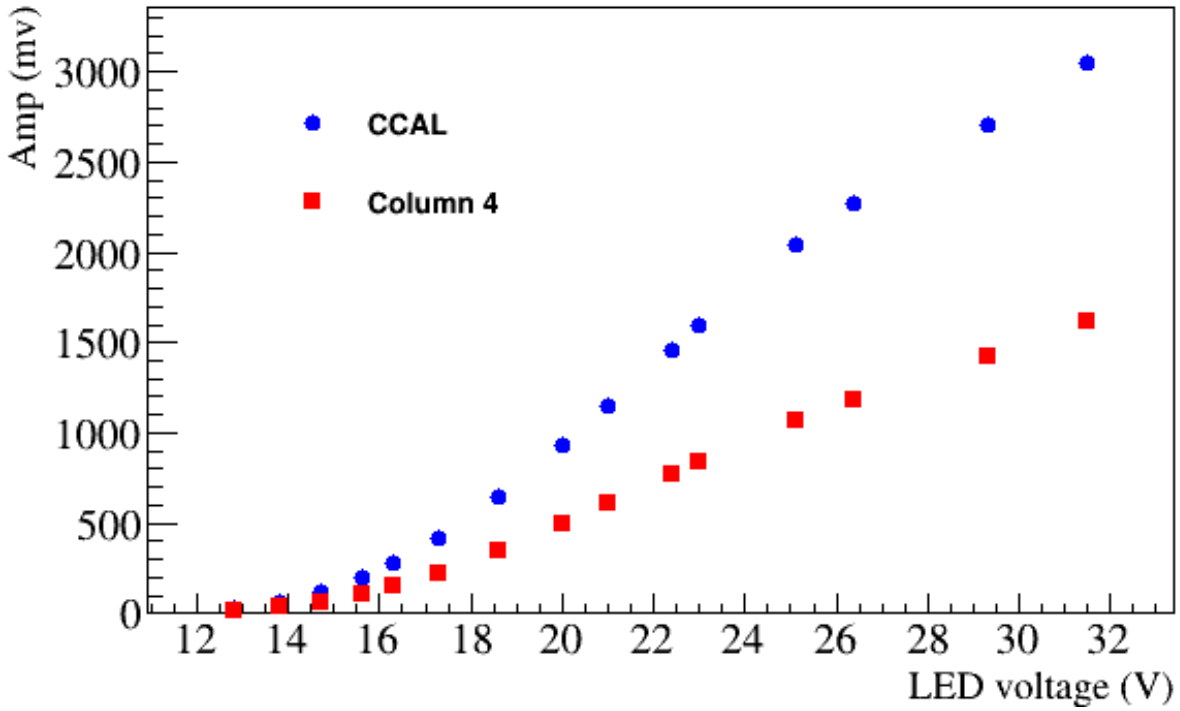
- 1 mA at 1 kV

Checked Dividers (no amplifier) using an LED

- Light source not calibrated. Estimate relative performance

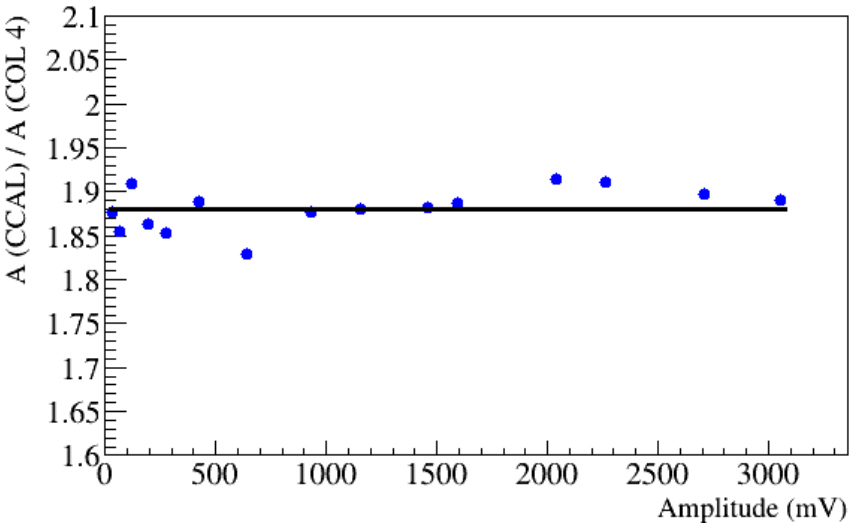
  - Position PMT to the same spot relative to the LED fiber (one divider after another)

  - Compare signal amplitudes for the same LED voltage

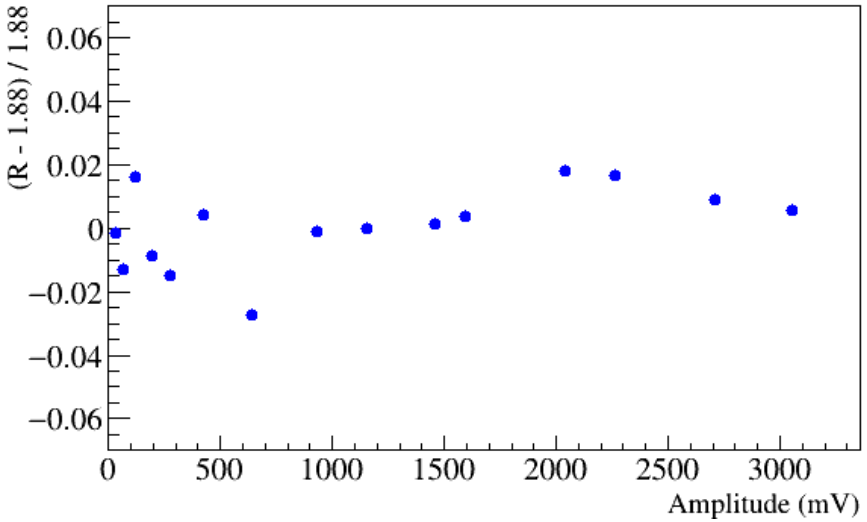


Checked Dividers (no amplifier) using an LED

Ratio of amplitudes



Relative ratio



No visible difference in performance (no trend)

Gain of the modified divider (increased voltage on 1st dynodes) is about 2 times smaller

- expected operation voltage – 1060 V