The VHDL code does the following:

1. Sum ADC samples from two FADC250 boards.
   1. SumN = F1SampleN + F2SampleN
2. Sum Up SumN in sliding window.
   1. SlideSumI = SumFrom0ToWindowWidth (SumN)
   2. WindowWidth is the number of samples in the summation. It is user programmable.
   3. One WindowWidth is one 7-bits user programmable register applied to all FADC pairs..
3. Set a bit when SlideSumI is greater than Threshold.
   1. Threshold is one 16-bit programmable register for all FADC pairs.
4. The 32-bit data format is described in “Some specification on the FADC250 and CTP trigger firmware for Hall D calorimeters. “ by A. Somov

Example for one pair of FADC250 processing:

0+1+2+3+

4+5+6+7

0+1+2+3

0+1+2

0+1

F1SampleN

F2SampleN

SumN

Sample #

0

2

4

6

8

SlideSumI

Threshold

BIT