The VHDL code does the following:

1) Sum ADC samples from two FADC250 boards.
   a) $Sum_N = F1Sample_N + F2Sample_N$
2) Sum Up Sum_N in sliding window.
   a) $SlideSum_I = SumFrom0ToWindowWidth\ (Sum_N)$
   b) WindowWidth is the number of samples in the summation. It is user programmable.
   c) One WindowWidth is one 7-bits user programmable register applied to all FADC pairs..
3) Set a bit when $SlideSum_I$ is greater than Threshold.
   a) Threshold is one 16-bit programmable register for all FADC pairs.
4) The 32-bit data format is described in “Some specification on the FADC250 and CTP trigger firmware for Hall D calorimeters. “ by A. Somov

Example for one pair of FADC250 processing: