12GeV Trigger meeting notes:

9-Sept 2011: C. Cuevas, B. Moffit, S. Kaneta, W. Gu. A. Somov, H. Dong, N. Nganga, E. Jastrzembski

2-Sept 2011: C. Cuevas, B Moffit, B. Raydo; J. Wilson, S. Kaneta, H. Dong, W. Gu. D. Abbott, A. Somov

26-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, B. Raydo; J. Wilson, E. Jastrzembski, S. Kaneta, W. Gu

19-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo; S. Kaneta, W. Gu

12-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo; S. Kaneta, E. Jastrzembski

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0. Trigger/Clock/Sync – TI/TD

9 Sept 2011

→It is time to replace the existing TI boards(older revision) in the EEL109 lab with the latest revision. The 10 new TI boards have been tested and updated to match the latest CODA library. The latest TI boards will be installed in the EEL109 two crate test stand the week of 12-Sept.

→William has the TS schematics and other design files complete and it is a good time to organize a 'review' meeting with the appropriate engineers for circuit design analysis and discussion. William will set up this meeting soon.

2 Sept 2011

→All ten boards are tested and working. It appears that the LGA voltage regulators were repaired.

→Install one pre-production TI (Version 4, Rev2) board in the EEL109 test stand.

→Discussion regarding firmware selection by software. Example, TI 'Master' function or normal TI function. Can firmware be all inclusive and then the modes are selectable? Capability of writing FPGA configuration device via VME exists also.

->Review configuration circuitry/requirements before FINAL order. Minor ECO will be required.

26-Aug-2011

→William reports that the four TI/TD boards that were sent for rework are still at the assembly company.

→We talked about the need to update the TS/Trigger Distribution crate map document to reflect actual TD implementation. Chris has updated the document to reflect the correct VXS pin map. The TD boards are assembled differently than a TI so that the payload mapping matches a standard front end board payload port.

→ There was some discussion about the Trigger Supervisor prototype which can be funded in October. (FY12 funding) More discussion regarding the latest revision of the TI; Will it support legacy DAq systems in Hall A and Hall C? Branch cabling, and other legacy interface connections will need to be reviewed including a few other technical details before the prototype TS is send for order. May be a good idea to set up a meeting with the Hall C and Hall A folks to verify their DAq plans/requirements for the next few years.

19-Aug-2011

William reports that four pre-production boards are still at the assembly company for rework/repair.

TD board has been tested to emulate the Trigger Supervisor crate functions. TS->SD->TD->TI

These functions appear to work correctly. William will continue testing all functions of the TI in Trigger Distribution mode... The firmware will be different for TI and TD, so there will have to be a library 'driver' for these different boards.

12-Aug-2011
Four boards sent for rework should be received next week. Acceptance testing is progressing well. There appears to be an issue with setting up the Trig_2 signal in the non-TS crate and William is investigating the problem. The Trig_2 signal will be used to initiate the "Playback" mode and the Trig_2 will need to be issued synchronously to each crate so that the playback data is aligned properly.

1. *SUB-SYSTEM PROCESSOR (SSP)*

9 Sept 2011
No report. SSP is presently being used in the two crate test station and performs well.

26-Aug-2011
Same notes as last week.

19 Aug 2011
Very brief discussion on the recent application plans for the SSP. The CLAS12 SVT group is planning to use the SSP as the front end readout interface to the FSSR ASIC silicon readout chip. Preparing an order for a quantity of ten (10) boards by January 2012 is realistic, and there are only minor changes to the fabrication files that need to be verified.

12 Aug 2011
Final ECO can be applied and the specification started to prepare an order for the SSP required for Hall D. We have delayed the production order, but preparing the production order specification can begin now. So far, the prototype SSP has functioned flawlessly, and has been ahead of schedule.

2. *CUSTOMERS*

9 Sept 2011
→Delivery of FADC250V2 boards to the following groups:
Injector group: 2 modules(A. Camsonne)
Hall D: 1 modules (A. Somov)
Hall B: 1 modules (S. Boyarinov)

→Need to consider the proposed setups for the beam tests coming up in Oct/Nov. How do these setups need to be configured. SD? Front panel clocks/synch/trigger? CTP?

26-Aug-2011
→There have been a few emails regarding the distribution of the latest FADC250-v2 boards and we are in agreement to release boards to the Injector group and Alex on 6-Sept-2011. Need at least thirty (30) boards to demonstrate the two crate performance operation using the playback feature.

19 Aug 2011
Week of 5-Sept a few boards will be distributed to a few groups.
EEL-109 lab will retain at least 32 boards!!

12 Aug 2011
No change from last week, but several of the FADC250-V2 boards that did not pass acceptance testing have been repaired. The remaining boards that did not pass acceptance testing will

need detailed troubleshooting. Signal data from all accepted boards has been collected and analysis continues.

3. "B" Switch - Signal Distribution Module (SD)

9 Sept 2011

→All the boards have been tested for hardware functionality. All boards have front panels, and the Tyco Gigabit backplane connectors have been installed.

→ Nick continues to test SNR using a single FADC250. Some noise floor issues still remain to be solved to be able to present data. May be able to extend raw data window to allow for more points in a sample window, which would allow an FFT of many more points (lower frequency analysis)

26-Aug-2011

→Nick reports that we are waiting on the Gigabit backplane (Tyco) connectors. Jeff has ordered these parts and they should be in stock.

→One Rev2 board is fully populated. Acceptance testing is almost complete, and includes tests with the TI and TD boards. The only ECO is a minor change for the ECL output section.

→Nick has performed jitter analysis using different signal frequency inputs and showed the initial results with and without the jitter attenuation circuit enabled. Full SNR plots to show affects of clock jitter/distribution are a work in progress and plans for IEEE-NSS 2011 in Madrid, Espana are becoming reality.

19 Aug 2011

Nick reports that all six pre-production SD boards have been received and pass the visual inspection step. Only two boards have been powered and we will need to order Tyco connectors for these switch cards.

One of the SD boards was tested as the clock distribution unit in conjunction with the TriggerDistribution board.(William). So far no show stoppers and William was able to complete several tests using a TI configured as a full Trigger Distribution board.(8 Fiber Transceivers)

Nick reports that the acceptance test firmware is complete and he has started using the code to test the pre-production boards. We will have to wait for the Tyco Gigabit connectors to fully populate all six new SD boards.

12-Aug-2011

→Partial delivery of the six SD boards is on schedule for the week of 15-August. One FPGA needed to be purchased because of a broken pin issue, but all boards should be here by the end of next week.

→Nick is nearly finished with the acceptance test firmware which will be installed with the standard operating firmware. Acceptance testing of all six pre-production SD boards will begin as soon as the boards arrive. At some point the Rev-1 boards in the existing EEL109 test stand should be replaced and tested thoroughly with a full crate of FADC250-V2 boards and the latest TI boards.

4. System Diagrams/Fiber Optics

No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

5. Two Crate DAq test configuration

9-Sept 2011

→The two crate testing has been slowed down this past week because 16 FADC250 are needed to test/verify the CTP firmware. Bryan reports that the driver library has been finalized for the version of FADC250 boards that have been distributed.

→Ed reports that the 2eSST readout mode testing with the latest software shows a few issues. Will need to be investigated and any firmware changes can be downloaded to modules in situ.

→Bryan showed a few plots of data from the "Playback" mode and there are a few issues/questions because the data results show some sort of offset that should not be present when using the "Playback" setup data. Hai will have to investigate the "Playback" mode to see where the problem may occur.

26-Aug-2011

Sixteen FADC250 boards are being used by Hai to verify the CTP code. 15/16 FADC250 are running at 2.5Gb/s with two full duplex lanes.

→2eSST mode has been simulated, verified and implemented into the FADC250 by Ed.

→Latest firmware that includes the 2eSST will be loaded into all FADC250 by next week.

→Will set up playback mode, 2eSST test soon to verify all connections, functions and high data transfer rate. The readout data will need to be pre-scaled, otherwise we will not be able run for a long time at the required trigger rate (200 KHz) because the disk will be full.

19 Aug 2011

→Bryan reports that "Playback mode" is working. No firmware changes needed to existing implementation.

Playback "Trig_2" rate is low. (200Hz)
All channels, all boards have pulse data loaded for playback mode. (100% occupancy)
Data transfer rate??
CTP and SSP are used in the playback mode.

→2eSST firmware has been simulated(Ed) and will be loaded into FADC250 boards soon! The 2eSST readout method will be required to achieve the fully specified trigger rate and readout capability of each front end crate.

12-Aug-2011

→Steady progress with the two crate testing and a total of 27 FADC250-V2 boards are in use. 16 boards in one crate and 11 in another.

→Configuration and test parameters as follows:

- **160KHz trigger rate!!**
- 16 analog pulses distributed to 4 boards. (Low occupancy; 3%)
- Pulse integrating mode
- 50MB/s data transfer rate; 2eVME transfers with token passing
- 40 events/block
- Final trigger created from two CTP, with the SSP combining the two crate trigger data

→"Playback" mode is in the process of implementation and a few small issues remain before testing all channels/boards in this method.

- Amount of readout data will increase when playback mode is used
- Disk space will be a limitation for long test operation
- 2eSST mode will definitely be needed to reach MAX readout rates

→Bryan showed plots of integrated pulse values for several FADC250-V2 boards

- Channel 14 on several boards show unexplained problem
- "Charge" value for active channels appears to have a low RMS value
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➔ The following is a copy of the test goal list created several months ago:

- **<u>Goals of the integration testing</u>:**
- **-Verify clock distribution through TID->SD and measure jitter to front end boards**
- **-Verify trigger rate and readout rate for a variety of occupancy levels.**
- **-Verity token passing scheme**
- **-Verify CTP operation with sixteen FADC250 @2.5Gbps**
- **-Test playback mode feature on two crates and verify operation with SSP.**
- **-Measure and record overall trigger latency. (Could include SSP)**
- **-Verify full 2eSST readout from payload modules**
- **-Verify TI-D features and use one TI-D in TS 'mode'**
- **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**

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<u>3 June 2011</u>

→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

<u>22 April 2011</u>

The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→<u>Goals of the integration testing</u>:
-Verify clock distribution through TID->SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

<u>16 July 2010 (Keep this because it needs to be implemented and tested at some point)</u>
<u>See older note dates for the list.</u>

6. *Crate Trigger Processor (CTP)*

<u>9-Sept-2011</u>

→Hai has a breakthrough with sixteen FADC250V2 boards passing trigger data to the CTP in one crate. Only two errors in 6 hours with sixteen FADC250V2 boards!!!! A new JLAB record! The errors are in the final sum value, and the errors do not crash the system. So far these tests only include the FADC250V2 and CTP board.
→Move one of the CTP to the EEL109 today, and setup/test the 2nd CTP early next week.
The EEL109 test station will have one CTP with a V5LX110 and one CTP with a V5FX70T.
→Plan to populate both crates in the EEL109 lab by end of next week.

2-Sept-2011
-->15 FADC250V2 boards with the CTP are under test in the DAQ lab.
→This test will need to be re-tested with ALL FADC250V2 AND CTP clocked by a single source.
→CTP#4 with 'FX70T are being tested now with the 15 FADC250V2
→By end of next week 9-Sept we will have two CTP in the EEL109 test station!

26-Aug-2011
→See test stand notes
Hai has been successful with CTP firmware that allows for synchronization and high speed data assembly from all the payload slots in the crate. There are a few problems, but he should be able to release the CTP soon so that the trigger from each CTP is a sum function from all the FADC250-v2 boards within a crate.
→Hai created a "Playback Mode" test document

19-Aug-2011
→Hai is using 10 boards with a single CTP, new JLAB record!
Payload slot 6 does not seem to work properly. PPT 1-10 with payload 6 causing problems.
Full crate test by the end of next week 26-Aug to verify CTP Gigabit serial functions!
Once these are tested in the DAq lab, we can move them to the EEL109 test stand.

7. GTP and Global Crate Developments

9-Sept-2011
→Ethernet and DDR2 memory testing is a work in progress and is going well.
→Nios core etc is on a trial basis. Will cost some money for a license.
→5Gb/s for two lanes from one SSP board has been successfully tested. Proves the Xilinx to Altera marriage will work. (Aurora protocol PRSB31 testing)
→Densi-shield cable testing may be next goal
→Paper/Poster work is in progress for ICALEPS-2011

2-Sept-2011
→Configuration bits loaded to the device and are stored on the board.
→MGT transceivers have been tested on slot 13 @5Gb/s PRBS-31 signal pattern; SSP was used so Xilinx to Altera marriage produces no known problems.
➔ DC power test matches expectations, no heat sink needed at this time. May need to be considered for final board.
➔ Memory testing DDR2, and other hardware testing is progressing nicely
➔ Densishield testing, Ethernet testing,

26-Aug-2011
-->Scott reports that the required clocks are running on the GTP board.
→Repair to LGA voltage regulators worked fine
→Test acceptance code is moving forward
→2.5Gb/s and 5Gb/s on two lanes have been loopback tested for one payload port. This test used PRBS with the Altera toolkit.
→Configuration work on Flash storage has started.
→Important test with SSP (Xilinx FX70 @2.5Gb/s) to the GTP Altera device can be started on Monday 29-Aug-2011.

19 Aug -2011
→Scott reports that the fully populated GTP board has been received from the rework company and the power supply circuits function properly.
→DC measurements have been completed, and FPGA JTAG scan works for the two devices.

→Acceptance test firmware is still under development, but initial code is being used to verify board functionality.

12 Aug-2011

DC power check has been measured and documented for the partial assembly board.
Fully assembled board will have the regulator rework wire added to the LGA circuitry.
Conference paper and poster framework started.
Full board back next week, ready for power test!!
Firmware and acceptance test code will become full time activities once the GTP board has been received and power tested.

ACTION ITEMS: **Next meeting -Friday 16 Sept @ 10AM in F226**