Pipelined Electronics for the Next Generation of DAQ at JLab

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JLab S&T Review

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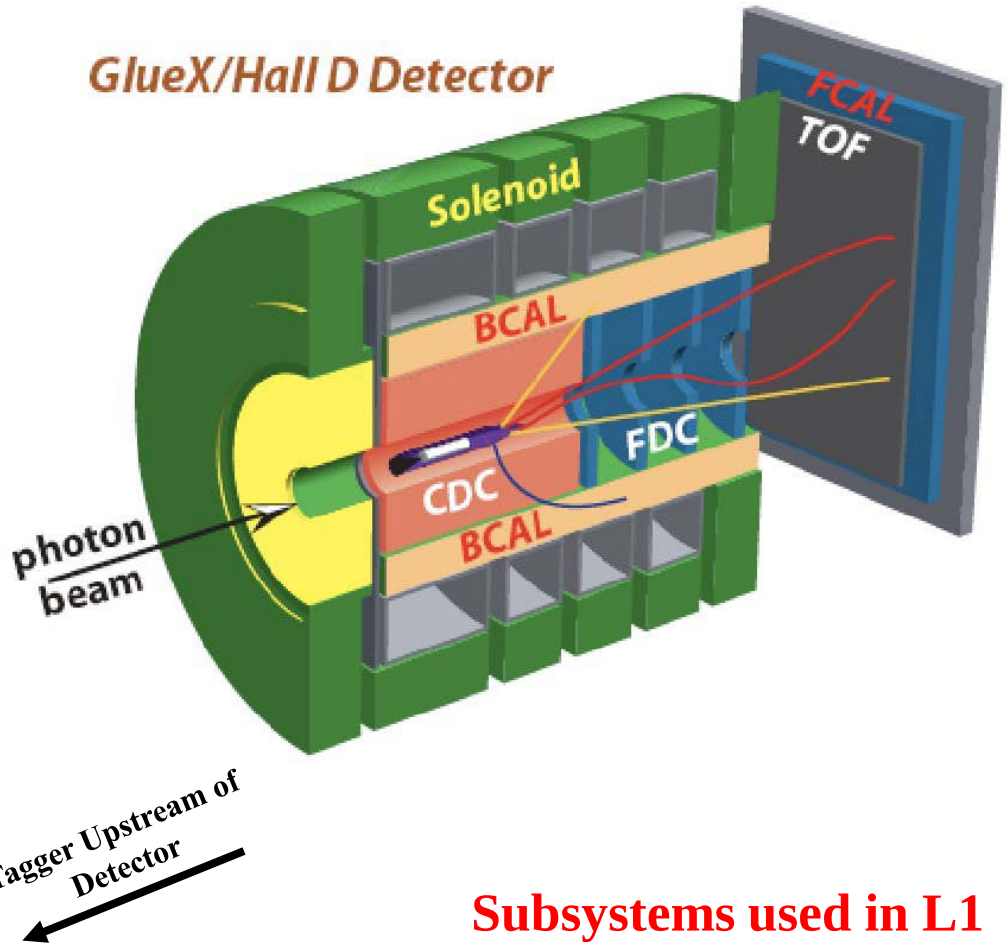
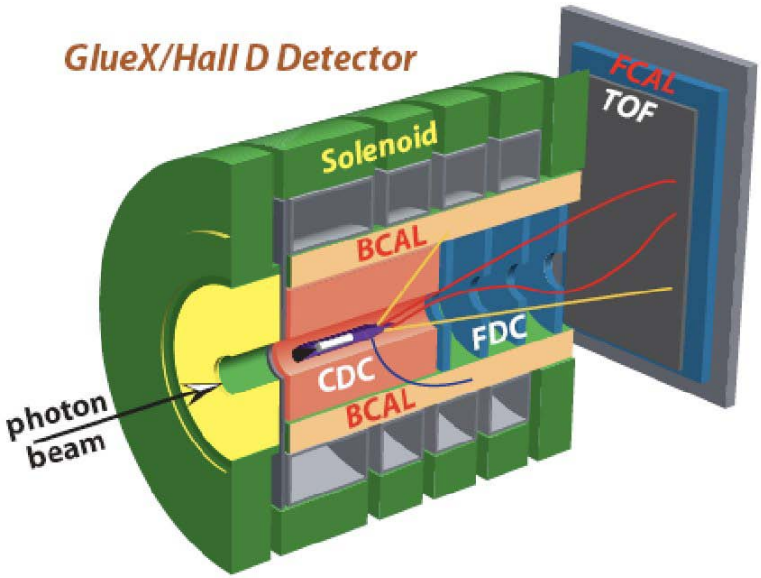
New Hall D – Detector

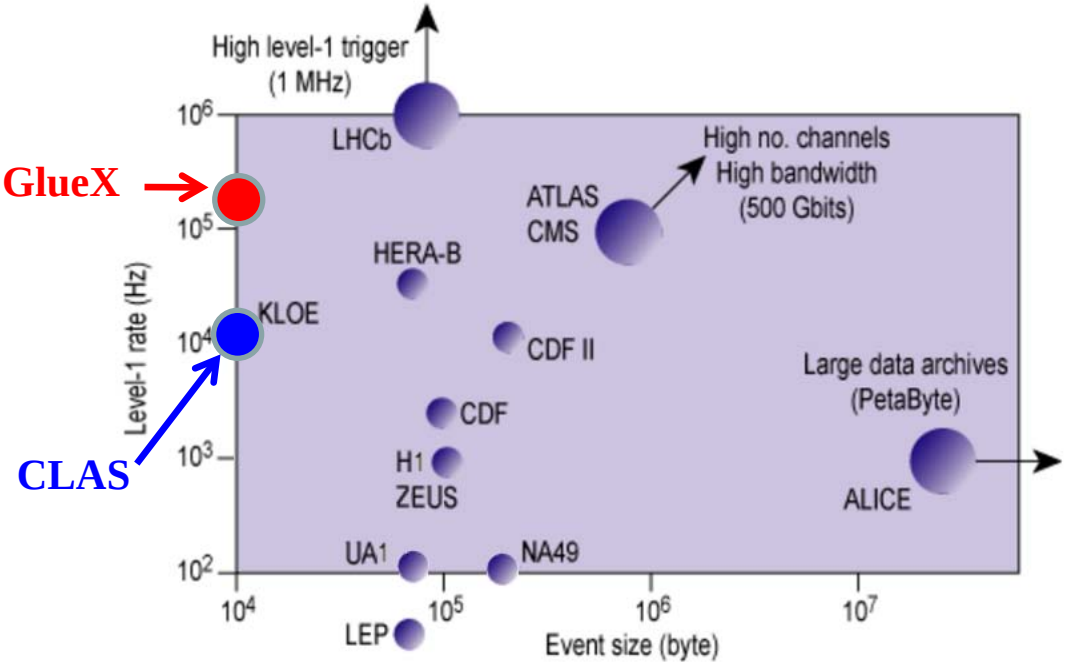


- Detector Channels: ~22,000
- Luminosity: $10^8\gamma$/s
- L1 Acceptance Rate <200kHz
- Event Size: ~15kbytes
- Detector Subsystems:
  - Central Drift Chamber
  - Forward Drift Chamber
  - Pair Spectrometer
  - Tagger
  - Start Counter (ST)
  - Time of Flight (TOF)
  - Barrel Calorimeter (BCAL)
  - Forward Calorimeter (FCAL)

Subsystems used in L1

Comparison to CLAS in Hall B



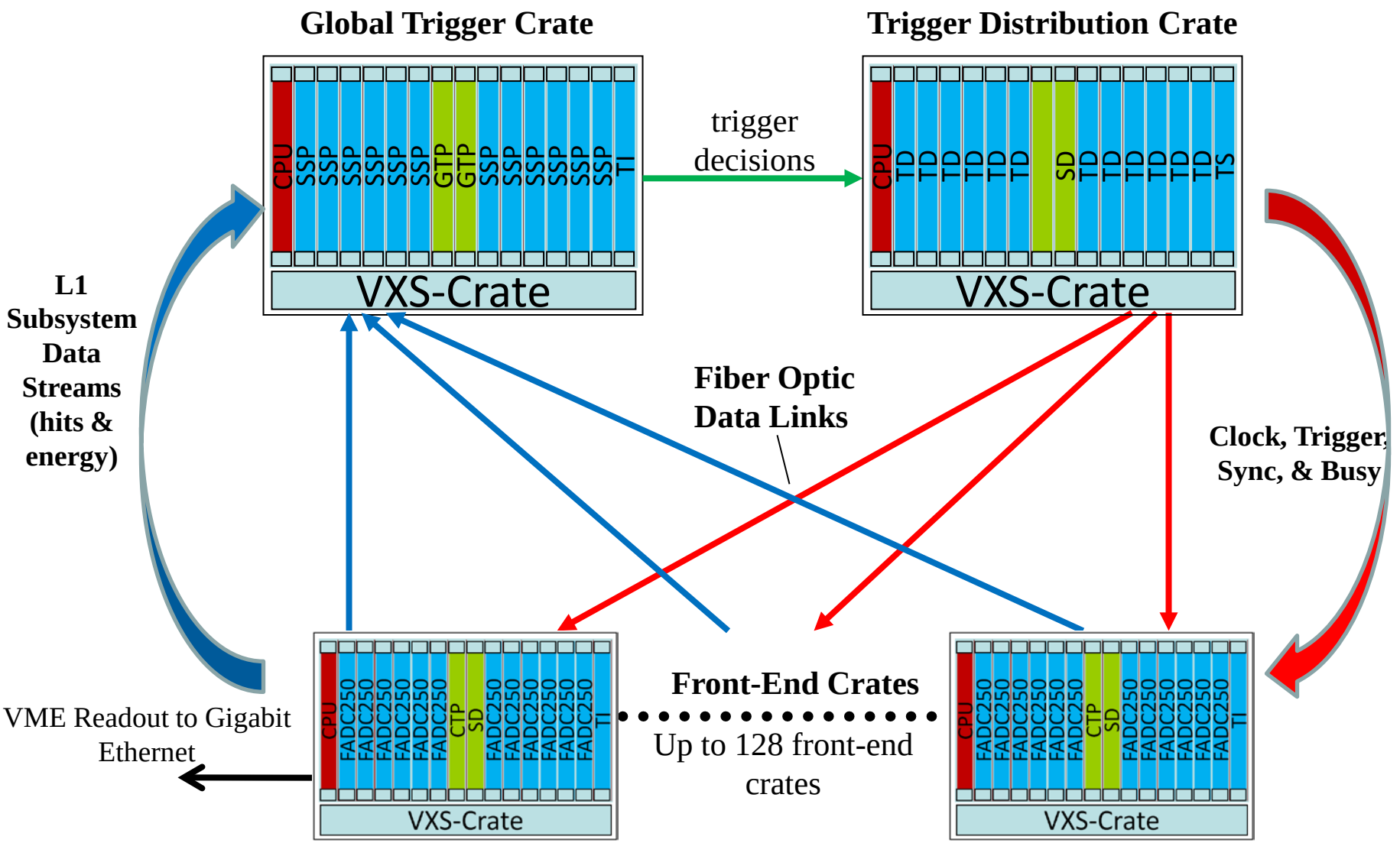


	Hall D-GlueX	Hall B-CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	**200kHz**	**10kHz**
L1 Data:	**3GB/s**	**60MB/s**
To Disk:	**L3, 20kHz, 300MB/s**	**L2, 10kHz, 60MB/s**

Main Trigger Design Requirements

- 200kHz average L1 Trigger Rate, Dead-timeless, Pipelined, 2ns bunch crossing (CW Beam)
- L1 trigger supporting streaming subsystem hit patterns and energy summing with low threshold suppression
- Scalable trigger distribution scheme (GlueX: ~30 L1 crates, ~50 total readout crates)
- Low cost front-end & trigger electronics solution
- Reconfigurable firmware – CLAS12 (Hall B) will use different programmable features than Hall D

Level 1 & Trigger Distribution



Crate Level – Signal Distribution

- VXS Based, 20 Slot Redundant Star Backplane

- VME64x backplane w/VXS (VITA 41 Standard) provides standard with high speed serial extension (new J0 connector)

- 18 Payload slots w/VME64x, 2 Switch slots

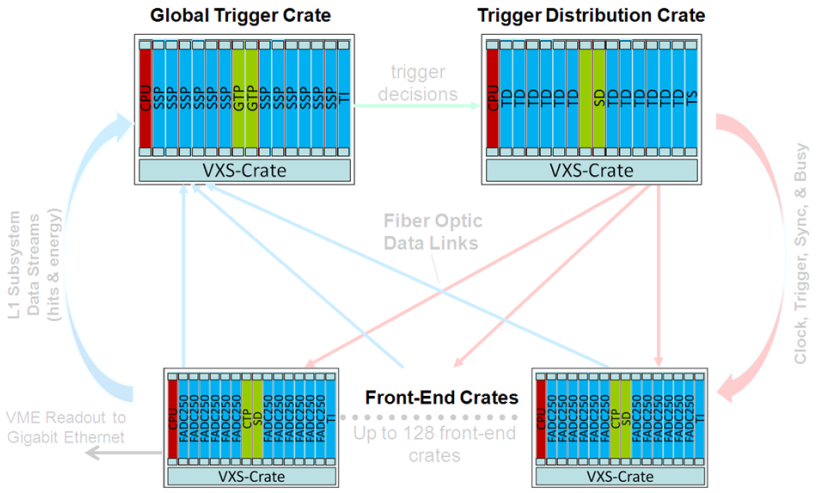
- Each payload slot has 8 high speed capable links (10Gbps each) to both switch slots

Crate Level Use:

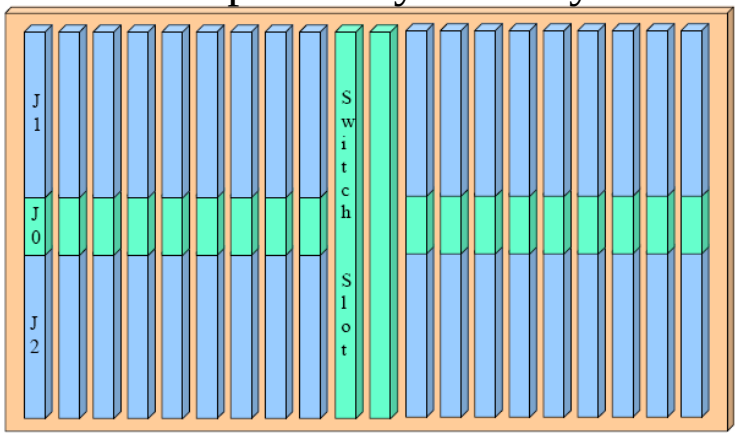
- VME64x used for event readout

- VXS: Low jitter clock & trigger distribution

- VXS: Gigabit serial transmission for L1 data streams to switch slot for processing



VXS Backplane Physical Layout:



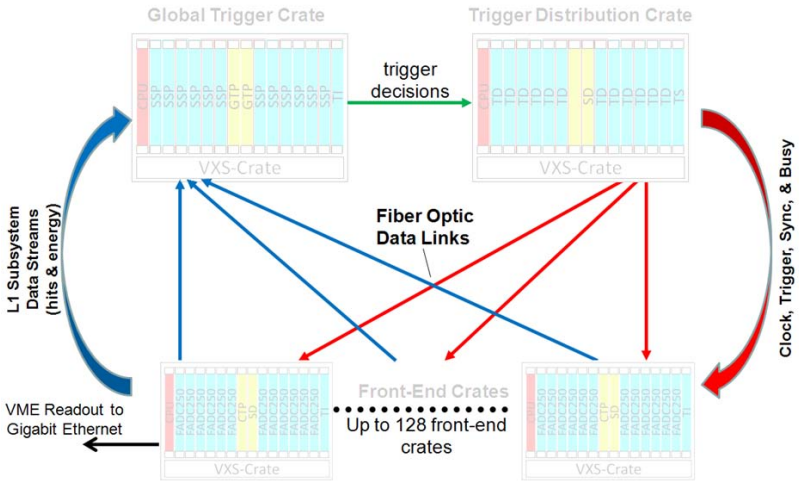
VXS (VITA 41 standard)
VME64x + high speed
serial fabric on J0

Global Level – Signal Distribution

• Four independent channel fiber optic transceiver connects global crates to front-end crates

• Transmits up to 150m @ 3.125Gbps per channel (12.5Gbps total)

• Uses MTP ribbon fiber optics (fewer connectors & fiber bundles)



Trigger Distribution -> Front-End Crate:

Delivers clock & fixed latency, synchronous triggers to all crates.

Front-End -> Global Trigger Crate:

Provides 10Gbps L1 data streams use to create L1 trigger.

Parallel Fiber Optic Transceiver (HFBR-7394):

Capturing the Pulses…

CLAS TOF has >150,000ft delay line!

Expensive, bulky delay cable dispersive & attenuates

Non-pipelined electronics guarantee dead-time (conversion time)

Existing Systems:

Delay line

Gate

detector signal

Splitter

QDC

Discriminator

to primitive trigger logic

TDC

Very limited channel resolution used in trigger

multiple modules for time & energy

New System:

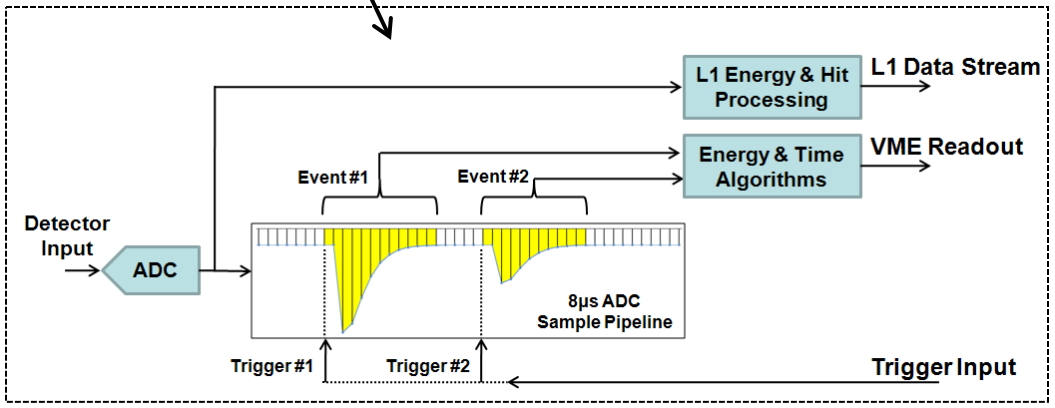
(for timing >500ps)

detector signal

FADC250

to smart trigger logic

Time, energy, trigger output in 1 module

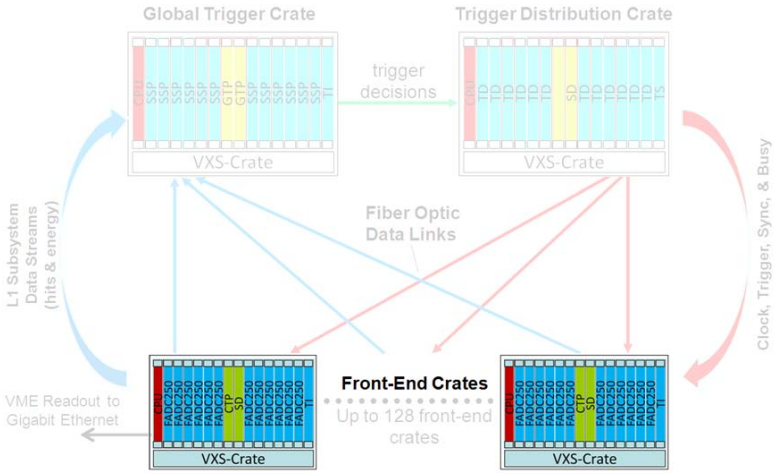


- **Pipelined sampling, readout, & trigger -> no dead-time**
- **Digitization retains original signal integrity**
- **Long pipeline allow more time for complex triggers**

Front-End Electronics
Flash ADC 250Msps

- 16 Channel 12bit, 250Msps Flash ADC
- 8µs raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- VXS P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)

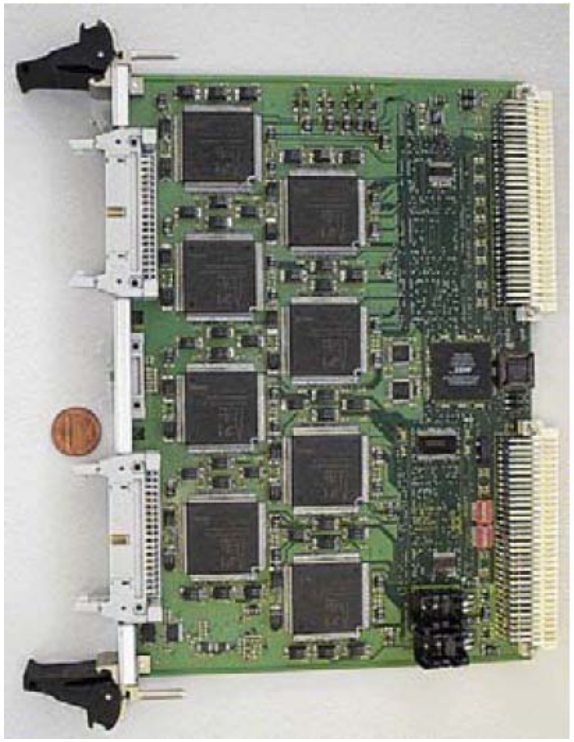
- Used in existing 6GeV program:
  - Hall A BigBite
  - Upgraded Hall A Moller Polarimeter



JLab-FADC250:

Front-End Electronics: F1TDC

JLab-F1TDC



Sets maximum trigger latency

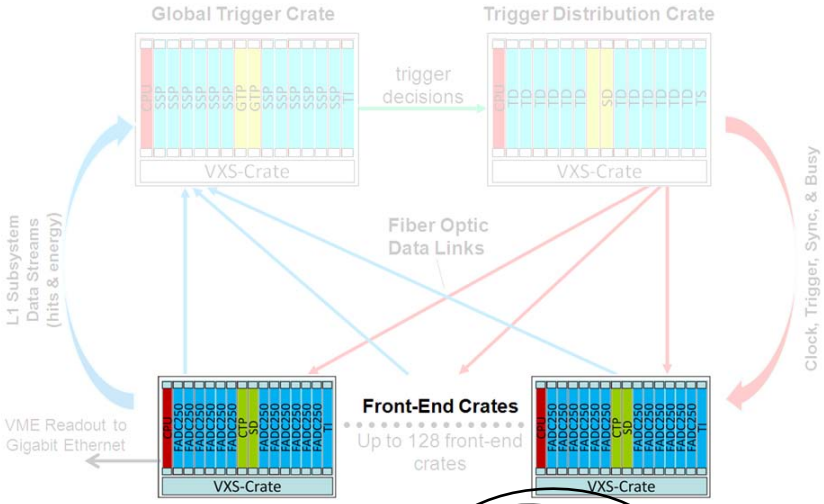
- **High resolution - 60ps/32 channel**
- **Normal resolution – 120ps/64 channel**
- **3.7μs sample pipeline**
- **Used in all subsystems except CDC & FCAL**
- **Not used in L1 trigger**

Front-end Crates: Level 1 Trigger

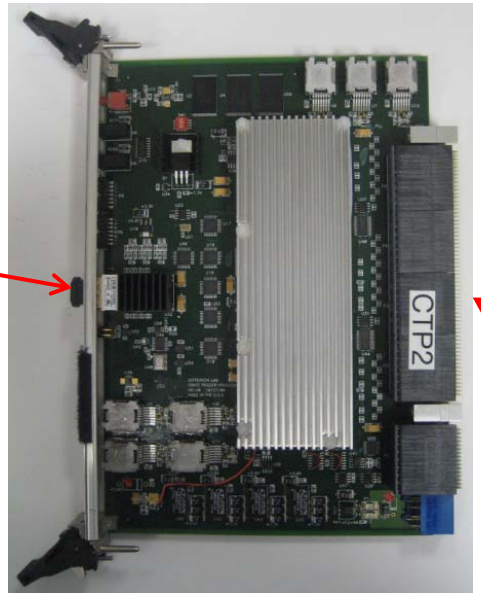
- Each FADC250 stream L1 board energy sum/hit to Crate Trigger Processor (CTP) residing in VXS switch slot A

- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)

- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



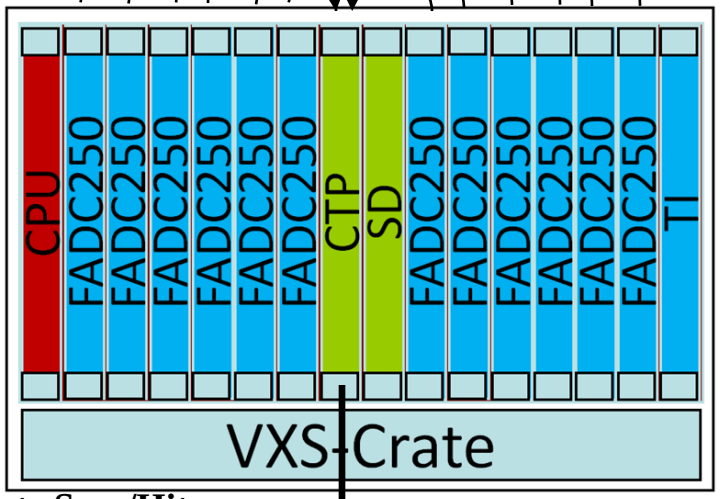
CTP Prototype:



Fiber Optics Transceiver

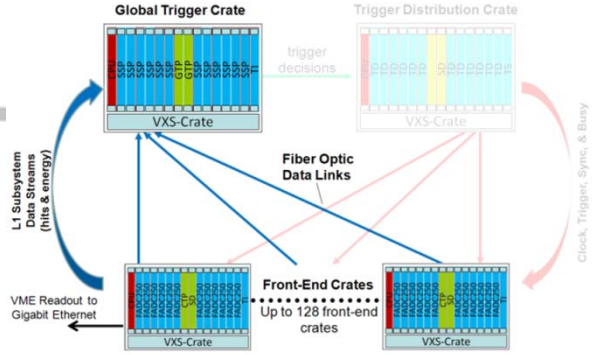
VXS Switch Connector

Board Energy/Hits 5Gbps to CTP



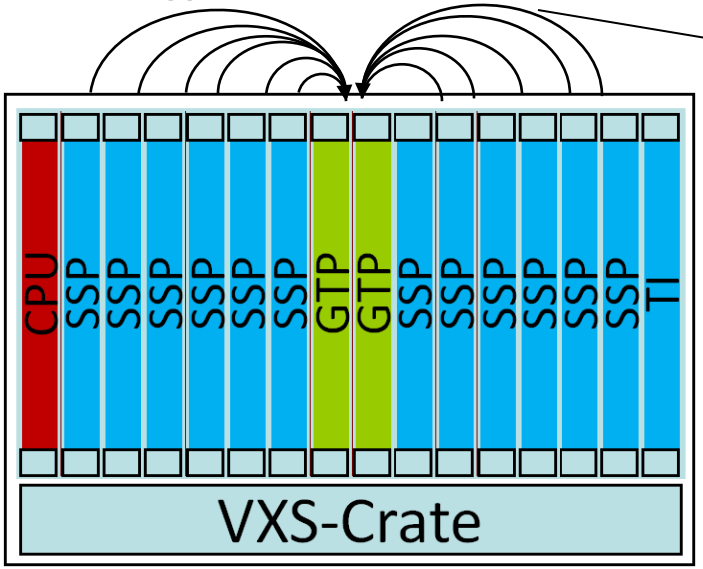
Crate Sum/Hits 10Gbps Fiber to Global Trigger Crate

Subsystem Processor: L1



Global Trigger Crate:

Subsystem Energy Sum & Hit Pattern (10Gbps to GTP)

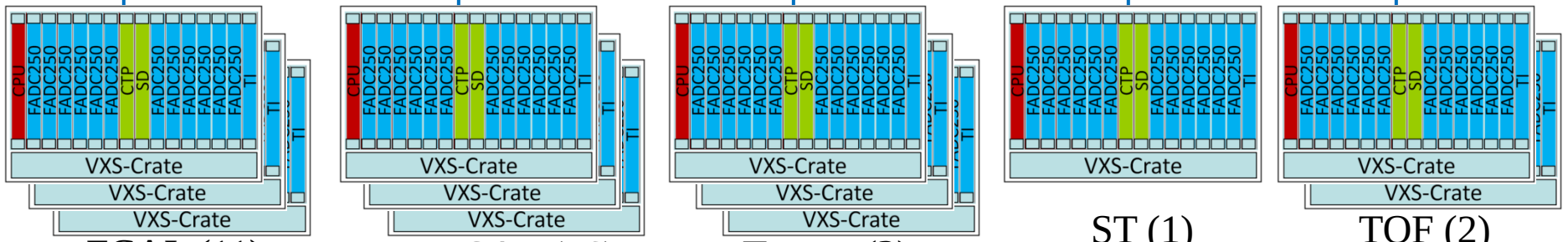


- Sub-System-Processor (SSP) consolidates multiple crate subsystems & report final subsystem quantity to Global-Trigger-Processor (GTP)
- 32bit quantity every 4ns

Hit Pattern

10Gbps fiber optics

Energy



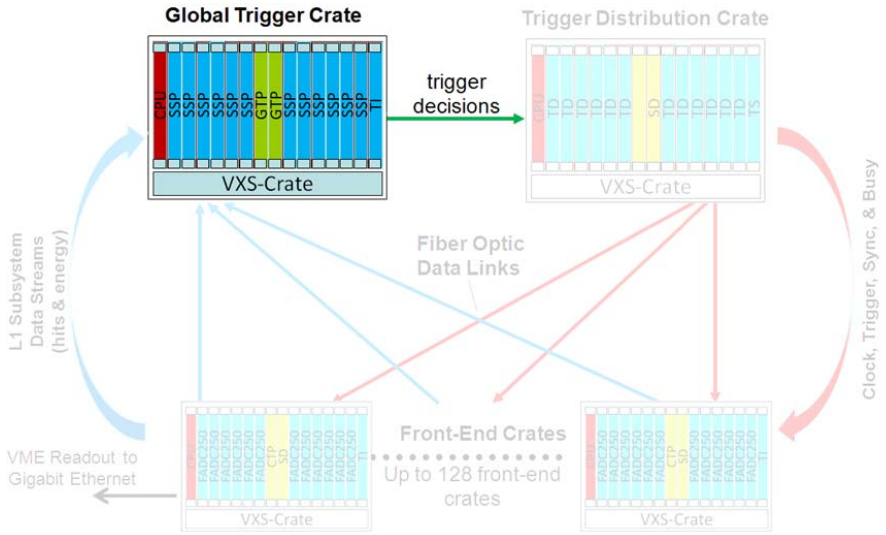
FCAL (11) BCAL (16) Tagger (3) ST (1) TOF (2)

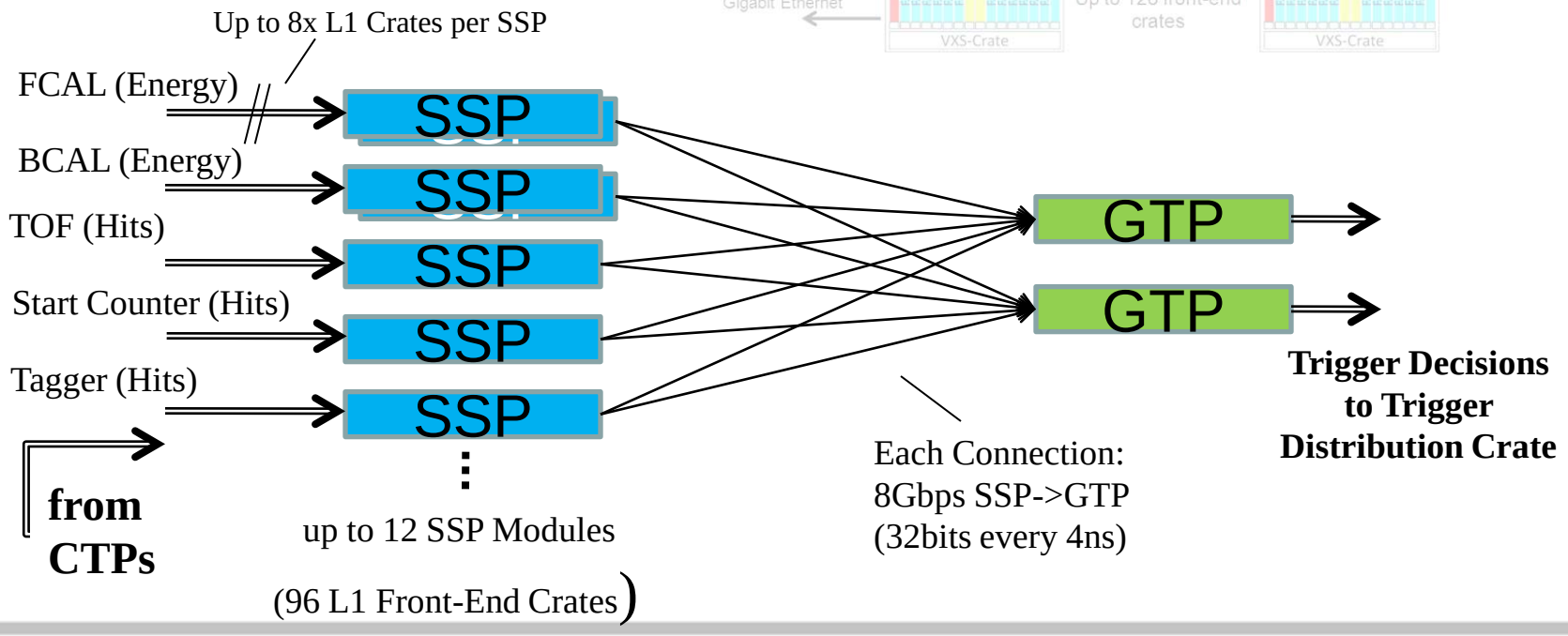
L1 Subsystems (# Crates)

Global Trigger Processor: L1

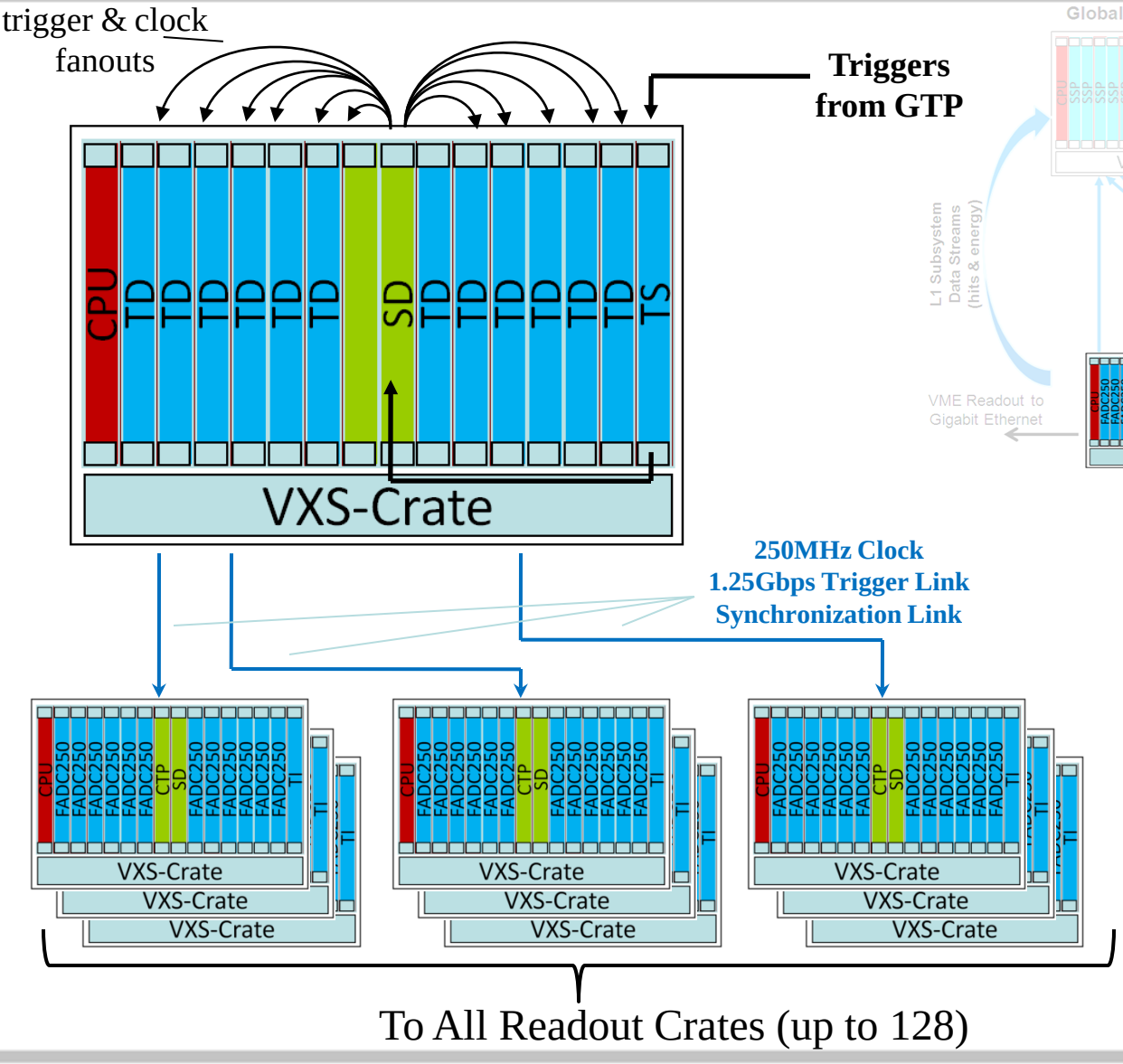
- Global Trigger Processor (GTP) receives all subsystem L1 data streams

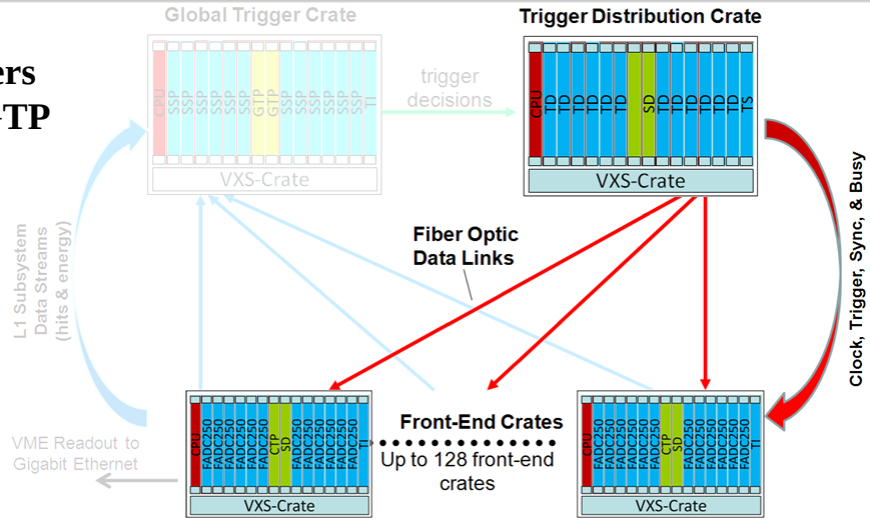
- Trigger decisions made in GTP and distributed to all crates at the Trigger Distribution Crate





Trigger Distribution

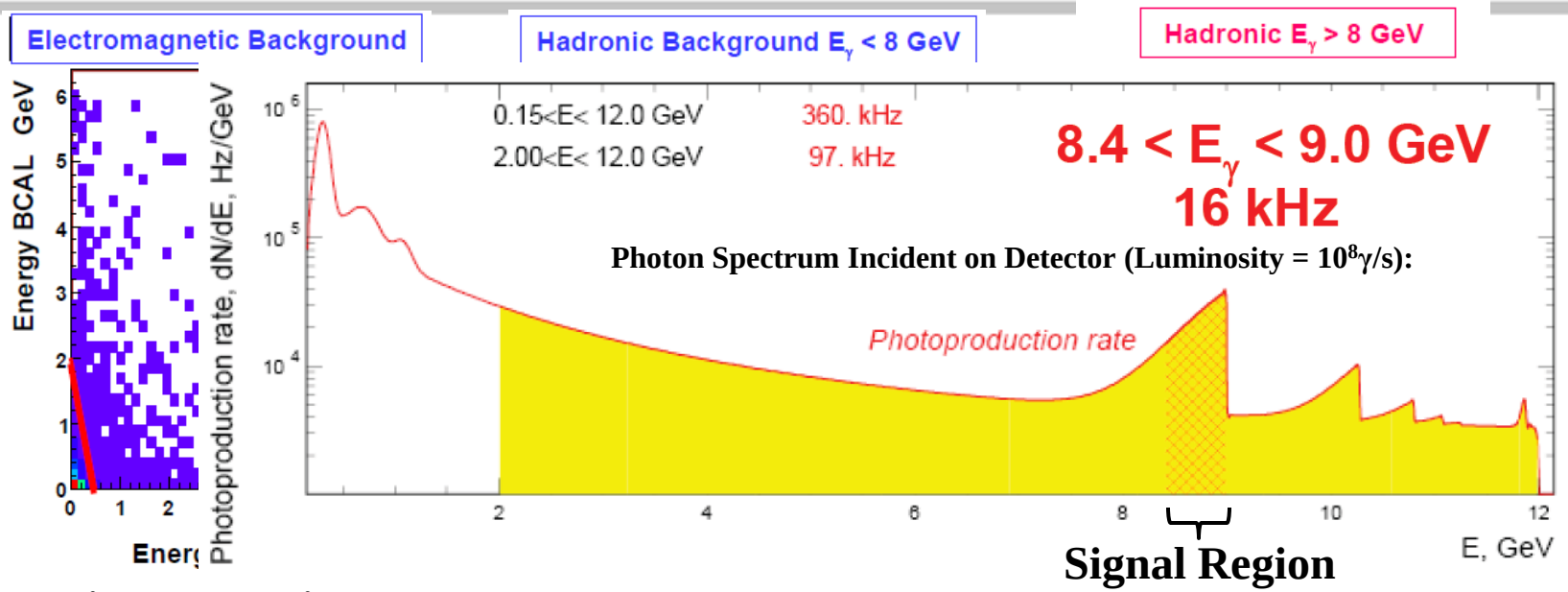




- Trigger Supervisor (TS) distributes clock & trigger to Trigger Distribution (TD)

- Each TD distributes synchronous, fixed latency clock & trigger to 8 crates

Example L1 Trigger (GlueX)



L1 Trigger Requirements:

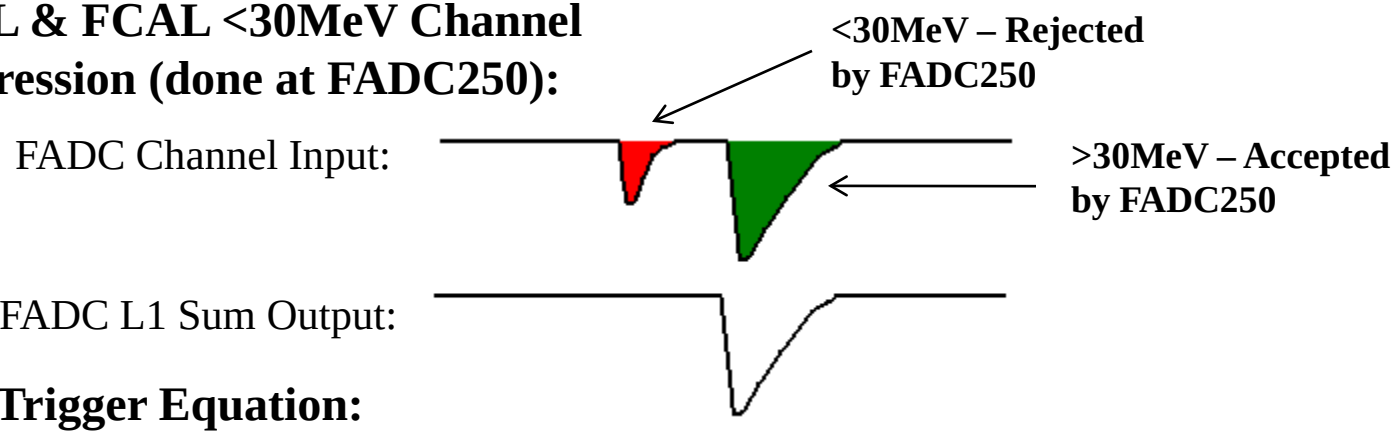
- Reduce 360kHz hadronic & 200MHz electromagnetic interaction to <200kHz L1 trigger rate
- High acceptance in signal region (8.4-9.0GeV)

L1 Trigger:

- Process in all 100ns time windows (4ns stepping)
- Start Counter Hits > 0
- L1 Energy sum suppresses BCAL & FCAL pulses <30MeV
- $BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$

Example L1 Trigger cont…

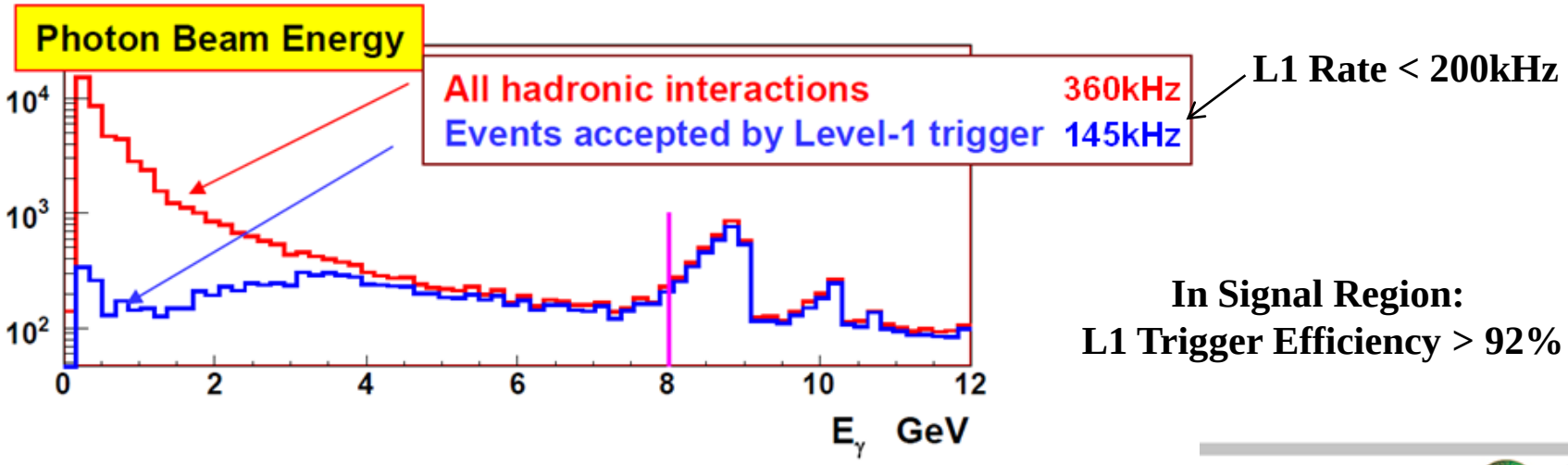
BCAL & FCAL <30MeV Channel Suppression (done at FADC250):



GTP Trigger Equation:

$$\sum_{t}^{t+100ns} ST_{hits} > 0 \;\&\&\; \sum_{t}^{t+100ns} BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$$

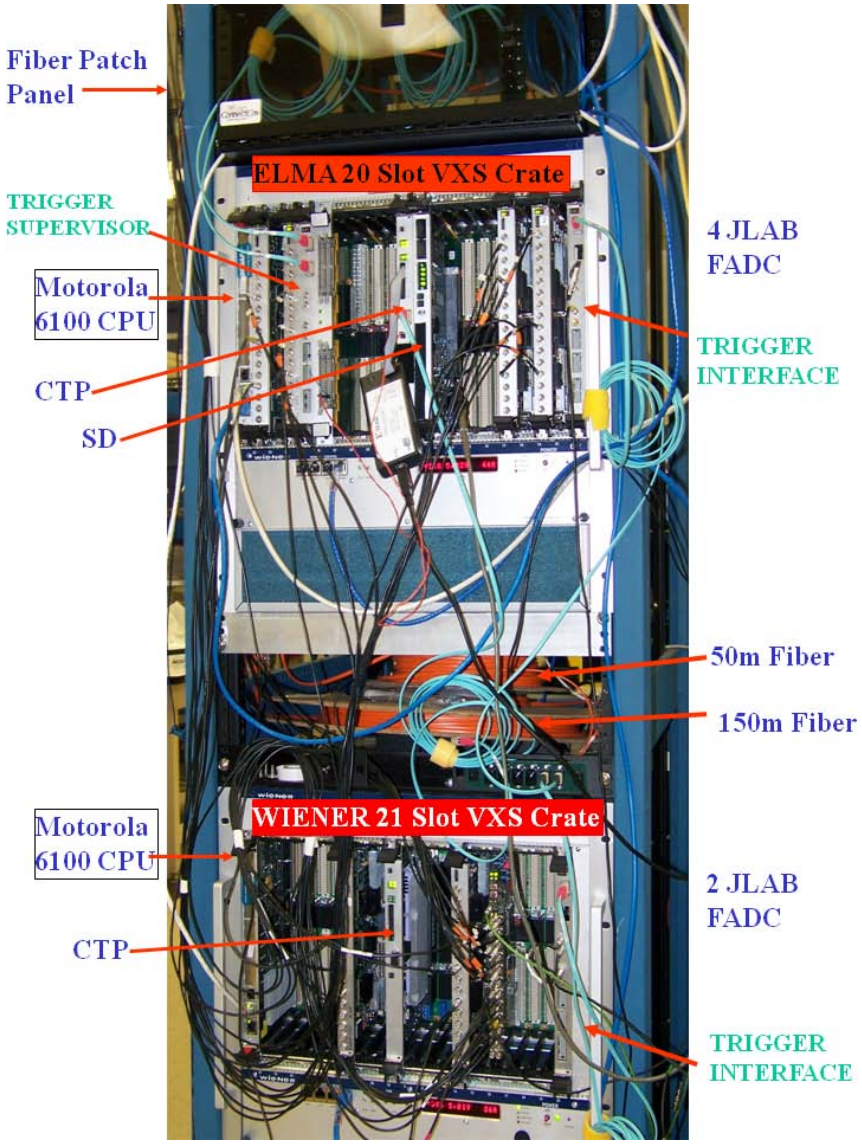
Resulting L1 Acceptance Spectrum:

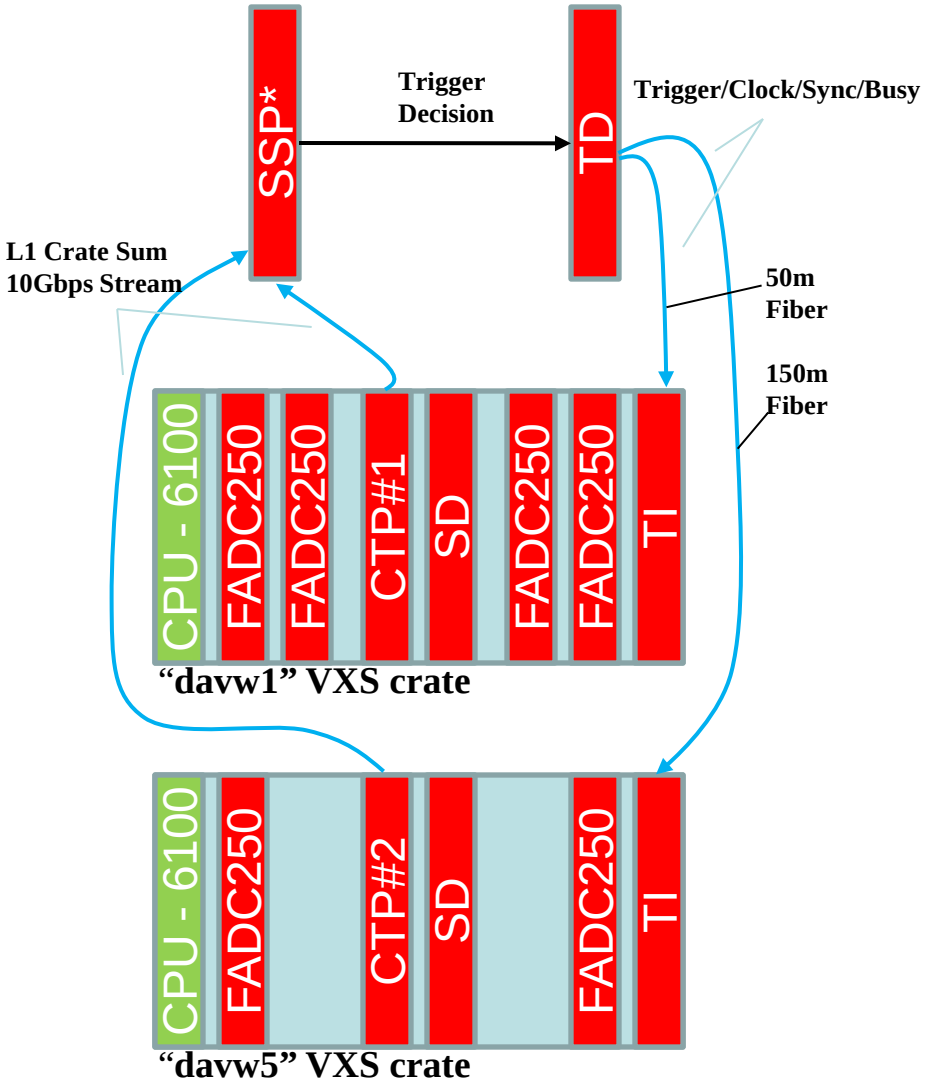


L1 Rate < 200kHz

In Signal Region:
L1 Trigger Efficiency > 92%

2 Fully Prototyped Front-End Crates

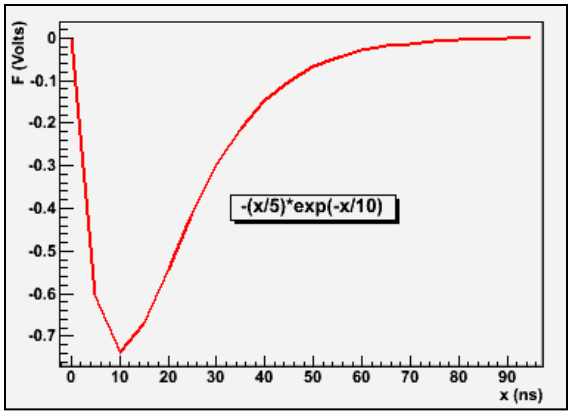




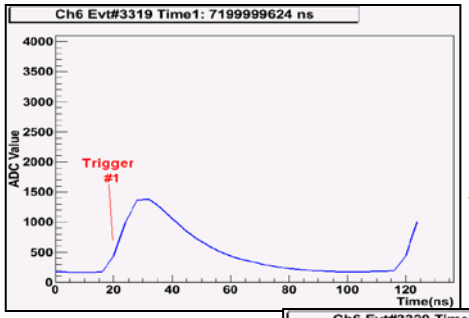
*SSP function embedded inside 2nd CTP

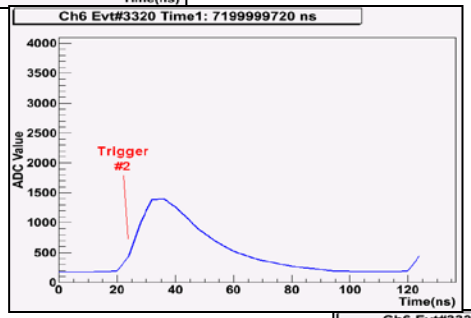
2 Crate Energy Sum Testing

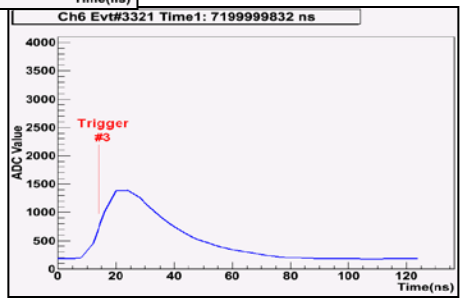
Input Signal(to 16 FADC250 Channels):



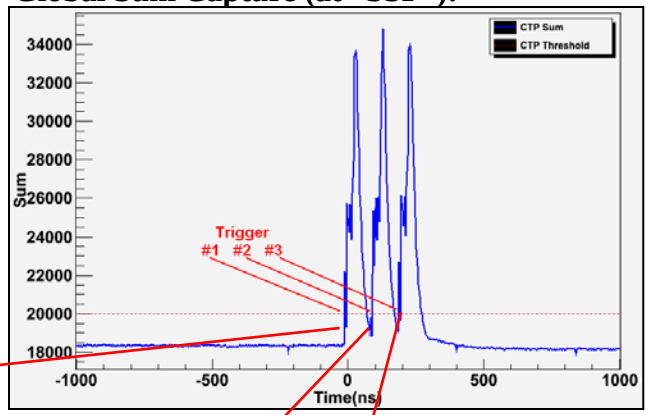
Raw Mode Triggered Data (single channel shown only):







Global Sum Capture (at "SSP"):



- **Threshold applied to global sum (80 digitized channels) produces 3 triggers.**
- **Raw channel samples extracted from pipeline shown for 1 channel.**
- **Runs at 250kHz in charge mode**
- **Latency: 2.3µs(measured) + 660ns(GTP estimate) < 3µs**

Conclusion

Overall design in great shape:

- Trigger distribution scheme successfully prototyped
- Much of L1 has been simulated, prototyped, and works
- L1 timing: <3.7μs latency can easily be achieved
- Modules are reconfigurable, which can adapt to future needs

Acknowledgements

GlueX Collaboration and…

Fast Electronics Group

Fernando Barbosa	Analog, PCB Design, Specifications
Chris Cuevas	Group Leader, Specifications
Hai Dong	FPGA, PCB Design, Specifications
Abhishek Gupta	PCB Design
Benjamin Raydo	PCB Design, System Testing, Specifications
Mark Taylor	CAD Engineer
Jeff Wilson	CAD Engineer

Data Acquisition Group

Dave Abbott	VxWorks
Ed Jastrzembski	VME, FPGA, PCB Design, Specifications

Hall D Physics Group

Alexander Somov	L1 Geant simulations & efficiencies

Christopher Newport University

Firmware development, architecture, & simulations

Indiana University

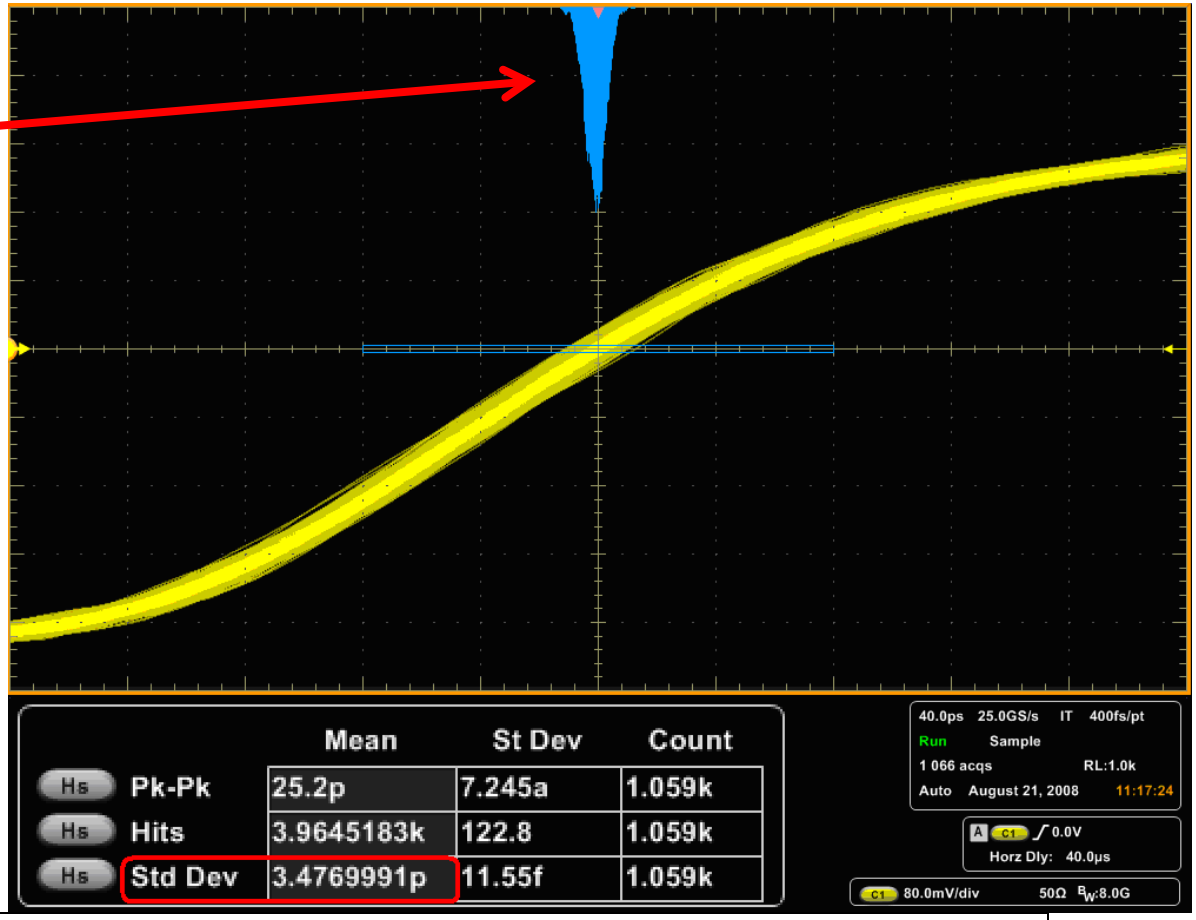
FADC250 Time resolution algorithm

Indiana University Cyclotron Facility

Gerard Visser	FADC125 Development

Clock Distribution Jitter @ Front-End

3.47ps RMS 250MHz Clock Jitter after 150m fiber distribution

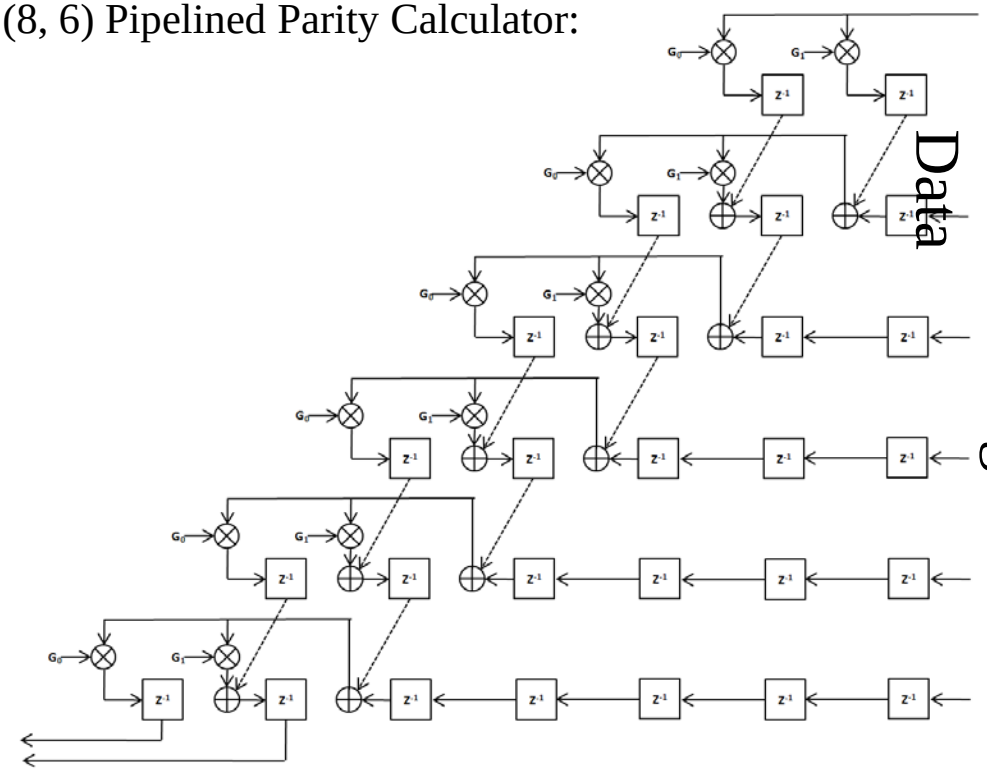


Critical requirement is for low-jitter clock distribution used by FADC250. This has been accomplished by transmitting a dedicated clock on one of the available fiber optic channels used for trigger distribution.

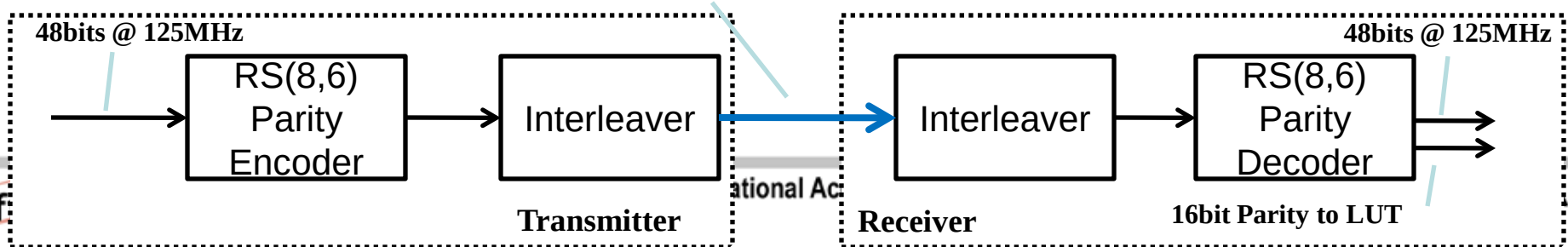
Forward Error Correction (FEC)

- Reed Solomon FEC encoder & decoder, RS(8, 6) GF(256), capable of correcting 1 byte out of each encoded 8 byte frame
- Encoder appends a 16bit parity to 48bit message data (64bits total)
- Decoder calculates parity of incoming 64bit messages, uses 16bit parity in lookup table (LUT) to correct up to 1 byte in frame
- Interleaving 64bit data frames provides burst error correction capability
- Pipelined Encoder/Decoder has fast & fixed latency

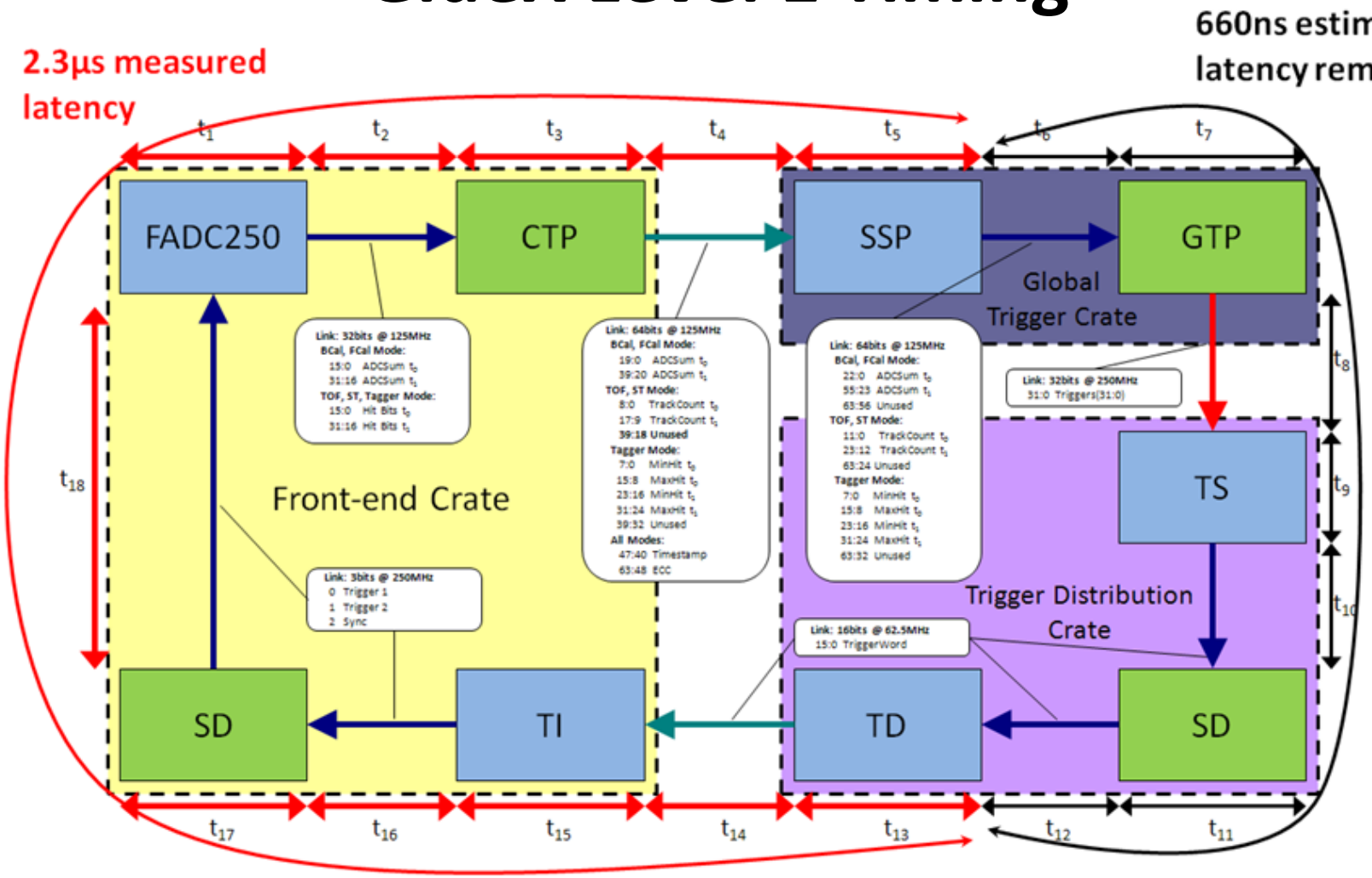
RS(8, 6) Pipelined Parity Calculator:



Latency = ~100ns + 8ns*N
(N = byte burst error correction capability)



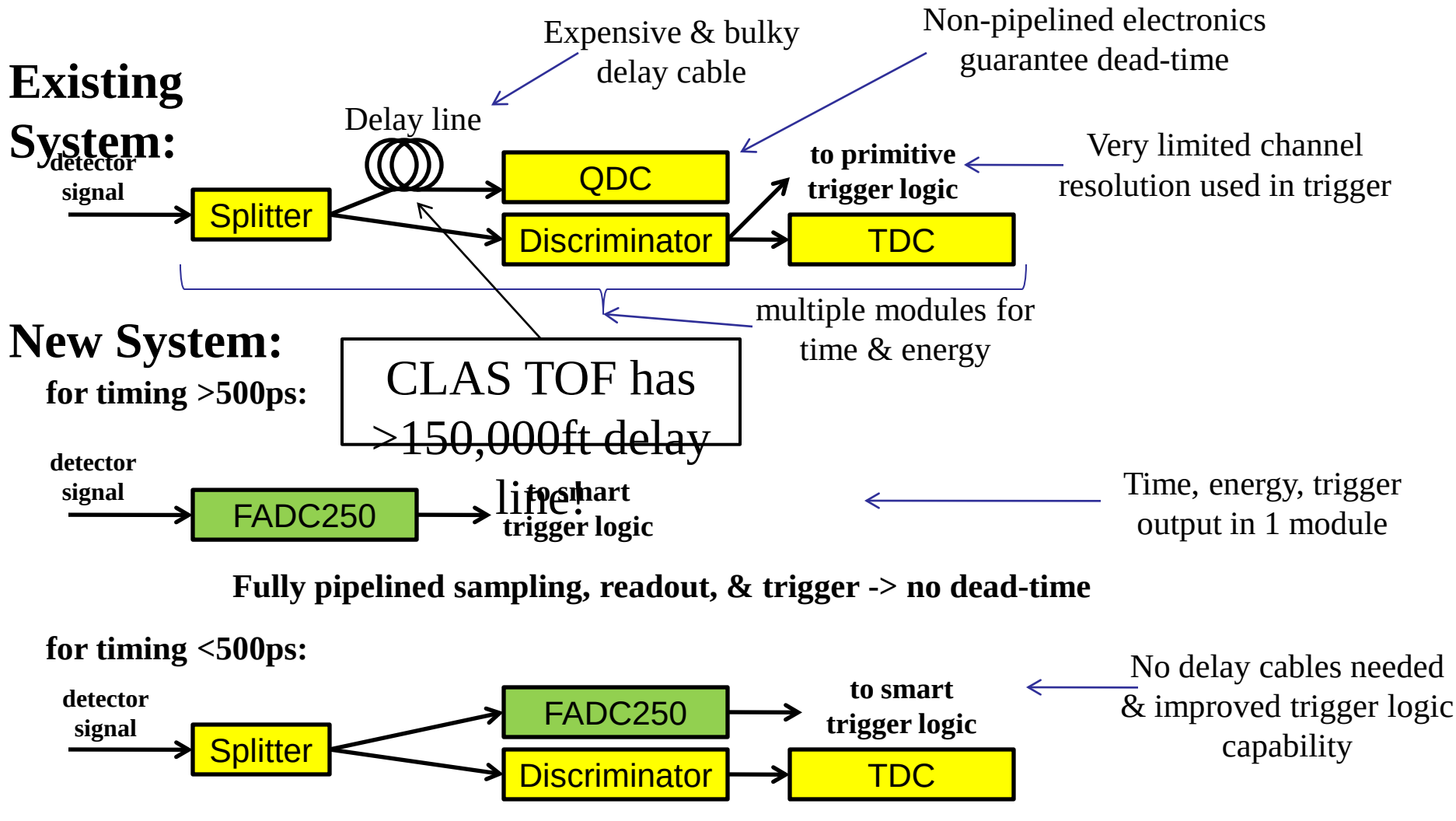
GlueX Level 1 Timing

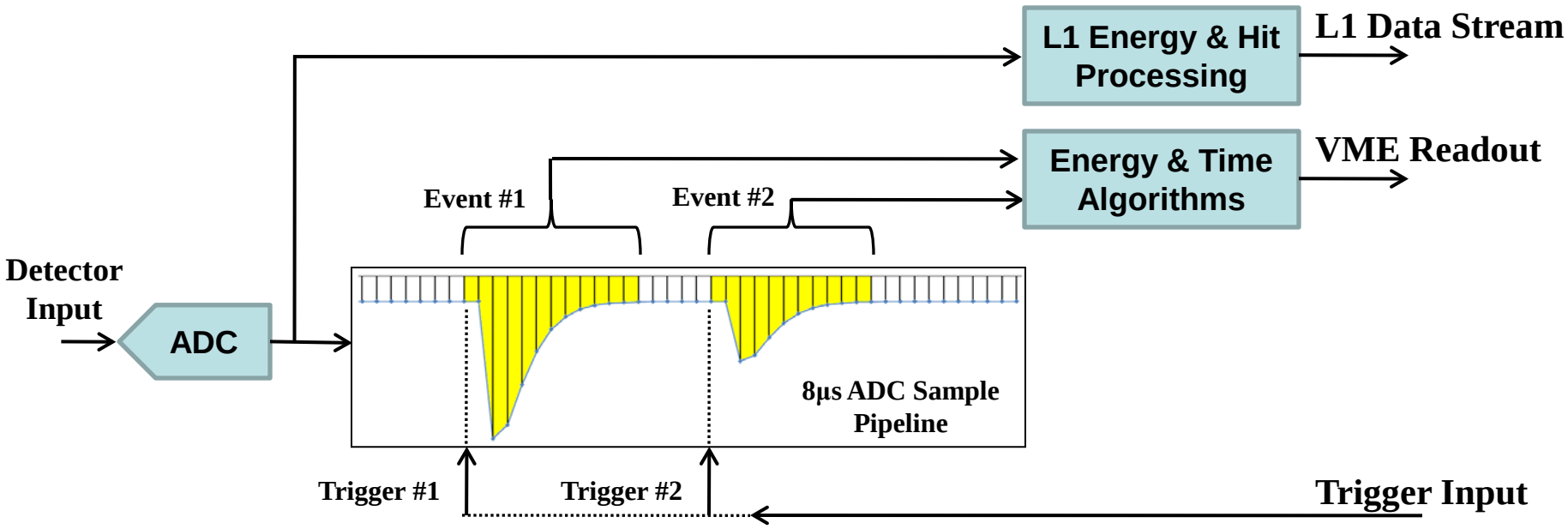


2.3µs (measured) + 660ns (estimated) < 3µs!

Fiber Optic Link
Copper Ribbon Cable
VXS Backplane

Capturing the Pulses…




L1 Energy & Hit Processing
L1 Data Stream
Energy & Time Algorithms
VME Readout
Event #1
Event #2
Detector Input
ADC
8μs ADC Sample Pipeline
Trigger #1
Trigger #2
Trigger Input