12GeV Trigger meeting notes:

11-11-11: C. Cuevas, S. Kaneta, W. Gu. A. Somov, N. Nganga, B. Raydo,E. Jastrzembski,

21-Oct 2011: C. Cuevas, S. Kaneta, W. Gu. A. Somov, N. Nganga, B. Raydo,E. Jastrzembski, H. Dong, D. Abbott

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0. Trigger/Clock/Sync – TI/TD

11 Nov 2011

→Procurements can be started for the TI-TD now so that the production contract manufacturing (CM) is delivered in early spring.
→I^2C issue has been resolved. William distributed a note regarding 4 byte transfers.
→TS 1st article (prototype version) will be ordered soon
→VME Front Panel Distribution boards are presently being assembled in the EEL. Hall B and Hall D groups purchased many of these units. These will need to be tested soon after assembly.

21 Oct 2011

→TI boards are ready for 'customers' and will be used in Hall B and for detector testing by Hall D Users.
→TS design review and resolutions have been completed by William. A few circuit changes have been identified and have been implemented on the prototype board design. Fiscal year '12 money should be available soon so the prototype can be ordered.

23-Sept-2011

-->TS review scheduled for Wed 28-Sept at 1pm. William sent the design paper and other documents for pre-review.
→The new TI boards that were installed in the EEL109 test station work and there were only a few software adjustments to match the latest register changes to the TI boards.

1. *SUB-SYSTEM PROCESSOR (SSP)*

11-Nov-2011

No update

21 Oct 2011

Prepare for production order in Q4 of FY12! Continue testing the SSP with the CTP and GTP. The HPS spring run would strongly desire the method for collecting individual channel sum data for cluster finding techniques. Documentation of these requirements will need to be finalized (at least a draft) soon.

23-Sept-2011

CLAS12 central detector meeting on Tues 4-Oct to discuss hardware needed for these different detectors.

2. *CUSTOMERS*

11 Nov-2011

→Check the FADC250 test log to see where the boards are located. Several of the FADC250 units have been repaired and the boards are being used in several test setups.
→Quick summary: Injector group, Medical Imaging group, Hall D group, Hall B group, DAQ group all have FADC250 plus TI, and SD boards.
→Boards are being collected for the FDC test (EEL-126).

21-Oct-2011
-->16 FADC250 boards, TI and SD have been delivered to Hall B.(Sergey) These units and VXS crate are temporarily in the counting house where Sergey will initially test and configure the modules before relocating them to the hall.
→The test log has been updated to reflect the location and firmware revision that is loaded in the 16 boards. Information on the SD and TI board firmware revision is important also and should be noted in the log.

23-Sept-2011
-->VME FADC250 fan-out bare boards have been ordered, and there is some issue with accounts for the components.
→FADC250V2 boards that were delivered to Hall D, HallB and the Accelerator groups are performing well. A few issues, but no show stoppers.

3. *"B" Switch - Signal Distribution Module (SD)*

11 Nov 2011
→Nick has created the status log file on the M:drive and will keep track of the 6 pre-production units.
→Nick gives a brief summary of his IEEE-NSS conference visit. There are other groups that are using VXS and they also have critical timing requirements.
→Test procedure for acceptance of the SD boards has been drafted. Consideration for using LabView or another GUI is in progress.
→The SD board should be prepared for production order by the end of December. Begin the purchase requisition and specification document now. Activity ID and account numbers will be required so prepare the order as soon as possible.

21 Oct 2011
→Test status and log for the SD boards should be placed on the M:drive. We can keep track of the SD locations, firmware revision and any other relevant notes for each board.
→Nick has completed his poster for the 2011 IEEE-NSS. Please stop by the 2nd floor Fwing hallway to preview the poster.
→Production activities will be scheduled for Jan-2012.
→Test procedures in place (draft)

23-Sept-2011
→All six preproduction boards have passed acceptance testing.
→Will install two new units in the EEL109 test station today. Be prepared for a few changes!
→PLL and jitter analysis continues and Nick is collecting data for his poster/paper at IEEE-NSS
→*Special note: Consider an implementation plan for remote configuration of the SD. Presently the SD only has a JTAG port for new firmware load.

4. *System Diagrams/Fiber Optics*

No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

5. Two Crate DAq test configuration

11 Nov 2011

-->Hai and Bryan have successfully tested a full crate using playback mode. The summing information from each FADC250 payload board has been aligned properly in the CTP to create the crate sum.

→The GOALS of the two crate test station have been successfully achieved and the amount of work is commendable.

→The number of available FADC250 boards is diminishing, but we should set up the two crate EEL109 test station for a long term BER test using as many boards as possible.

→Creating a draft procedure for a full crate test using playback mode and CODA would be brilliant and would allow other personnel to perform full crate acceptance testing. Typical questions, Who, When, What priority?

21 Oct 2011

→Moving one full crate to Hall B on Monday 24-Oct-2011. We have enough boards to continue CTP testing and deliver to Users.

→Hopefully Bryan returns on Monday to help with firmware loading/verification before sending the full crate to Hall B.

-->Collect 16 FADC250 boards to continue CTP testing in the lab.

23-Sept-2011

-->CTP 4 (V5FX70T) is installed and under test in the EEL109 test station. Alignment of the Gigabit serial lanes is the present challenge with ten FADC250 boards installed in the crate. Power up alignment is the key problem right now. Testing is performed with FADC250 in playback mode.

→Round up as many working FADC250 as possible to install in the two crate test station.

→CTP1 and CTP2 (V5LX110T) need to be tested and verified and the testing will occur in the DAQ lab(F117) Hai will need at least 16 FADC250 boards.

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➔ The following is a copy of the test goal list created several months ago:

- **Goals of the integration testing:**
- **-Verify clock distribution through TID->SD and measure jitter to front end boards**
- **-Verify trigger rate and readout rate for a variety of occupancy levels.**
- **-Verity token passing scheme**
- **-Verify CTP operation with sixteen FADC250 @2.5Gbps**
- **-Test playback mode feature on two crates and verify operation with SSP.**
- **-Measure and record overall trigger latency. (Could include SSP)**
- **-Verify full 2eSST readout from payload modules**
- **-Verify TI-D features and use one TI-D in TS 'mode'**
- **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**

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3 June 2011

→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

22 April 2011

The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
See older note dates for the list.

6. Crate Trigger Processor (CTP)

11-Nov-2011
→Hai has tested a CTP with 16 FADC250 in the crate and has successfully aligned the Gigabit lanes.
→One CTP is in Hall B and can be used to produce an energy sum IF that is useful for the Inner Calorimeter folks.
→All four CTP are working and a long term BER test would be very useful.

21 Oct 2011
→Hai will continue with the CTP testing to verify data alignment with 16 FADC250 boards. There are a few issues to resolve, but progress continues. I believe we have enough boards to continue with these essential tests.

23-Sept-2011
→Ben and Scott will investigate the problem with CTP3(V5FX70T) This plan may speed up the effort to get two CTP in the EEL109 test station. If CTP3 is revived, then Hai does not have to continue with the revival, of the CTP1 and CTP2.

7. GTP and Global Crate Developments

11 Nov 2011
-->Testing continues: DDR memory, power, and several other hardware functions have been tested.
→Ethernet development has started, but details need to be defined.
→Investigate how to make the GTP appear as a ROC; (Cmsg). Investigate does not mean implement, but Scott needs to know the requirements for the Ethernet interface.
→Physics equation was loaded into the GTP Altera FPGA and Scott presented the latest results for the latency through the part.

- Altera design approach used 46 clock cycles (184ns) to perform the final GTP equation that was initially tested with the Xilinx FPGA.

→Prepare a test plan for the global trigger crate. (SSP, GTP, SD, TI, TS?)

21 Oct 2011
→Functional hardware testing is virtually complete
→Ethernet development is a work in progress, but needs a requirement document.
→Final Physics trigger 'equation' has been placed in the GTP and testing will continue to verify timing and other parameters. How will Users 'Load' new equations, etc?

***ACTION ITEMS*: Next meeting -Friday 17 Nov @ 10AM in F226**