12GeV Trigger meeting notes:

26-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, B. Raydo; J. Wilson, E. Jastrzembski, S. Kaneta, W. Gu

19-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo; S. Kaneta, W. Gu

12-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo; S. Kaneta, E. Jastrzembski

5-Aug 2011: C. Cuevas, A. Somov, N.Nganga, Bryan Moffit, J. Wilson, B. Raydo; S. Kaneta

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0. Trigger/Clock/Sync – TI/TD

26-Aug-2011

→William reports that the four TI/TD boards that were sent for rework are still at the assembly company.

→We talked about the need to update the TS/Trigger Distribution crate map document to reflect actual TD implementation. Chris has updated the document to reflect the correct VXS pin map. The TD boards are assembled differently than a TI so that the payload mapping matches a standard front end board payload port.

→ There was some discussion about the Trigger Supervisor prototype which can be funded in October. (FY12 funding) More discussion regarding the latest revision of the TI; Will it support legacy DAq systems in Hall A and Hall C? Branch cabling, and other legacy interface connections will need to be reviewed including a few other technical details before the prototype TS is send for order. May be a good idea to set up a meeting with the Hall C and Hall A folks to verify their DAq plans/requirements for the next few years.

19-Aug-2011

William reports that four pre-production boards are still at the assembly company for rework/repair.

TD board has been tested to emulate the Trigger Supervisor crate functions. TS->SD->TD->TI These functions appear to work correctly. William will continue testing all functions of the TI in Trigger Distribution mode... The firmware will be different for TI and TD, so there will have to be a library 'driver' for these different boards.

12-Aug-2011

Four boards sent for rework should be received next week. Acceptance testing is progressing well. There appears to be an issue with setting up the Trig_2 signal in the non-TS crate and William is investigating the problem. The Trig_2 signal will be used to initiate the "Playback" mode and the Trig_2 will need to be issued synchronously to each crate so that the playback data is aligned properly.

29 July 2011

Acceptance testing is going well with six boards working well, and 4 boards have issues with power supplies. (LGA). These boards will be returned to the assembly vendor for rework/repair. One TI-D has been tested with all eight optical transceivers operating at the same time and firmware for the Master TI is ready

2. *SUB-SYSTEM PROCESSOR (SSP)*

26-Aug-2011

Same notes as last week.

19 Aug 2011
Very brief discussion on the recent application plans for the SSP. The CLAS12 SVT group is planning to use the SSP as the front end readout interface to the FSSR ASIC silicon readout chip. Preparing an order for a quantity of ten (10) boards by January 2012 is realistic, and there are only minor changes to the fabrication files that need to be verified.

12 Aug 2011
Final ECO can be applied and the specification started to prepare an order for the SSP required for Hall D. We have delayed the production order, but preparing the production order specification can begin now. So far, the prototype SSP has functioned flawlessly, and has been ahead of schedule.

29 July 2011
Ready to go for full crate testing!

3. CUSTOMERS

26-Aug-2011
→There have been a few emails regarding the distribution of the latest FADC250-v2 boards and we are in agreement to release boards to the Injector group and Alex on 6-Sept-2011. Need at least thirty (30) boards to demonstrate the two crate performance operation using the playback feature.

19 Aug 2011
Week of 5-Sept a few boards will be distributed to a few groups.

EEL-109 lab will retain at least 32 boards!!

12 Aug 2011
No change from last week, but several of the FADC250-V2 boards that did not pass acceptance testing have been repaired. The remaining boards that did not pass acceptance testing will need detailed troubleshooting. Signal data from all accepted boards has been collected and analysis continues.

5-Aug-2011
Week of 22 August is the goal to release FADC250-V2 boards to Injector group and A. Somov.
THE REST OF THE BOARDS WILL REMAIN IN THE EEL-109 TWO CRATE TEST STAND UNTIL END OF SEPTEMBER 2011!!

29 July 2011
Meet on Monday 1 August to establish priorities to test problematic boards that did not pass acceptance testing. Deliver two boards to Injector group. Latest firmware can be downloaded in situ.

4. "B" Switch - Signal Distribution Module (SD)

26-Aug-2011
→Nick reports that we are waiting on the Gigabit backplane (Tyco) connectors. Jeff has ordered these parts and they should be in stock.
→One Rev2 board is fully populated. Acceptance testing is almost complete, and includes tests with the TI and TD boards. The only ECO is a minor change for the ECL output section.
→Nick has performed jitter analysis using different signal frequency inputs and showed the initial results with and without the jitter attenuation circuit enabled. Full SNR plots to show affects of clock jitter/distribution are a work in progress and plans for IEEE-NSS 2011 in Madrid, Espana are becoming reality.

19 Aug 2011

Nick reports that all six pre-production SD boards have been received and pass the visual inspection step. Only two boards have been powered and we will need to order Tyco connectors for these switch cards.

One of the SD boards was tested as the clock distribution unit in conjunction with the TriggerDistribution board.(William). So far no show stoppers and William was able to complete several tests using a TI configured as a full Trigger Distribution board.(8 Fiber Transceivers)

Nick reports that the acceptance test firmware is complete and he has started using the code to test the pre-production boards. We will have to wait for the Tyco Gigabit connectors to fully populate all six new SD boards.

12-Aug-2011

→Partial delivery of the six SD boards is on schedule for the week of 15-August. One FPGA needed to be purchased because of a broken pin issue, but all boards should be here by the end of next week.

→Nick is nearly finished with the acceptance test firmware which will be installed with the standard operating firmware. Acceptance testing of all six pre-production SD boards will begin as soon as the boards arrive. At some point the Rev-1 boards in the existing EEL109 test stand should be replaced and tested thoroughly with a full crate of FADC250-V2 boards and the latest TI boards.

5-Aug-2011

SD delivery on track
Test firmware complete
Front panels (machining) have been ordered.
Rev2 board firmware/register map is identical to existing Rev1 board. Should be no software interface issues.
Need to document results

5. System Diagrams/Fiber Optics

26-Aug-2011

No update.

15-Aug-2011

No update to the draft specification.

29 July 2011

No update to draft specification status. Procurement is not critical until first quarter of FY12. System level drawings have been updated for both Hall D and Hall B to reflect the latest requirements for the parallel fiber optics that will be used for the trigger hardware.

6. Two Crate DAq test configuration

26-Aug-2011

Sixteen FADC250 boards are being used by Hai to verify the CTP code. 15/16 FADC250 are running at 2.5Gb/s with two full duplex lanes.

→2eSST mode has been simulated, verified and implemented into the FADC250 by Ed.

→Latest firmware that includes the 2eSST will be loaded into all FADC250 by next week.

→Will set up playback mode, 2eSST test soon to verify all connections, functions and high data transfer rate. The readout data will need to be pre-scaled, otherwise we will not be able run for a long time at the required trigger rate (200 KHz) because the disk will be full.

19 Aug 2011

→Bryan reports that "Playback mode" is working. No firmware changes needed to existing implementation.

Playback "Trig_2" rate is low. (200Hz)
All channels, all boards have pulse data loaded for playback mode. (100% occupancy)
Data transfer rate??
CTP and SSP are used in the playback mode.

→2eSST firmware has been simulated(Ed) and will be loaded into FADC250 boards soon! The 2eSST readout method will be required to achieve the fully specified trigger rate and readout capability of each front end crate.

12-Aug-2011

→Steady progress with the two crate testing and a total of 27 FADC250-V2 boards are in use. 16 boards in one crate and 11 in another.

→Configuration and test parameters as follows:

- **160KHz trigger rate!!**
- 16 analog pulses distributed to 4 boards. (Low occupancy; 3%)
- Pulse integrating mode
- 50MB/s data transfer rate; 2eVME transfers with token passing
- 40 events/block
- Final trigger created from two CTP, with the SSP combining the two crate trigger data

→"Playback" mode is in the process of implementation and a few small issues remain before testing all channels/boards in this method.

- Amount of readout data will increase when playback mode is used
- Disk space will be a limitation for long test operation
- 2eSST mode will definitely be needed to reach MAX readout rates

→Bryan showed plots of integrated pulse values for several FADC250-V2 boards

- Channel 14 on several boards show unexplained problem
- "Charge" value for active channels appears to have a low RMS value

29 July 2011

→ At least 20 FADC250-V2 boards are populated into two VXS crates in the EEL109 lab. There are a few critical firmware items that remain to be completed before reaching the goal of 200 KHz trigger rate.

- Firmware for 2eSST working with Token passing
- CTP must be programmed to receive Gigabit serial data from each of the 16 payload slots.
- Did I forget anything?!

→ Running in "Playback" Mode

- Firmware and software exists to configure the FADC250 boards with data that will be cycled with the Trig_2 signal. The "Playback" Mode will allow deterministic testing of

the energy summing, and Bit_Error_Rate (BER) testing. The "Playback" Mode also allows testing of every channel without cabling input signals.

➔ The following is a copy of the test goal list created several months ago:

- **Goals of the integration testing:**
- **-Verify clock distribution through TID->SD and measure jitter to front end boards**
- **-Verify trigger rate and readout rate for a variety of occupancy levels.**
- **-Verity token passing scheme**
- **-Verify CTP operation with sixteen FADC250 @2.5Gbps**
- **-Test playback mode feature on two crates and verify operation with SSP.**
- **-Measure and record overall trigger latency. (Could include SSP)**
- **-Verify full 2eSST readout from payload modules**
- **-Verify TI-D features and use one TI-D in TS 'mode'**
- **-Synchronization testing. Quantify number of out of sync events, clock counters etc.**

3 June 2011

→ ***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

22 April 2011

The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→Goals of the integration testing:
-Verify clock distribution through TID->SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
See older note dates for the list.

6. Crate Trigger Processor (CTP)

26-Aug-2011

→See test stand notes

Hai has been successful with CTP firmware that allows for synchronization and high speed data assembly from all the payload slots in the crate. There are a few problems, but he should be able to release the CTP soon so that the trigger from each CTP is a sum function from all the FADC250-v2 boards within a crate.

→Hai created a "Playback Mode" test document

19-Aug-2011
→Hai is using 10 boards with a single CTP, new JLAB record!
Payload slot 6 does not seem to work properly. PPT 1-10 with payload 6 causing problems.
Full crate test by the end of next week 26-Aug to verify CTP Gigabit serial functions!
Once these are tested in the DAq lab, we can move them to the EEL109 test stand.

12-Aug-2011
Hai was not at the meeting, but he has started the firmware modifications and testing needed to receive and process the Gigabit serial data from the 16 payload modules within a crate. Hopefully by the next meeting, we will have an initial test report on the progress.

5-Aug-2011
Hai will begin testing CTP with 16 FADC250-v2 running two full duplex lanes at 2.5Gb/s next week. Hopefully one week will be enough time for implementation and test.

29 July 2011
CTP work will be 2nd priority after the FADC250V2 troubleshooting period. Hai has started testing a CTP with sixteen loop back connectors, and results are promising. Hai will need 16 FADC250V2 to verify his latest CTP firmware, and then the CTP can be installed in the two crate test station. At some point the 'broken' CTP needs to be repaired.

7. GTP and Global Crate Developments

26-Aug-2011
-->Scott reports that the required clocks are running on the GTP board.
→Repair to LGA voltage regulators worked fine
→Test acceptance code is moving forward
→2.5Gb/s and 5Gb/s on two lanes have been loopback tested for one payload port. This test used PRBS with the Altera toolkit.
→Configuration work on Flash storage has started.
→Important test with SSP (Xilinx FX70 @2.5Gb/s) to the GTP Altera device can be started on Monday 29-Aug-2011.

19 Aug -2011
→Scott reports that the fully populated GTP board has been received from the rework company and the power supply circuits function properly.
→DC measurements have been completed, and FPGA JTAG scan works for the two devices.
→Acceptance test firmware is still under development, but initial code is being used to verify board functionality.

12 Aug-2011
DC power check has been measured and documented for the partial assembly board.
Fully assembled board will have the regulator rework wire added to the LGA circuitry.
Conference paper and poster framework started.
Full board back next week, ready for power test!!
Firmware and acceptance test code will become full time activities once the GTP board has been received and power tested.

5 Aug-2011
Partial assembled board is on site! Thorough DC voltage check/verification needs to be completed on the partial power board before powering the fully assembled GTP.

Firmware for acceptance testing is in place.
Ethernet interface has been implemented as a demo using the BeMico EDK.

29 July 2011

The partial (power) board will be shipped the week of 1-Aug. It is a very prudent step to verify and fully test the power board and then proceed with testing of the board that was fully populated.

Acceptance firmware: Development work is a work in progress.
Document is in progress. Updates to specifications should reflect latest hardware revisions.
Full crate could be used to test the Xilinx Aurora protocol with the Altera Transceivers.

ACTION ITEMS: **Next meeting -Friday 2 Sept @ 10AM in F226**