

## 12GeV Trigger meeting notes:

14 & 21 Jan 2011: C. Cuevas, A. Somov, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta

17-Dec-2010: Meeting canceled

10-Dec-2010: C. Cuevas, N. Nganga, B. Raydo, E. Jastrzembski, S. Kaneta, B. Moffitt, H. Dong, A. Somov, D. Lawrence

3 -Dec-2010: C. Cuevas, N. Nganga, W. Gu, , B. Raydo, E. Jastrzembski, S. Kaneta, B. Moffitt, . D. Lawrence, H. Dong, A. Somov

### **Updated prototype board status table:--17-December 2010**

Quantity	Description	Location	STATUS/Contact
8	<u>10 bit FADC250</u> <u>SN001 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN002 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN003 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN004 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN005 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN006 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN007 &gt;&gt;&gt;&gt;&gt;&gt;</u> <u>SN008 &gt;&gt;&gt;&gt;&gt;&gt;</u>	<u>F110</u> <u>Injector Group</u> <u>Injector Group</u> <u>EEL – 126</u> <u>Hai's office</u> <u>F-Wing Lab</u> <u>Hall A</u> <u>EEL – 126</u>	<u>DAQ Lab</u> <u>J. Grames</u> <u>J. Grames</u> <u>FDC test setup</u> <u>Needs repair</u> <u>F117 (A. Somov)</u> <u>Moller setup</u> <u>FDC test setup</u>
1	12bit FADC250	Indiana Univ	New timing algorithm firmware loaded Sent to IU for FCAL testing 12Oct2009 '64x crate and LinuX Cpu sent 24Jan10
4	Crate Trigger Processor	F-Wing F110 EEL109 EEL109 EEL109	Initial prototype CODA Library development Initial prototype - EEL109 Assembled needs testing Assembled needs testing
1	Sub-System Processor	F-Wing(Ben)	Successful testing with CTP. SODIMM testing to be completed.
4	Signal Distribution	V1 EEL 109 V1 EEL 109 V2 EEL 109 V2 EEL 109	CODA Library development Testing with initial TI prototype Assembled and testing is proceeding Assembled and testing is proceeding

### **0. Trigger/Clock/Sync – TI/TD**

#### **January 2011**

→William has completed the TI-D I^2C firmware and has distributed the specifications. Nick will modify the ‘Receiving” side of the I^2C firmware so that it is compatible with William’s changes. William also distributed the test results for the clock distribution jitter and the results are very good with a jitter histogram measured with the Tektronix scope at <2ps!

→Nick was successful in testing the SD board with the original TI board and established I^2C communications to the board before the holidays. There have been several modifications to the SD board, and once the I^2C firmware is fully tested and stable, Nick can proceed to measure the clock jitter with and without the PLL in the distribution chain. All other I/O will also be tested soon after.

→Schedule: The plan is still on track to prepare the TI-D files for production order before the summer. We will use the existing TI-D prototype boards for the two crate tests, but ECO modifications can begin for the schematic and board layout activities.

## **17 December 2010**

→Nick has completed the register map and updated the SD documentation to reflect the latest changes. The firmware for the new SD boards is progressing and the I<sup>2</sup>C communication with the new TI-D has not been completed yet. Nick has set up the original SD and TI to establish communications with the new SD boards.

→William has made minor alterations to the original TI I<sup>2</sup>C firmware that are affecting progress with testing the CTP and new SD. We will need to discuss this further when William returns, and the easiest path to success will be to revert to the original I<sup>2</sup>C addressing scheme.

→There are two TI-D that have been assembled and tested, and these will be used for the two crate test plan in early spring. Do we have enough fiber transceivers to fully load and test a TI-D in distribution mode? Complete test results for the TI-D will be discussed soon.

## **12 November 2010**

William reported that the TID prototypes are ready for testing with the SD and CTP. The I<sup>2</sup>C functions will be exercised and the CTP can be used to verify the TID→Switch card interface.

The definitions for the 32 trigger signals have been determined and to save I/O space on the TS we will send the GTP outputs to the TS from a rear transition module. The connectors will be four 4X infiniband style. These signals are not serial links, but the connectors and cable support the high speed LVPECL signaling that will be used between the GTP and TS.

The TS specification has been updated and circulated for comments. The design of the board is not the highest priority this year because the TID will need to be completely tested with multiple modules in a crate to measure and record performance of the trigger link, clock distribution and zero latency setup.

Six V1290 TDC fan-out boards have been sent for assembly. The initial partially assembled board has been tested and final test results will be reported.

## **1. FIRMWARE TESTING**

### **January 2011**

Firmware details will be listed under each of the module sections for the immediate future. At some point, there will be significant firmware testing for new algorithms that need to be developed. One example is the Hall B cluster finding algorithm, and there are other firmware projects associated with the global trigger modules as well.

### **17-December 2010**

→The 2eSST firmware revision that Ed has created has been used in the SSP and TI-D. Ed reports that he will test the revision also with the FADC250-v2 boards.

→There is a large amount of firmware development activities for each board, so it is not productive to list these here, but suffice it to say, that these development activities have been successful and final firmware revisions will be ready by the time these boards are in production. (End of FY11)

## **12 November 2010**

Firmware updates will continue for the prototype board revisions. Once all tests have been completed for all features of the boards, (SD; TID, for example) the final software libraries can be released.

## **2. SUB-SYSTEM PROCESSOR (SSP)**

### **January 2011**

No test report at the last meeting, and the SODIMM memory test has taken a lower priority given Ben's other projects. We will plan to use the SSP in the two crate test this spring and it

may be too early to start development of the CODA library for the SSP. It will be later in the fiscal year before the SSP can be tested with the GTP prototype module.

### **17-December 2010**

→The SSP prototype is virtually complete with SODIMM memory testing and P0 gigabit lane testing still to be fully verified. The SSP BGA issues have been resolved and the design will be virtually unchanged for the production version.

→The SSP has been proposed as a data readout/trigger interface for up to 32 detector readout devices. The proposed idea may be a perfect solution for the Hall B central detector readout scheme and the fiber links from up to 32 custom readout devices can be connected to a single SSP. The SSP engine would manage the data reduction and local trigger algorithms for up to 32 detector readout devices, and as a payload module, the detector data will be read out through VME2eSST. Nice development and further details will emerge soon.

### **12 November 2010**

Ben reports that other high priority work has pushed the SSP testing and firmware iteration activities back. The SSP has been tested and there will be minor ECO to the prototype. There are several tests (SODIMM for example) that will need to be completed, but the SSP is ahead of schedule and will be used for the two crate test that is planned later this year.

### **29 October 2010**

Ben reports that the SSP testing will continue and that the board was repaired (re-balled/reflowed) so that the intermittent pins are now working. The SSP complete verification will need to take a higher priority to fully qualify the SSP design. At some point soon, this module design and VME register map will need a CODA ‘driver’, but there are still many tests to perform.

### **22 October 2010**

Ben reports that the SSP has been repaired and has been sent back to Jlab. He will continue testing the SSP and can continue to fully check all functions. (SODIMM – DDR2, etc). The module will need to be tested with the TI-D, and of course the SD board to verify the initial global trigger crate ‘system’. We can also use the existing CTP in another crate to record and test data transfer from two CTP to a single SSP.

### **1 October 2010**

Ben has tested virtually all functions of the SSP with the exception of the SDRAM and output serial streams to the GTP. The board has been sent to the assembler for reflow/repair of one of the FPGA that appears to have solder connectivity problems. Fiber transceivers have been exercised and BitErrorRate(BER) testing has been measured to be well within limits.

## **3. CUSTOMERS**

### **January 2011**

→Not a specific trigger module topic here, but preparation for the pre-production order for the FADC250 boards is virtually complete. The Medical Imaging group and Injector group will purchase two boards each, in addition to the 35 pre-production units.

→Small pre-production builds for the TI-D and SD boards make sense because there are several Users/Groups that will need to begin testing detectors soon after the two crate testing has been completed.

### **17-December 2011**

→There may be a need from the Medical Imaging group to use a single FADC250 module for verification of new front end electronics designs. The use of a single board will be an interim solution until the new custom readout design is complete.

## **12 November 2011**

The injector polarimeter folks presented results from a FADC250 board and will continue to develop their applications. Another FADC250 was given to them. I will not be long before all the original prototype boards will be replaced, but those prototypes certainly produced a great deal of development success.

## **29 October 2010**

No new reports and no new customers lately.

## **4      "B" Switch - Signal Distribution Module (SD)**

### **January 2011**

→ Some redundancy here, but Nick has modified the I<sup>2</sup>C firmware to be compatible with the changes that William created for the latest TI-D design. The new firmware will be loaded in the SD and thoroughly tested. Bryan requests that the old SD be updated with the latest I<sup>2</sup>C firmware. At some point the I<sup>2</sup>C firmware can be loaded into the CTP and verified with the TI-D also.

→ Initial test results for the SD have been reported, and once the communication firmware is resolved, the jitter analysis for the clock signals will be measured. Full verification of all other SD I/O will be tested also, and then work on revising the schematics and board layout can begin.

### **17-December 2011**

→ Progress continues and the two rev-1 SD boards have been updated with the latest ECO for the power supply section. Nick has set up the original SD and TI to establish the I<sup>2</sup>C communication link, and has loaded the I<sup>2</sup>C firmware on the new SD board. The new TI-D module uses a different I<sup>2</sup>C address scheme which does not work with the original I<sup>2</sup>C firmware. This will have to be resolved when William and Nick return from the holiday break.

→ Hall B purchased components for eight(8) SD boards, so as soon as ALL ECO have been identified and crate testing is complete, the final revision of the SD will be ready to order.

→ Nick has updated the SD documentation and the new front panel design is complete and looks nice. Significant testing remains for the thorough analysis of the PLL clock jitter attenuation function including all other SD functions using a full crate of FADC250 are on the horizon.

## **12 November 2011**

The two rev-1 SD boards are being tested and minor ECO will be required. Nick will continue testing all sections and has started the firmware revisions. The new firmware will need to be tested soon with the revised TID and performance results for clock jitter distribution etc will be recorded.

Scott has completed two switch card test boards that will be used during testing of the FADC250 plus the SD card. These cards provide loopback signaling, clock distribution, and test points for the SD and FADC250 modules. The boards will be received and assembled soon.

## **5. System Diagrams & Test Stand Activities**

### **January 2011**

→ The Hall D trigger fiber optic drawings are complete and have been sent to at least one company for price estimates. The price estimates will include installation labor and testing. Final lengths will be **required** before the final order is placed. Drawings for Hall B will need to be started soon.

→ 1<sup>st</sup> article VXS crate has been received and will be tested in the EEL109 lab. This crate will be used for the two crate daq/trigger testing. I believe we have all peripheral hardware/fiber to perform the two crate testing in the spring.

→ We had a brief discussion about the software effort needed for testing and operating all of the modules needed for the two crates DAQ/Trigger test. CODA can be used to configure all the modules and will certainly be the engine to collect the data from the modules. Displays of plots for trigger rate, data readout rates and all other essential test results will be needed. There was also a discussion on what single board computers (CPU) will be used for the two crate testing and Bryan described the existing CPU that have been evaluated by the DAQ group.

### **17-December 2010**

→ Mark and Chris have revived the CD3 drawings for the trigger fiber optic infrastructure drawings. Ben and Chris met with a supplier of the fiber and patch panels and we will request a price estimate for the fiber trunk cables included the patch panels and patch cables. The drawings will be updated to reflect the cable lengths as shown in the Hall D 3D CAD model. (Tim and Chuck) This work will have to be completed for Hall B at some point before FY12.

### **12-November 2010**

Preliminary trigger system drawings were produced for CD3 reviews, and the number and style of fiber optic cabling was included. A price estimate will be requested from at least one source soon, to verify that the cost will be within the scope of the planned budget.

### **16 July 2010 (Keep this because it needs to be implemented and tested at some point)**

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

- A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
- B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

- A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

- B) Multiple triggers will occur for a given trigger ‘window’. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger ‘window’. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP ‘window’ and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

## Crate Trigger Processor (CTP)

### January 2011

→Nick will produce the new I<sup>A</sup>2C firmware that is compatible with William's TI-D interface. This block of code will be instantiated into the CTP as soon as reasonable.

→Scott has started testing with one of the original CTP modules and will also test the two 'new' CTP. The 'new' CTP includes different FPGA (FX70T) but other than that, the modules are identical. Goal is to report test results by 14-February-2011.

### 17-December 2010

→The old I<sup>A</sup>2C firmware in the CTP is not compatible with the new I<sup>A</sup>2C revision that was implemented by William in the new TI-D. Brain has a CTP and new TI-D but will need to have William modify his I<sup>A</sup>2C firmware so that he can complete the work needed for the CTP software library.

→The heat sink material has been machined and the front panels also. The machined panels and heat sinks will be ready for assembly by the New Year.

→One of the CTP has been assembled with a high speed grade V5FX70T FPGA and will be used to fully qualify the v2 FADC250 at 5Gbps/lane.

→Scott will work with one of the original CTP to become familiar with the design, Chipscope, and other features of the board. Scott can then begin testing the new CTP assemblies in January.

→Scott has completed the design for two switch card test boards and these have been assembled and are in use by Hai and Nick for testing their boards. The documentation for these switch card test boards has been completed by Scott.

### 12-November 2010

Two more CTP have been received and the heat sinks, front panel are almost ready for assembly. These modules will need to be tested and prepared for additional testing (5Gbps) with the version 2 FADC250 boards.

Bryan has one of the initial prototypes CTP and will continue testing the software library with the latest TID firmware.

## 6. Projects for FY11 (GTP and Global Crate Developments)

### January 2011

→Scott has shifted to working on the CTP for a few weeks, but the effort for the GTP schematic continues to show good progress. Virtually all the integrated circuits for the GTP design have been specified.

→The interface between the GTP (front panel) and the TS (P2-rear panel) has been defined and library parts created for the GTP. We should consider purchasing the cable and connectors soon, and any other GTP components that may show a long lead time.

### 17-December 2010

→We dedicated a significant portion of the 10-Dec meeting to discussion of the trigger board and system schedule for the remainder of FY11 and test integration activities planned for FY12 including what I call "Pre-commissioning" activities that will need significant resources once the crates and modules are installed in the hall(s).

→The preliminary schedule was distributed and the engineers for each board development project provided feedback and adjustments were made to show the activities needed to achieve a reasonable estimate-to-completion for almost all the trigger system board designs. It is realistic to expect that the final board designs will be ready for production orders as soon as FY12 begins and possibly sooner. Budget allocations for the volume purchases of SD and TI-D for instance, may need to be moved to FY12, but the goal is to have the board design files ready for order by end of FY11.

→Alex and Chris have created schedules that show activities from the Hall D P6 schedules and there are several activities that will need to be assigned new IDs.

### **12-November 2010**

→Large portion of the meeting was to discuss the ‘integration’ testing required for all of the latest revisions of the front end trigger modules. Virtually all the boards are at the first revision stage and will need to be tested with in a full crate. The FADC250 pre-production schedule is progressing well, so the SD & TID will need to be fully tested by the time we have more than 16 FADC250.

#### **→Goals of the integration testing:**

- Verify clock distribution through TID-SD and measure jitter to front end boards
- Verify trigger rate and readout rate for a variety of occupancy levels.
- Verify token passing scheme
- Verify CTP operation with sixteen FADC250 @2.5Gbps
- Test playback mode feature on two crates and verify operation with SSP.
- Measure and record trigger latency. (Could include SSP)
- I am sure there are more milestone tests, but we can iterate the list.

I have an integration test schedule developed and we can discuss the dateline at the meeting.

**ACTION ITEMS: Next meeting → Friday 28 January 2011 10AM in F226**