Trigger meeting notes:

27 March 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, E. Jastrzembski; J. Wilson

20 March 09: C. Cuevas, A. Gupta, B. Raydo, F. Barbosa; M. Taylor; A. Somov, E. Jastrzembski; J. Wilson

6 & 13 March 09: C. Cuevas, A. Gupta, H. Dong, B. Raydo, M. Taylor; A. Somov, E. Jastrzembski

27 Feb 09: C. Cuevas, A. Gupta, B. Raydo, J. Wilson, M. Taylor; A. Somov

Updated prototype board status table:--27 March 2009

Quantity	Description	Location	STATUS
5	10bit FADC250	EEL109/DAQ Lab	NEED to gather all boards and verify firmware version and prepare for full crate testing
1	10bit FADC250	ORNL – D. Curry	SN#003 Evaluation
1	10bit FADC250	EEL109/DAQ Lab	Experiment testing successful! Will be returned to the EEL109 lab
1	10bit FADC250	EEL109	Needs repair; Clock Issues
1	12bit FADC250	EEL109	Received 12Mar09 Start SNR tests
4	Trigger Interface Trigger Distribution	EEL109/DAQ Lab	Trigger testing
5	VME -- FP-SD Front Panel – Signal Distribution	EEL109/DAQ Lab	Complete Use in test crates
1	Crate Trigger Processor	EEL 109	Successful testing with multiple FADC250!!
1	Crate Trigger Processor	EEL 109	Initial tests started
2	Signal Distribution	EEL109	Initial functional testing continues. 2nd board to be tested week of 30March

0. Trigger/Clock/Sync – TI/TD

27 March 2009

→Sebouh can proceed with further development using the VXS test crate by adding wires to the CTP boards so that they receive the I^2C signals from PayloadPort 10. The 20 slot backplanes are occupied with SD testing, so having the alternative method to continue the CTP interface control testing will be useful for a few weeks.

→I^2C control and monitoring for the SD board will begin by the week of 6 April. Abhishek and Sebouh will have to work together to ratify their respective firmware so that control of the SD board is robust and ready for testing in the 20 slot backplane crates

20 March 2009

Sebouh continues with his work plan for the Virtex5 monitor implementation. The SD boards are presently being tested, so testing the I^2C interface and GUI will have to wait until Abhishek and Mark have initially tested the functions of the SD boards. Sebouh can test his latest firmware with the CTP units at his earliest convenience and coordinate this work with Hai.

13 March 2009
Sebouh sent his draft report on Friday. He will return from spring break next week.
All three FPGA on the CTP are communicating with his GUI and interface code. He can continue with the Virtex 5 monitor if the SD is not ready to test.

27Feb 2009
Sebouh will complete his firmware and GUI documentation and has worked with Hai to implement the Virtex V monitor functions. The monitor functions will provide continuous data for the core temperatures, voltage and current of the Virtex V FPGA on the CTP. At some point soon, it may be a good idea to work with Sebouh to alter the GUI so that we can use a LabView interface. His firmware and GUI will be used to control the SD also, and will be tested on the SD as soon as we receive the SD boards.

1. FIRMWARE TESTING

27 March 2009
→Ed reports that the SST mode is working on the FADC250 module and he is testing the board with the token passing scheme. The Retry* signal will need to be wired on the FADC250 Altera Fpga to satisfy the SST block transfer features.
→By the week of 6 April, the new SST firmware can be copied to the FADC250 boards and testing can begin with the boards in the 20 slot VXS crates. There are several tests to complete by using the SD module as the token pass 'hub', including the logic to control the BUSY signals from each FADC250 modules.

20 March 2009
Ed reports that he has successfully tested a single FADC250 board with his latest firmware for the Source-Synchronous-Transfer (SST) mode. VME bus transfer rate testing and modifications to the "Coda" driver will be updated and then this new firmware will need to be stored on each FADC250.

The SST readout has been tested with a single FADC250 board, so the token passing scheme will have to be verified soon. Provisions for wiring the token passing is possible with the VME P2 connectors, and the SD token passing function will have to be verified as soon as we have several FADC250 modules ready with new firmware.

13 March 2009
Ed reports that the SST VME interface firmware simulation is complete. Initial testing with a single board is underway. Progress continues and debug has started. At some point soon after the SST interface is verified, all the proto boards need firmware verification and update if necessary.

27 Feb 2009
→Ben reports that the 64bit bus transfer is now working properly and that the firmware has been updated on the Trigger Interface boards. The firmware for the FADC250 boards needs to be verified and updated so the latest VME interface code is loaded.
→I know Ed has been working on the VME-SST firmware and hopefully will be ready for a test soon. Stay tuned for an update next meeting.

2. *SUB-SYSTEM PROCESSOR (SSP)*

27 March 2009
The V5LX30T FPGA has been added to the schematic and the VME interface and local control bus will be managed by this chip. The MGT on the LX30T will be connected to P0 and ultimately to the GTP. Two V5FX70T FPGA will be added to the schematic to interface to the eight Fiber Optic transceivers. Plenty of schematic work to do, but I am using this design as my

full fledged tutorial with the new Altium CAE/CAD tools. So far so good, albeit my slow progress.

20 March 2009

Progress continues and the VME sections and front end fiber optic sections have been added to the hierarchy drawings. I need to add the three FPGAs to the design this week and then start the process of initial pin assignments for the FPGAs. Plenty of other work to finish for the schematic, then it will be board layout time.

13 March 2009

SSP schematic presented by Chris and the work is progressing. The Altium tool is quite extensive and my goal is to use this design to fully understand the FPGA tools that are included with the 'Unified' license. Hierarchy levels of schematics I believe will help also with the documentation for later use. I will use the VXS payload board that was used for the TI as the template for the circuit layout as soon as I get to that point.

27 Feb 2009

Jeff reports that the XC5VLX110T part is the same pinout as the VC5VFX70T that we are planning to use for the front end SSP FPGA. If this is the case, then I can use the LX110T part that is included with Altium and continue with the schematic and start to become familiar with Altium's FPGA tools. So far Altium is rather useful and has nice features that will need to be fully tested, especially with FPGA that have high pin counts.

3. CUSTOMERS

27 March 2009

Data from the latest Hall A experiment will be requested by Chris for a brief presentation by the Hall A Users. I believe they were successful, and it would be interesting to hear about the results.

There is a request to use a single FADC250 as an upgrade to the Moller Daq in Hall A in about 4 months. Hai is presently working on the changes to the firmware (V4FX20) that will be necessary for the experiment proposal. The experiment does not require the use of the VXS trigger data transmission and testing can begin after the work for the trigger test stand is complete.

20 March 2009

Effectively the same notes from last week. The FADC250 board has been returned by the Hall A folks, and we can integrate this board back into the test stand.

The trigger test stand area is a busy place, so we will have to coordinate testing of the 12bit board with the continued testing of the SD boards. The SD board should take highest priority and will need only a single crate to continue the initial functional testing.

13 March 2009

- ➔ The 12 bit FADC250 board has been received and is in the EEL109 test stand. Plan to setup the test for SNR next week. May be able to test with all boards running the new SST transfer firmware.
- ➔ The Hall A group will return a 10bit FADC250 board soon. Initial reports from Hall A Staff are positive data analysis will hopefully be presented soon.
- ➔ Doug Curry @ORNL has demonstrated the FADC250 to his group and is presently writing a proposal to use the board for Accelerator Improvement Projects (AIP). The board is due back by the end of next month.

27 Feb 2009

→ I requested the return of the 12bit FADC250 from Matt Sheppard @IU. The SNR tests can be performed with the 12bit board, and quite possibly with more boards transferring data on the

bus at least in D64 mode. If the VME-SST readout is ready to test, it would be interesting to see if that bus mode has any effect on the SNR value.

→Need to request the 12 bit board from the FCAL group so that we can perform a SNR test. It would be a good comparison to the 10 bit SNR test. We would need the 12bit board for only a few weeks.

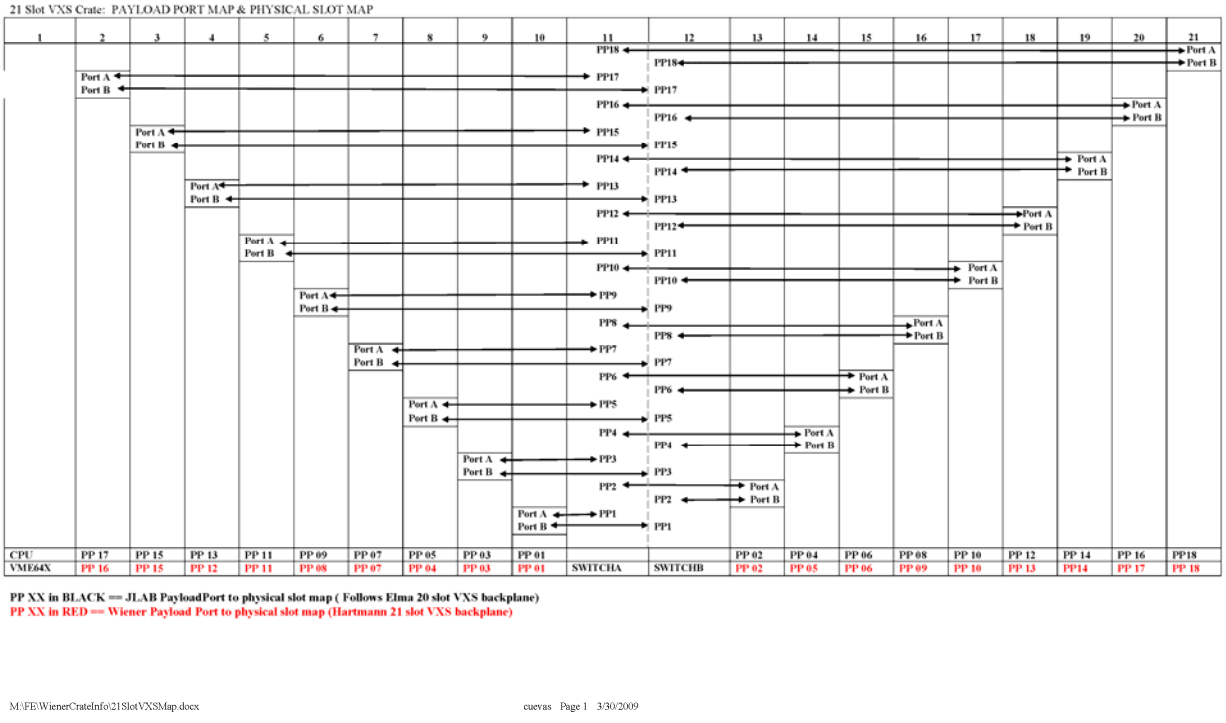
→D. Curry at ORNL has a 10 bit board as an evaluation unit until May 1. He has successfully operated the board and will present the Jlab board as an inexpensive solution for a beam diagnostic upgrade application. My hopes are that their group can provide extra money for the next revision (pre-production quantities). Details will be presented soon.

4 "B" Switch - Signal Distribution Module (SD)

27 March 2009

→Abhishek and Mark's measurements of the clock jitter as it is received on the FADC250 were presented and the results are very promising. Initial results for the jitter of a received 250MHz clock is ~3ps and the histogram showed a peculiar 'picket fence' display.

→The Wiener (Hartmann) backplane is indeed different than what was specified and apparently they were able to save 8 layers on their backplane design by adopting a different PayloadPort map. See the drawing below: (pdf file so you can zoom)



We will continue to test with both VXS backplanes and record any differences. The PayloaPort mapping from Wiener is their creation and effectively makes the design a sole-source. Several companies sell 20 slot VXS backplanes using the 'Elma' port mapping, and we have designed the SD and TI boards to follow. The Wiener backplane is not unusable, but it adds a bit of confusion to an already crowded room full of slots, port maps, pins, lanes, switch slots, etc.

20 March 2009

→Testing results were presented by Abhishek and the scope photos presented show the clock, trigger, and sync signals driven from the SD board to a payload slot. The payload slot is only instrumented with passive components and the proper biasing network to receive and test the SD signals. There were a few questions regarding the O'scope photos, and Abhishek and Mark will continue to verify clock jitter, and other essential tests on the SD prototypes.

→The repairs to the LGA66 regulator parts were successful, and the DC voltages are stable. Ripple measurements need to be measured for all voltages on the board, and these measurements should be compared to the manufacturer's specifications.

→Abhishek reports that the Altera FPGA is functional and he is able to load firmware to complete the initial testing of the module. Further firmware development is not presently the highest priority, but will be needed to fully verify the functions of token passing, BUSY, and implementation of the I^2C control features.

→The Wiener (Hartmann) VXS 21 slot backplane has been organized differently than what was specified. For some reason the PayloadPort to physical slot map that was specified was not followed. Abhishek and Mark discovered the different mapping, and have identified the PayloadPorts for the Wiener backplane. Tests can continue, but the Wiener mapping adds a bit of confusion. More details next week.

13 March 2009

Five LGA-66 regulator parts were replace on each of the SD prototype boards and a trace was added to connect the Track pin to VIN. These boards were received in record time and the DC voltages are stable. No report given at the meeting, and these DC voltages need to be recorded and include ripple measurements.

A few other problems were mentioned having to do with the circuit section that receives the clocks from the TI. These problems have been resolved and will be discussed at the next meeting.

27 Feb 2009

Two SD boards were received from the assembler and they corrected the placement of the 12 QFN parts. DC testing resumed and another problem was identified.

At first it appeared to be another assembly problem, this time with the LGA66 packages for the LTM4604 regulator parts. The DC voltages were not regulating correctly unless pressure was applied to the regulator parts, but in fact the Track pin needs to be connected to the VIN pin. For some reason this was omitted on the design, so we will have to rework the board to add a connection for each regulator and replace the parts. The LGA66 package is fairly new in the industry, and we have located a company in Texas that has had success with this type of part for rework and repair. This company was used when we replaced the engineering samples (ES) series of VirtexIV FX20 FPGA to the commercial parts. They are company that specializes in rework and repair of fine pitch components.

5. System Diagrams & Test Stand Activities

27 March 2009

→Jeff presented a preliminary route of the proposed 'single Fpga' idea for Rev-1 of the FADC250 board. There will be iterations, and there will be another Fpga for the VME interface and local control bus. The Gigabit transceivers were not routed to P0, but the position of the single FPGA is planned to accommodate the lanes needed. Plenty of other details remain, and the FADC250 Rev-1 design ideas will continue.

20 March 2009

→Jeff has started to look at the board routing challenges for the FADC250 design revision idea that uses a single FPGA to interface all 16 ADC signals. A second FPGA will be used to manage the VME interface.

→At some point soon, we will need to look at cost issues for the FADC250 Rev1 design.

13 March 2009

→Test stand activities are abundant lately which is a good sign!! The CTP and SD testing activities dominate the action and soon we will configure the two crates with the hardware necessary for creating data needed for the conference paper.

→This section will be updated soon to include the work activities required toward the 2nd (and final) version of the FADC250. Jeff and Hai have started work on a few conceptual ideas and will need to study the impact of routing, thermal, and cost issues before deciding on the final solution.

→Two abstracts submitted to the IEEE-NPSS Real Time Conference 2009 have been accepted. The topics are (obviously) related, and the poster session will compliment the talk with details of the hardware interfaces and other challenges. April will be a busy month of testing the two crate system with CTPs, SDs, FADC250s, and of course the TIs all running in unison. GREAT Work!

27 Feb 2009

The block diagram that shows the details of the trigger test stand hardware and which components will be presented in the Real Time Conference paper was discussed. Critical items for these tests are obviously the SD and two CTP units. The TI and Flash boards are ready to go, and there is quite a bit of work to gather useful results to post in the conference article.

6. Crate Trigger Processor (CTP)

27 March 2009

Both CTP are running in the twelve slot VXS crates and Hai has been successful with transporting 'trigger' data from three FADC250 boards to the CTP and then to the 2nd CTP that is operated as an SSP. He has set up a test program and is using Chipscope© to register an error condition. The plan is to continue testing in the twelve slot crates, and then very soon, transfer these boards to the two 20 slot VXS crates and use the SD in each crate to distribute the clocks and common signals to each module in the crates. Once the modules have been configured in the crates, we can distribute signals to various input channels and configure the system to TRIGGER on a particular sum. There are many other test results to record for the IEEE-Real Time Conference poster.

20 March 2009

Hai has successfully tested the 2nd CTP and a small problem developed with a part after the initial success. The part has been removed and bypassed for now. The firmware has been developed for the 2nd CTP to operate as an SSP. This firmware has been simulated and implementation and testing are a work in progress. In SSP 'mode', the 2nd CTP receives trigger data from the first crate CTP, and also trigger data from FADC250 modules that reside in the 2nd crate. The multi-fiber link is used to transmit the data between CTP and the method to bond the multi-gigabit (Aurora) lanes is presently being tested and refined. Soon, possibly next week, we can configure the two Wiener VXS crates with all of the FADC250 boards that are needed for the trigger system testing.

13 March 2009

Three FADC250 boards have been successfully operated with the 1st CTP module. Each FADC connects to one MGT on each of the three FPGA on the CTP. These tests have been performed in a twelve slot VXS crate so serial data from PPT 11-18 have not been verified. The 2nd CTP is presently being tested and no problems to report. We will need to move these tests to the twenty slot backplanes soon to verify the serial connections from PPT 11-18.

Data alignment testing and debug has been successful and additional firmware has been developed to drive trigger data from one CTP to the other using the fiber port path.

Block diagram for the paper will be presented at the 27March meeting. (Chris)

27 FEB 2009

→Hai was unable to be at the meeting but told me that he has tested the Gigabit transceivers from multiple payload ports into each of the three FPGA on the CTP. A quick list below shows the connections from the payload ports to the FPGA (X == 1 gigabit lane)

U1-XC5VLX50T – 5 FADC250 (2X each so 10X used; 2X spare) Payload Ports: 8.10,12,14,16

U3-XC5VLX50T – 5 FADC250 (2X each so 10X used; 2X spare) Payload Ports: 7,9,11,13,15

U24-XC5VLX110T – 6 FADC250(2X each so 10X used; 4X used for Fiber Optic output port)

Payload Ports: 1,2,3,4,5,6

Data alignment testing is going well and soon Hai will need the SD module to distribute the clock and sync signal from the TI and increase the number of FADC250 boards to test all of the input lanes to the CTP.

→All of the parts for the 2nd CTP have been received and the assembly kit is ready to ship. The assembly PO is ready, and Jeff will ship the parts and board to the assembler next week. Delivery is one week, so we should see the 2nd board during the week of March 16.

ACTION ITEMS: **Next meeting will be Friday 3 April 2009 → CCF228 @10am**