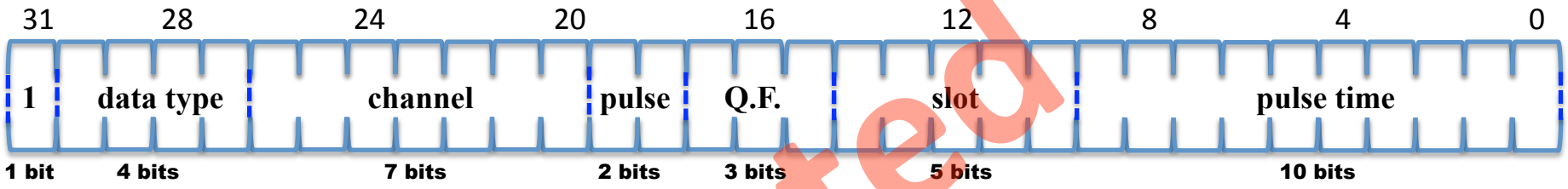
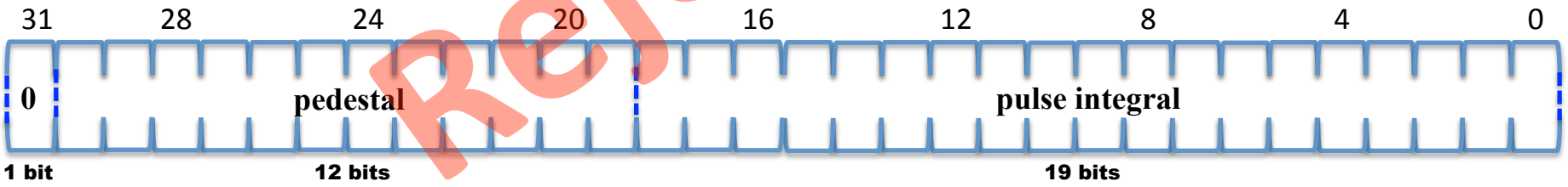
Option 1: Coupled words w/ pedestal

First word



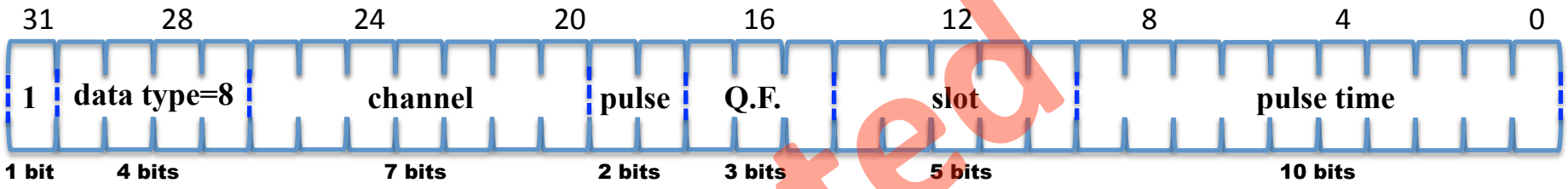
Second word



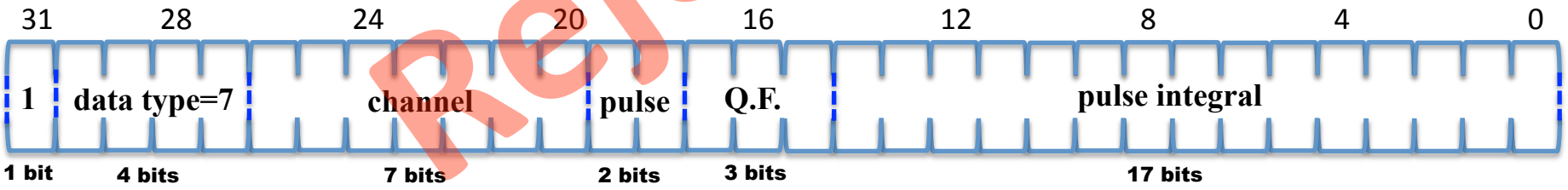
Option 2: De-coupled words w/o pedestal

(Closely follows FADC250)

First word: Pulse time

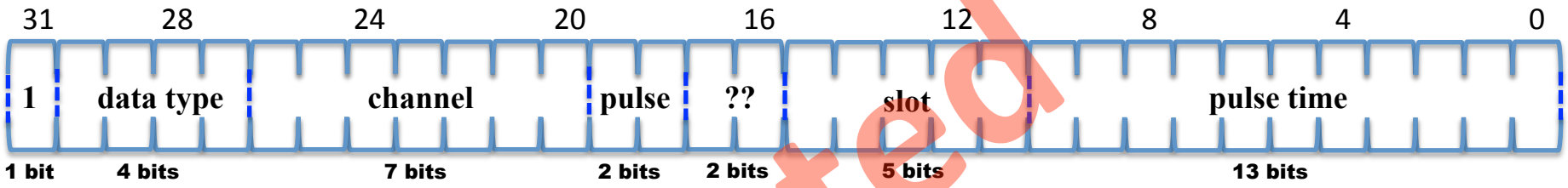


Second word: Pulse integral

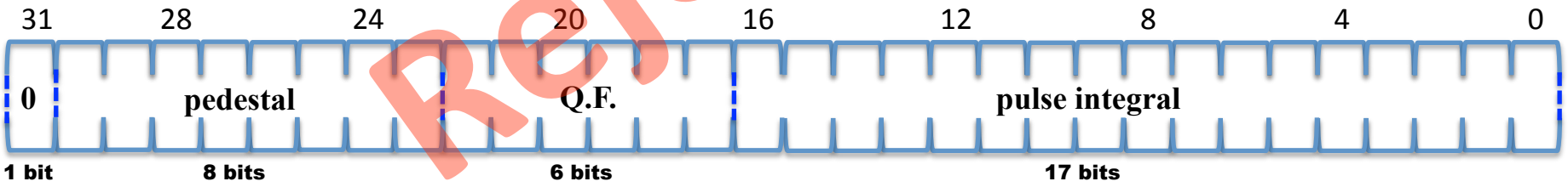


Option 1a: Coupled words w/ pedestal

First word

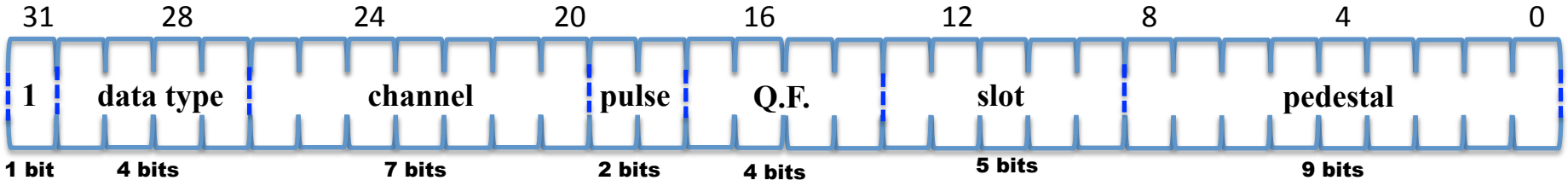


Second word

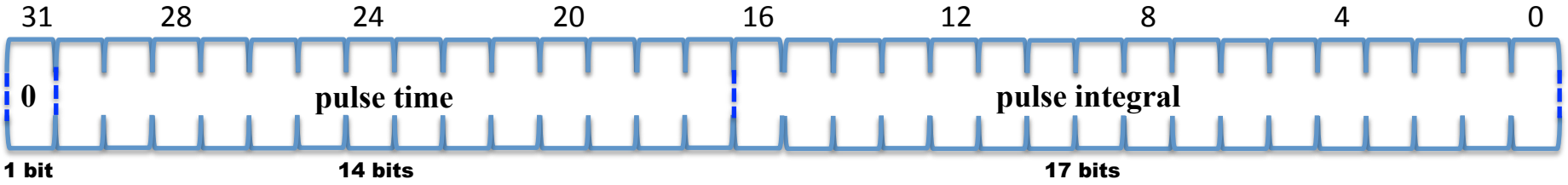


Option 1c: Coupled words w/ pedestal

First word

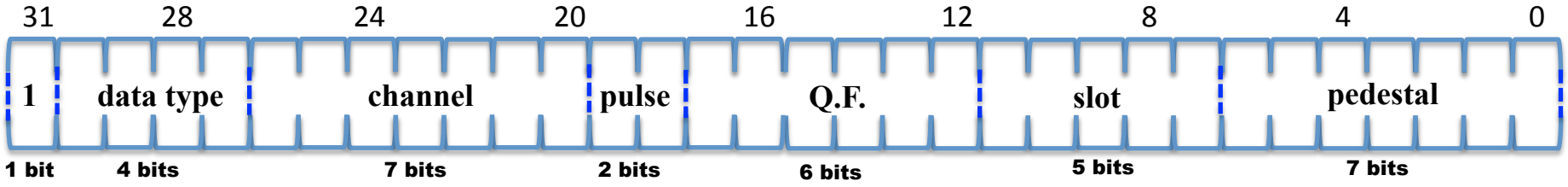


Second word

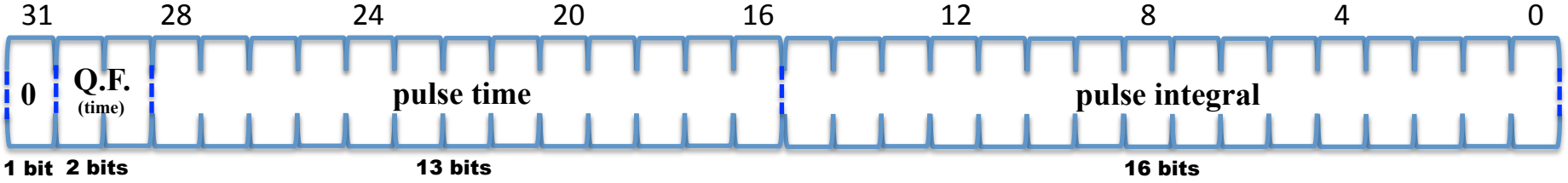


Option 1d: Coupled words w/ pedestal

First word



Second word



Pedestal subtraction

- FADC's will use pulse finding algorithm to identify pulses and analyze samples in pulse region to generate digitized values
- Pedestals (by definition) are the digitized values in regions where no pulses exist
  - Option 1: Measure and subtract pedestals event by event in FADC125 FPGA
    - Suppresses uncorrelated noise (e.g. 60Hz)
  - Option 2: Special trigger forces readout of all channels using different mode
    - Uses different algorithm on FPGA
    - Average pedestal subtracted