12GeV Trigger meeting notes:

27 May 2011: C. Cuevas, H. Dong,S. Kaneta, J. Gu, B. Raydo, B. Moffit, A. Somov,

20 May 2011: C. Cuevas, S. Kaneta, J. Gu, B. Raydo, J. Wilson, B. Moffit, N. Nganga, E. Jastrzembski

13 May 2011: C. Cuevas, N. Nganga, S. Kaneta, J. Gu, A. Somov, B. Raydo, J. Wilson, B. Moffit

6 May 2011: C. Cuevas, N. Nganga, S. Kaneta, J. Gu, A. Somov, B. Raydo; H. Dong

22 April 2011: C. Cuevas, N. Nganga, B. Moffit, S. Kaneta, J. Gu, A. Somov, J. Wilson, E. Jastrzembski

15 April 2011: C. Cuevas, B. Raydo, N. Nganga,. B. Moffit, S. Kaneta, J. Gu; A. Somov, J. Wilson

1 April 2011: C. Cuevas, B. Raydo, N. Nganga,. E. Jastrzembski, B. Moffit, H. Dong,S. Kaneta, J. Gu; A. Somov, J. Wilson

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0. Trigger/Clock/Sync – TI/TD

27May2011

→The circuit board order for the pre-production units has been awarded. The components are on site and once the bare boards have been received and verified, they will be sent to the assembly vendor. Presumably all the front panels have been completed for the pre-production quantity.

→The TI can be tested with the existing FADC250-V2 to measure and record the maximum sustainable trigger rate in conjunction with the front end BUSY signal to verify the proper operation of the TI under maximum specified conditions. Multiple signals can be applied to the two FADC250 units to produce front-end data for readout.

20 May 2011

→Pre-production parts have been received. Assembly quotes ready. Final Gerber check in process.

→William presented summary of TS meeting that was held on Monday 16-May. File is located on the trigger wiki page.

13 May 2011

→Pre-production parts on order, fabrication files ready, PR can be started and after initial test of multiple FADC250 the order will be placed.

→Both TI boards have been configured in the EEL109 test setup for a few weeks. Not sure if these units have been run continuously for a full shift to verify that the values of counters in both units for trigger, clock, etc match perfectly. Trigger signals through the fiber distribution to each crate have been deskewed.

6 May 2011

Two FADC250V2 boards are installed in one crate. Some issues with token passing in block transfer mode. Need to check this early next week. What is the token passing sequence? i.e. TI always initiates the token in block mode?

22 April 2011

--> Two crates are configured in the EEL109 lab and William and Bryan have completed the procedure to remove the fiber optic cable delay(skew) between the crates. The two trigger signals were captured on the O'scope and at some point soon, it would be a good idea to go

through the zero delay adjustment procedure again, so that others can become familiar with the setup.
-->See SD section for additional discussion, and also notes in the 'customer' section for the status of the FADC250-V2 units that will be installed into these two EEL109 crates.

15 April 2011
→The 2nd VXS crate will be installed next week (Monday) and the 2nd TI, CPU and SD can be installed and configured. We will use the 50m fiber through the patch panels and prepare for the initial FADC250 unit. This will be a perfect opportunity to execute the setup procedure for removing the 'skew' from the different TI fiber lengths.
→No change to the initial single crate setup, and configuring (adding) another ROC should not take too long.

1 April 2011
A TID and SD have been installed the EEL109 VXS DAq crate. A 150m fiber has been connected from TI-port 5 to TI-port 1 through the patch panel and fiber patch cords. The number of tests that can be performed with these two boards is not too large, and a payload test board can be used to monitor clocks and other signals that are driven by the SD board. The status of the firmware for the TI and SD is complete for now, and Bryan can continue testing the library functions for each of these boards.

2. *SUB-SYSTEM PROCESSOR (SSP)*

27 May 2011
Ben and Hai have installed and initially tested the firmware used in both the CTP and SSP for serial transport of trigger information. Ben showed a ChipScope plot of signal received from a single CTP which was the sum of two channels, one signal into each FADC250. It is a perfect opportunity to measure and record the serial transport time for each of the modules in the system. This transport time will be fixed for each "link" (i.e. FADC250 to CTP and CTP to SSP) but needs to be measured and recorded.

20 May 2011
→New communication link from the CTP to the SSP has been discussed and implementation plan is in the works. It will be important to measure and record the propagation through the SSP. Two CTP will be implemented with Ben's firmware, and then the CTP->SSP link will be tested. SSP VME control/configuration registers will be defined soon and the command map will be distributed. Diagnostic 'history FiFo' can be implemented later.

13 May 2011
→ Ben and Hai have discussed the link definition that will be used for the two crate test. Ultimately, the SSP will collect the summing information from both CTP and generate a trigger signal that will drive the TI running in TS mode. There will not be a need for complex functions on the SSP, but a few registers will be needed to monitor the trigger output rate, and set the final threshold for the two crate sum.
→ECO list will need to be applied to the schematic and board layout as time permits.

6 May 2011
CTP → SSP link is the next work. Discussions have started. ECO list is documented but not implemented in schematic or pcb. We may want to purchase high cost components this fiscal year for the production quantity if funds are available.

22 April 2011
No report from Ben, but it was suggested that a sub-group should meet and discuss the initial implementation plan for using the SSP with the two CTP that will ultimately be used to generate the readout trigger signal to the TI(TS) module. The implementation will have limited programmability and will effectively combine the trigger information from the two CTP. There will be significant firmware work to implement this by the time we have two crates of FADC250, so now is the time to discuss the details.

15 April 2011
→Ben will complete a register map for the SSP that is specific to this two crate test. Bryan will have to build a driver for the SSP, and clearly it will not be the final revision. The SSP will be used to collect the summing information from the two crates and provide the final trigger signal to the TI that is running in TS mode.
→Ben and Hai have not finalized the transmission scheme for the CTP to SSP link, and next week will hopefully be a good opportunity to review this topic and begin the firmware effort.
→Ben will order a few MTP fiber optic jumpers and we should include fiber links from the CTPs to the SSP.

1 April 2011
Ben reported that he is at the stage of reviewing the details of the transmission protocol/scheme for the link between the CTP and the SSP. 4 bonded Aurora lanes @2.5Gp/s was the method used in 2009, and this will have to be reviewed. Hai will be ready to work with Ben on the CTP->SSP link firmware after work for the FADC250 is running flawlessly.

3. CUSTOMERS

27 May 2011
→An issue with the preproduction bare boards has been discovered and this will impact the delivery schedule of the remaining 33 assemblies. The bare boards will be sent to the board manufacturing company for test verification. Stay tuned,,,

13 May 2011
→There is another small order of 4 FADC250-V2 for the Radiation Detector Group and the Injector Group. This assembly order will be released in a week as soon as the bare boards have been received for the pre-production order.
→There are several groups that will need to begin testing detectors soon, and they will need crates, FADC250, SD, and TI. The need to order TI and SD will be urgent in a few months.

22 April 2011
-->Bryan has at least one of the FADC250-V2 boards with the latest 'Hall D' firmware revision and Ed has provided an update to the register map document so the iterations to the CODA software libraries can be completed.
-->During the week of 25-April, at least one FADC250-V2 module should be running in the EEL109 two crate test station, and hopefully we can proceed with the second unit as soon as the Detector Group returns the module.

15 April 2011
→Even though Ed and Hai were not present, they demonstrated on Thursday, a fully functional FADC250-V2 running with the latest firmware and with a CTP. Only one channel was used to create a 'sum' and the rate of the trigger was over 1 KHz. The plan is to move this board to the EEL109 lab and begin checkout with the other boards. Ed will update the register map document and Bryan can begin the modifications to the driver.
→Once the 2nd crate is configured we will need the FADC250-V2 that was loaned to the Detector group.

1 April 2011 (Not an April Fools)

Ed reports that the FADC250 board has been tested and that the data format and other firmware features are working. Hopefully we can use at least one of the version 2 boards for initial testing with the SD, TI and CTP in the EEL109 DAq crate. The FADC250-V2 that was loaned to the Radiation Detector and Imaging group should be returned and loaded with the latest firmware so that we can begin populating the 2nd DAq crate.

4 "B" Switch - Signal Distribution Module (SD)

27 May 2011

→Nick is at another meeting and will need to implement ALL Engineering Changes to the schematic and PCB and prepare for a pre-production order. The test stand group will need the 2nd SD during the week of June 1 to complete a two crate test with a single FADC250-V2 in each crate.

→Complete diagrams and documentation for the phase adjustment technique that was successfully implemented using the Altera Nios and carry chain logic.

20 May 2011

→Token passing is OK!

→Diagrams for the phase adjustment technique will be produced. Successful implementation

→Turn-Key Production order discussion.

13 May 2011

→Nick has successfully implemented the phase adjustment technique on one of the SD. ~100ps is the resolution for measuring the phase difference using a dedicated carry chain circuit on the Altera FPGA. The full loop control has been tested through SPI to the SiliconLab PLL.

→Only one SD board has been modified and only one needs this change at the present time.

→ECOs must be completed in the schematic and circuit board as soon as possible and the parts kit for ordering six more SD assemblies is virtually complete.

6 May 2011

Phase adjustment technique with Altera FPGA. Any progress?

Carry chain technique to measure phase difference and feed correction through SPI interface to the PLL chips.

We have a plan to use the Silicon Lab board and the old TI prototype to implement a test of the new phase compensation technique. Done by Wed 11-May-2011. B. Raydo will assist.

22 April 2011

-->Nick presented a few oscilloscope photos that showed the clock signals in relation to one another from both crates. There was a good discussion on why the second scope trace exhibited a somewhat significant jitter with relation to the first. Nick also showed a long term, (>8hr) photo from the O'scope that had acquired signals in infinite persistence mode. The two signals did not appear to have any significant variation which shows that the clock signals are definitely phased locked and show no clock cycle drift.

-->Nick mentioned that the SD parts kit is close to final and that the front panels were ready for machining. The files for manufacturing the final pre-production boards are virtually complete and pending final review and performance results from the two crate test.

15 April 2011

The 2nd SD will be needed for when we install the second crate. We do not have a spare SD so any changes to firmware that may be required will have to be kept at a minimum. Nick reports

that the front panels for six more boards have been ordered, and that Mark will finalize the parts kit to build six more SD as soon as all testing is complete, and ECOs are verified.

1 April 2011
For the time without a FADC250-V2 board, we can use the payload test board to send a trigger signal to the SD and pass this signal to the TI. Nick has been busy with final firmware changes and has also started to implement the ECOs for the final board design. The components for six SD boards have been received and assembly of the parts kit has started. Soon after the two crate DAq testing, we can send the order for a six board assemblies. The front panel drawings should be checked and ordered now.

5. System Diagrams & Test Stand Activities

27 May 2011
There have been good discussions with Sergey et al from CLAS12 to work on displays and other GUI for configuration and control of the plethora of functions from the trigger modules. The CLAS12 folks would certainly like to get started with their detector DAq testing and as soon as we have completely verified the FADC250 assemblies, and tested them in a full crate, groups can begin their detector tests.

20 May 2011
GUI and displays for graphing results from test stand modules. How are we going to implement this, what values need to be displayed? What scaler items need to be implemented?

Global SUM plot—Read from SSP (Could read CTP1 and CTP2 from SSP also)
Crate SUM plot – Read from CTP (Via I^2C)
Scalers: A strong comment from Bryan Moffit: Put the scalers in registers, NOT data stream. Must create a list of scaler registers to implement in the hardware.

Event counters
Trigger counters
Clock counters
Readout rate Vs trigger rate
Channel bar graphs
Any channel 'Scope shot'

13 May 2011
→No report on fiber specification draft document.
→16 more VXS crates arrived and will need preliminary checkout soon.
→EEL109 two crate test station has new Wiener VXS crates installed!

6 May 2011
No report.

22 April 2011
→No significant update on the draft fiber specification for the trigger signal distribution for the halls. The specification will need to be completed before the end of May to establish a pre-procurement plan for fiber purchase/assembly/installation and testing.

15 April 2011
→The trigger system fiber optic specification will be created and sent for comments soon. It is not clear when these fiber trunk cables and patch panels will be installed in the hall. Finishing the specification and installation requirement document makes sense to complete now, and at

least when the procurement begins, the items will only need to be ordered. Fortunately, there are several commercial sources for the fiber and patch panel equipment.

1-April 2011
Start a pre procurement plan for Hall D to include fiber trunk installation and testing. Patch cables and patch panels will be ordered separately.

5. Two Crate DAq test configuration

27 May 2011
We have three FADC250-V2 boards that are working and will proceed to configure the two crate test stand with one FADC250-V2 per crate. Will need the 2nd SD board and will also use the SSP to collect trigger data from each crate trigger processor. We will measure and record the trigger transition delays (Should be fixed and is a function of the Aurora serial protocol) from each serial link.

13 May 2011

Four FADC250-V2 boards are in the EEL109 lab!! Two of the boards were received 12-May-2011 and will need to be tested with Hai's automatic test routine.

Next Steps:
Install two FADC250-V2 in one crate
"Hardcode" payload ports to CTP
Troubleshoot token passing problem
Set 'Sum' threshold to CTP
Use CTP output to TI(TS) to create final trigger
Then;
Install two boards in each crate
Use hardcoded CTP in each crate
Use two CTP outputs to drive two TI(TS) inputs to create final trigger
Initial test complete
→Need to create simple 'event' displays to view important values during test procedures

6 May 2011
We should have three or four FADC250V2 boards in the EEL by 13-May-2011. Two crate testing will begin next week with one flash board in each crate.
Good progress by Bryan et al.

22 April 2011
-->Ed and Hai have completed the final firmware revisions for the initial FADC250-V2 boards and at least one unit should be installed in the EEL109 lab for an initial test with the TI and SD module. Continued progress, and it will not be long before we have two full front end crates!
-->The main goals of the two crate test are extracted from past meetings as follows:
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of:
-Readout rates
-Trigger rates, and a variety of other information needed to claim success.
The list of verification requirements are listed below:
→Goals of the integration testing:
-Verify clock distribution through TID->SD and measure jitter to front end boards

-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

15 April 2011

→See 1st section, but the good news is that the FADC250-V2 is ready to be installed in the 1st VXS crate. Achieved the new deadline, and we will configure a 20 slot VXS crate that has an ELMA backplane for now. There will be a slight delay for the delivery of sixteen more VXS crates, but we can use the ELMA crate to continue progress with the testing.

1 April 2011

TI-D, SD, Linux ROC, are **installed in the EEL109 lab!!** 150m fiber with patch panels installed also. We will need a FADC250-V2 as soon as possible**!** At least one FADC250-V2 will be ready by 15-April!
The clock phase alignment procedure has been completed by William, and the adjustment for clock phase alignment between front end crates is one 4ns clock cycle.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)

So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

   The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

   Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to

the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. ***Crate Trigger Processor (CTP)***

27 May 2011
See SSP notes

20 May 2011
Two FADC250V2 have been tested in one crate with a CTP @2.5Gb/s with signals from the front end of the FADC250V2. We are 1/16th of the way there!!! Original version of the CTP is used in this test.

2nd crate will use 2nd original version of the CTP.

→Hai has successfully tested the latest version of the FADC250 boards with the CTP. Presently the CTP is 'hardcoded' to accept serial trigger data from pre-determined payload slots. Not sure how much work it will take to implement a register that will enable/disable a serial stream from a particular payload slot. For the immediate future, the payload serial streams to the CTP will be 'hardcoded'.
→We have 4 CTP units and I am not sure which ones have been exercised with the latest version of the FADC250. The two CTP with the V5FX70T devices will be tested at the higher serial transfer rate (5Gb/s) but this test is not the highest priority and will be delayed.

13 May 2011
Ben has firmware that was developed during testing of the SSP. Re-use code

6 May 2011
Testing has started with the FADC250V2 boards and the CTP. Initial serial transceiver testing will use 2.5Gb/s per lane.

22 April 2011
-->As stated in a previous section, the plan is to use the latest CTP in the two crate test and verify full functionality with two lanes at 2.5Gb/s from each payload slot. We *should* use the CTP that have the Virtex V FX70T FPGA and increase the serial lane transmission AFTER the initial testing is complete.
-->Details of the CTP to SSP data transfer technique will have to be settled sooner than later, so plan on meeting a few times for informal discussions on the best way to implement these techniques in firmware/software.

15 April 2011
→No report but Hai will meet with Ben to arrange a method to transfer the summing information to the SSP. I believe all four CTP are working, but it is not clear which units have the latest firmware. It would be best to use the CTP that have the 'FX70T components, but this is not absolutely required. Will check with Hai next week for the latest status.

1 April 2011
→CTP 1 and 2 will be used *initially* in the two crate test. These units use LX110T and will have the transceiver selection *hardcoded* in the FPGA for a single FADC250.
→For the **final** two crate configuration with 16 payloads we will use CTP 3 & 4 that are assembled with the FX70T part. We will need to have the CTP firmware developed so that each of the Gigabit transceivers can be disabled or enabled. If there are counters (scalers) that need to be added, these must be defined now.

→The ECO list for the CTP design is well known, and will need time to implement on the schematics and PCB. These changes include adding front panel I/O and other small circuit corrections. These ECO are in the plan and create a good deal of work to complete before the end of fy11.

7. GTP and Global Crate Developments

27 May 2011

→Fabrication files ready to be checked thoroughly and quotes for bare board and assembly have been received. Is the BOM final and do we have all components kitted in the lab? We will need to have another group contribute funds for the prototype, and this is a work in progress. The order for the boards and assembly should pass through procurement without issues, considering Scott has received estimates from several sources.

→Firmware development: Several complex sections:
-Ethernet interface
-SSP serial streams
-Global logic
-Nios implementation
-Functional hardware test is the first plan

20 May 2011

→RFP for circuit board fab and assembly.
→Review schematic: DRC
→Review Gerbers
Large polygons and large smd pads. Do manufactures require thermal relief?
→Parts kits have been prepared and ordered.
→Who's going to pay for the prototype fab cost?

13 May 2011

→Scott is reviewing the component purchase requisitions and the board has been fully routed. Post routing verification is presently underway and it is time to obtain a price quote for at least two bare boards.
→There has been some discussion regarding the Densi-shield connectors and also the timing skews between the output trigger bits. Presently, the GTP drives the 32 trigger output bits from the Altera FPGA via LVDS. These LVDS signals are buffered and drive the Densi-shield connector with pECL level signaling to be received by the TS. These outputs from the GTP will not be 'registered' before being driven to the TS, and the TS will be responsible for latching and deskewing (if required) the 32 trigger bits.
→Final check of fabrication files will happen soon, so that we can order the boards in a few weeks. One board will be partially assembled for full DC power verification and then a full assembly will be produced.

6 May 2011

16 layer routing is 90% complete. DDR2 memories are the last section being routed and pin swapped. Progress coming along nicely. Need to order parts ASAP and prepare board manufacturing procurements including assembly/solder requisition.
Review schedule and update order date(Milestone)

22 April 2011

-->Scott continues with the final stages of routing the external DDR memory and is quickly learning how to use the Cadence routing tools. The GTP is at the stage of final routing and verification of the fabrication files will soon be needed.

-->The final Bill of Materials is also a work in progress and only a small fraction of the components have been purchased and delivered. The longer lead items and expensive items have been received. Very soon, we should consider starting the parts "kit" for the initial prototype build.
-->Time to revisit the schedule and update any changes that will be needed for firmware development and simulation. There will be a significant development period to implement the Ethernet interface and other required features.

15 April 2011
→Scott reports that the routing stage is nearly complete and once the external DDR memory chips and configuration devices are routed, he will verify the BOM and initiate an order for parts.
→Firmware development will begin soon and will be a significant effort considering the board functions and specifications. Considerations for hardware (full functional) test methods will also require development time.

1 April 2011
Scott presented the latest update on the board layout and the routing for the transceiver lanes look very impressive and on one layer and manage sixteen SSP with 2 full duplex lanes! The board routing paths for the memories, and Ethernet interface is a work in progress. The Specctra router routines will need to be developed but the progress is very promising. Ethernet firmware and Nios embedded code will begin when board sent for assembly. Initial code framework has been developed.

ACTION ITEMS: **Next meeting → Friday 3 June at 10AM in F226**