12GeV Trigger meeting notes:

4 March 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov

18 & 25 Feb 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov

11 Feb 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu

14 & 21 Jan 2011: C. Cuevas, A. Somov, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta

Updated prototype board status table:--2 March 2011

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250** SN001 >>>>>>>>> SN002 >>>>>>>>> SN003 >>>>>>>>> SN004 >>>>>>>>> SN005 >>>>>>>>> SN006 >>>>>>>>> SN007 >>>>>>>>> SN008 >>>>>>>>>	 F110 Injector Group Injector Group EEL – 126 Hai's office F-Wing Lab Hall A EEL – 126	 DAQ Lab J. Grames J. Grames FDC test setup Needs repair F117 (A. Somov) Moller setup FDC test setup
1	12bit FADC250	Indiana Univ	New timing algorithm firmware loaded Sent to IU for FCAL testing 12Oct2009 '64x crate and LinuX Cpu sent 24Jan10
4	Crate Trigger Processor	F-Wing F110 EEL109 EEL109 EEL109	Initial prototype CODA Library development Initial prototype - EEL109 Tested with SSP Received from CEM. Needs testing
1	Sub-System Processor	EEL109	Successful testing with CTP. SODIMM testing to be completed.
4	Signal Distribution V1 V1 V2 V2	F-Wing F110 EEL 109 EEL 109 EEL 109	CODA Library development Testing with initial TI prototype Assembled. TESTING Continues Assembled. TESTING Continues

0. Trigger/Clock/Sync – TI/TD

4 March 2011

A brief discussion on radiation affects on the Avago transceivers was opened by Chris and there are several articles from LHC groups that cover not only the electro-optics, but the fiber degradation from radiation dose. Fortunately there will not be high enough radiation dose in Halls D & B, and the equipment racks will be a decent distance from the Tagger and Target areas. At any rate, if someone would like to research this topic further we can discuss this again and possibly set up a test in Hall C or Hall A. Avago does not have radiation affect data for their fiber optic transceiver product.

William brought up the point about the CLKA and CLKB signals that the TI-D will distribute to the SD. The present design revision does not allow any of the three clock choices to be distributed to either CLKA or CLKB. The SD provides fan-out of CLKA to the "odd" payload

ports (Left) and CLKB to the "even" payload ports (Right). The final TI-D requirement is to send any of the three clocks (250MHz, 125MHz, and 31.25MHz) to both CLKA and CLKB. (D. Abbott)

February 2011

William presented a diagram that shows the configuration for the TI-D boards that will be used in the upcoming two crate DAq testing. One module will be operated as the TS for the two crate test. This module will use one transceiver to effectively loop back to another transceiver on this module. 50m of the MTP fiber will be used for crate #1. The second crate will have a TI-D module operated strictly in TI mode and we will plan to used the 150m MTP fiber for crate #2. We will plan to use the patch panels in this test to fully simulate a typical installation in the halls.

Nick presented jitter analysis results that showed the function of the jitter attenuation PLL circuit. The baseline resolution of the DSA70000 is about 1ps, and one of the tests that were performed used the RF generator that has a specified baseline jitter of 500fs. Using the RF source and a single high speed line driver, a baseline jitter measurement was established. Long story short, is that when the PLL is enabled the clock jitter measured at the farthest Payload port (15) is better than the source. (TI slot).

Nick has completed the changes to the 'receiving' I^2C firmware and has tested it with William's new TI-D. Nick is almost finished with the firmware that controls the SPI bus from the SD Fpga to the SiLab PLL components. All other firmware for Token Passing, BUSY Or'ing and other selections is complete and will need to be tested with a few payload boards.

Engineering changes to both the SD_Rev1 and The TI-D can begin and William reports that he has started the changes on the TI-D. PLL verification testing is the highest priority, and once that is complete, the changes to the board can be completed.

William distributed a test report for the TI-D jitter and fiber optic latency testing. We will begin to set up the two crate Daq/Trigger test stand in EEL-109 soon, so repeating the latency measurements for a 50m and 150m fiber including patch panels and patch cables can be completed before March.

January 2011

→William has completed the TI-D I^2C firmware and has distributed the specifications. Nick will modify the 'Receiving" side of the I^2C firmware so that it is compatible with William's changes. William also distributed the test results for the clock distribution jitter and the results are very good with a jitter histogram measured with the Tektronix scope at <2ps!
→Nick was successful in testing the SD board with the original TI board and established I^2C communications to the board before the holidays. There have been several modifications to the SD board, and once the I^2C firmware is fully tested and stable, Nick can proceed to measure the clock jitter with and without the PLL in the distribution chain. All other I/O will also be tested soon after.
→Schedule: The plan is still on track to prepare the TI-D files for production order before the summer. We will use the existing TI-D prototype boards for the two crate tests, but ECO modifications can begin for the schematic and board layout activities.

2. *SUB-SYSTEM PROCESSOR (SSP)*

4 March 2011

Ben reports that the testing of the SSP is complete and that he will spend some time on the firmware required for the SSP in the two crate DAq setup. The SSP is planned to be used to collect the trigger data from two CTP and combine this trigger information and create the L1 trigger signal that will be sent to the TI-D. At some point soon, the CODA 'driver' library for the

SSP will have to be created, so whenever the firmware is at a stable revision, Bryan can start the library development.

February 2011
Ben reported that the SODIMM testing was progressing and he has run the memory module at 200MHz. Ben also presented jitter analysis and eye diagrams for the SSP backplane Gigabit transceivers that have been tested with a CTP. Initial test results are impressive and a series of parameters have been adjusted for the Xilinx transceivers to optimize the performance of the transceivers at 2.5Gb/s and at 5Gb/s. The eye diagrams and BitErrorRate (BER) testing at 2.5Gb/s are significantly better that the initial testing at 5Gb/s. Longer periods of testing will be needed to establish a BER lower than 10^-15.

11 February 2011
The SSP documentation has been updated to include a new application (solution) for interfacing up to 32 front-end readout devices from detectors that use custom ICs developed for high density central tracking apparatus. Each of the 32 Tx/Rx links can be run at 3.125 Gbps, and provides an elegant consolidated and isolated method to readout and control the high channel count custom ICs.

SODIMM memory testing to be completed.

3. CUSTOMERS

4 March 2011
I will keep this section to list a brief status of the FADC250 boards, and Ed reports that testing with the version 2 pre-production unit is going well and that 2eSST readout is imminent. The order for 35 boards/assembly is ready to proceed.

January 2011
→Not a specific trigger module topic here, but preparation for the pre-production order for the FADC250 boards is virtually complete. The Medical Imaging group and Injector group will purchase two boards each, in addition to the 35 pre-production units.
→Small pre-production builds for the TI-D and SD boards make sense because there are several Users/Groups that will need to begin testing detectors soon after the two crate testing has been completed.

4 "B" Switch - Signal Distribution Module (SD)

4 March 2011
Nick presented a block diagram of the test setup used to perform the clock distribution jitter analysis. He showed how the use of an external receiver/buffer circuit allowed a precise baseline measurement of the test equipment. The 250MHz clock was distributed from the TI-D to the SD and the clock signal was measured at PayloadPort-15. The jitter was measured with and without the SD jitter attenuation PLL circuit and the results showed that the PLL circuit worked as designed. The baseline jitter 'calibration' was a very good method and demonstrated that the PLL jitter contribution is negligible.

18 February 2011
Jitter analysis results were presented by Nick and the jitter attenuation from the PLL on the SD definitely has a positive effect on the distribution of the clock signal received from the TI. The SPI communication is working and has been mapped internally to the SD FPGA.

The final firmware for the I^2C 'receiver' has been tested and this block of firmware will need to be implemented in each of the four CTP modules. This firmware change should work seamlessly with Bryan's library.

11 February 2011

→The new I^2C firmware that Nick completed can be given to Scott for inclusion in the CTPs. SPI control is a work in progress with a breakthrough soon. Preliminary jitter and clock distribution measurements are forthcoming.

→Engineering changes for the final SD revision can be worked on by Mark when he returns full time. For now, we have the components for at least six more SD, so we should be in good shape to make the last changes and order a pre-production lot.

5. System Diagrams & Test Stand Activities

4 March 2011

A brief discussion on the collection of hardware that has been assembled in EEL109 for the two crate DAq test. In the next week or two it would be an important goal to setup a single crate with a CPU, TI-D, CTP, SD and a single FADC250. There are numerous details to verify a 'simple' configuration of these essential modules.

The price estimates for the trigger system fiber optic cabling, patch panel hardware and installation is due this week from the initial vendor. There are quite a few details to discuss before installation in the hall.

25 February 2011

Bryan reported that the 1U rack mount LinuX PC has been installed in the EEL109. This unit has plenty of speed to manage the two crate test. Will the disk speed be capable of streaming the data from two crates? (I remember this was a question from Ben)

No budgetary pricing received from fiber optic company yet. A representative from a local installation company was here a few weeks ago to get an idea of the installation project scope. Pricing estimates are due soon!

11 February 2011

We had a significant discussion about the two crate Daq/Trigger testing that will happen in a few more months once the pre-production lot of FADC250 arrive. In the meantime, we have a virtually all the other hardware needed for this test. See below:

Description	Quantity	Firmware Rev	Model#	Notes
VXS Crate	2	n/a	Wiener	EEL-109/Chris
Single Board CPU	2	Linux ?	?	Bryan/Dave?
CTP	2	?	Use latest version	Hai/Scott
SD	2	?	Use Rev1 boards	Nick
TI-D	2	?	1-TI 1-TI-D	William
SSP	1	?	Prototype	Ben
Fiber	2 -50m & 150m	n/a		EEL-109
Fiber patch	1	n/a		EEL-109
Fiber patch cables	4	n/a		EEL-109

For the DAQ/CODA software side:

Description	Quantity	Revision	Model#	Notes
GigEthernet Switch	1 multi port			EEL-109
Linux PC	1	Dell 1U	FAST	Installed by

				Bryan in EEL109
CODA				Bryan/Dave
CODA board libraries				Bryan/Dave

We have test equipment, pulsers, fanout modules etc so that should not be an issue.
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of readout rates, trigger rates, and a variety of other information needed to claim success.
The list of verification requirements (goals) are listed below:
→**Goals of the integration testing**:
-Verify clock distribution through TID-SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

   The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

   Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within

the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

4 March 2011

The two newer CTP units have been received from the rework vendor, and the repairs appear to be OK. At least two of the four CTP units will have to be loaded with the final firmware revision soon which includes the latest I^2C block from Nick. Need to push this to a higher priority soon.

25-February 2011

→The two latest CTP boards have been reworked by CEM and received. One has been used with an SSP @5Gb/s. Ben shows nice plots with BER testing between SSP in PPort15 and CTP. Plots shown for transmission @5Gb/s and various receiver attribute settings.
→Scott will continue testing both of the latest units and at some point soon, all four of the CTP should be loaded with the latest firmware in preparation for the two crate DAq testing.

11-February 2011

Scott has identified a few problems with each of the new CTP and these have been sent back to CEM for part replacement. Once they return from CEM, Scott can continue his testing and prepare these units for the two crate tests.

7. Projects for FY11 (GTP and Global Crate Developments)

4 March 2011

Scott, Nick, Ben, Hai and Chris met after the trigger meeting to review the latest GTP schematic. This 'review' was helpful and no show stoppers were identified. There were several important details that were noted, and Scott captured the changes that need to be added. Board layout should begin as soon as possible.

25 Feb 2011

Scott explains the latest progress on the CTP and we will review the schematics, global pair map and other details soon. The GTP will use an interswitch pair for clock to take advantage of the beautiful clock signal from the SD jitter attenuating PLL. The Schematic is virtually complete, and the power distribution/analysis is almost done. The Densishield cables have been received and the Altera FPGA has been ordered.

11-February 2011

Scott continues to make progress on the schematic and will be prepared to have a review before he begins the significant work of board layout. Scott has been pre-planning the FPGA resource layout so that the routing on the board should be reasonable. The power distribution section of the design is under careful analysis also.

ACTION ITEMS: **Next meeting → Friday 11 March 2011 11AM in F226**