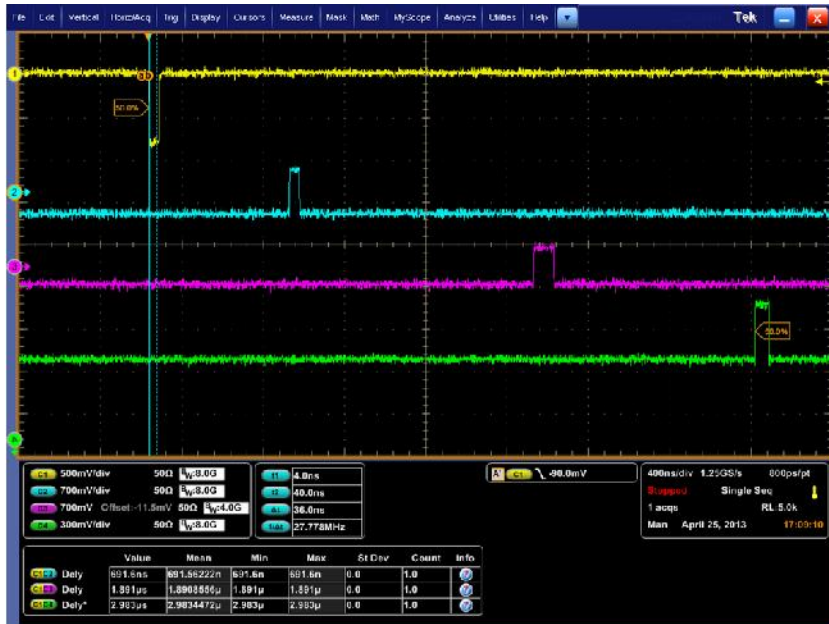


Front End System Test



- Yellow
 - Fanout board output
- Magenta
 - Probe on ADC data bus
 - See cursors (~37ns)
- Cyan
 - CTP Trigger Out

Complete Trigger Path



- Yellow
 - Fanout board output
- Blue
 - CTP Trigger Out
- Magenta
 - SSP Trigger Out
- Green
 - Front end SD Trig1 Out

Trigger Path Measurements

Sync to Data

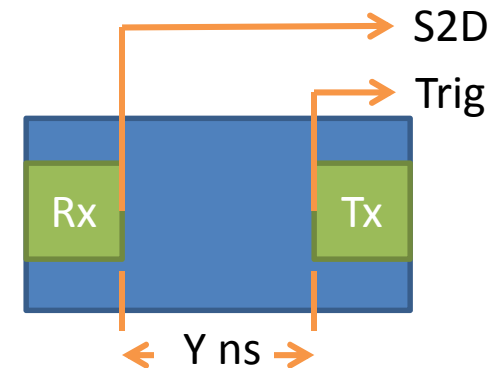
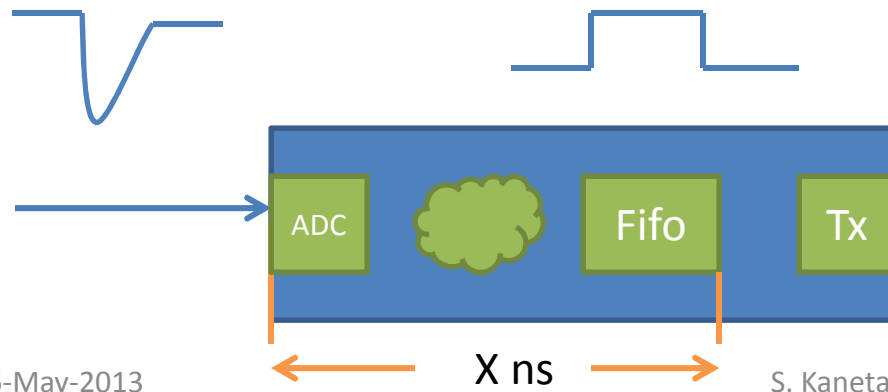
- 0ns – Sync released
 - 432ns – Data at CTP
 - 1.628us – Data at SSP
 - ~750 ns fiber delay (150m)
 - 1.760us – Data at GTP
- Sync to Data shows the time from sync release to data appearing at the deserializer output of each module
 - Processing is included
 - Calculated by each module and reported by register

Trigger Path Measurements

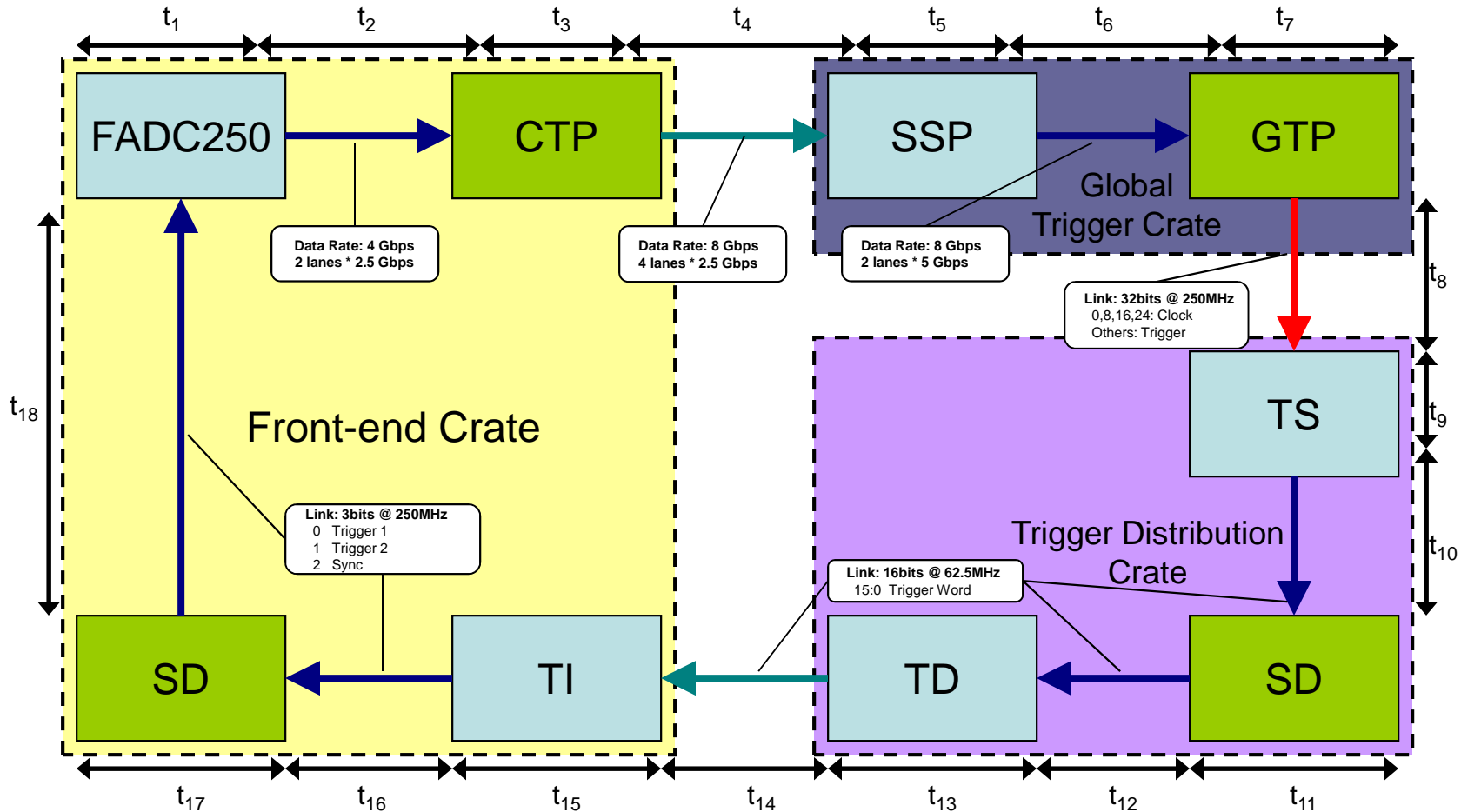
Pulse into FADC

- 0ns – Fanout board out
- 686ns – CTP Trigger Out
- 1.89us – SSP Trigger Out
- 2.035us – GTP Trigger Out
- 2.954us – FE SD Trig 1 Out

- This measures the actual trigger latencies
- Trigger Out - Sync to Data
 - $X + Y = \sim 260\text{ns}$
 - Includes
 - ADC to Fifo
 - A/D conversion $\sim 37\text{ns}$
 - Module processing
 - Varies by module ($\pm 10\text{ns}$)



Measured D Level 1 Trigger Timing Fill in the ?



t_0 : Fanout		0 ns	0 ns
t_1 : FADC250	(ADC->Tx)		?
t_2 : FADC250->CTP	(SERDES + VXS)		
t_3 : CTP	(Rx->Tx)		686 ns
t_4 : CTP->SSP	(SERDES + Fiber)		
t_5 : SSP	(FiberRx->Tx)		1.89 us
t_6 : SSP->GTP	(SERDES + VXS)		
t_7 : GTP	(Rx->TrigBit)		
t_8 : GTP->TS	(Densishield)		2.035 us
t_9 : TS	(TriggerBitIn->Tx)		?
t_{10} : TS->SD	(Serializer)		

t_{11} : SD	(Px->Px)	Passive?
t_{12} : SD->TD	(Px->P0)	
t_{13} : TD	(P0->FiberTx)	Passive?
t_{14} : TD->TI	(Deserializer)	
t_{15} : TI	(FiberRx->P0)	?
t_{16} : TI->SD	(P0->Px)	
t_{17} : SD	(Px->Px)	2.954 us
t_{18} : SD->FADC250	(Px->P0)	
$t_{19}(?)$: FADC Buffer Processing		

6-May-2013

S. Kaneta



Total: