Trigger meeting notes:

20 Feb 09: C. Cuevas, A. Gupta, H. Dong, B. Raydo, J. Wilson, M. Taylor; A. Somov

No meeting 13Feb or 6 Feb09:

30 Jan 09: C. Cuevas, A. Gupta, H. Dong, E. Jastrzembski, B. Raydo, J. Wilson, M. Taylor

Updated prototype board status table:--20 February 2009

Quantity	Description	Location	STATUS
5	10bit FADC250	EEL109/DAQ Lab	Trigger testing
1	10bit FADC250	ORNL – D. Curry	SN#003 Evaluation
1	10bit FADC250	Hall A Experiment	1st board in Experiment!
1	10bit FADC250	EEL109	In Repair
1	12bit FADC250	Indiana University	FCAL testing
4	Trigger Interface Trigger Distribution	EEL109/DAQ Lab	Trigger testing
5	VME -- FP-SD Front Panel – Signal Distribution	EEL109/DAQ Lab	Complete Use in test crates
1	Crate Trigger Processor	EEL 109	Initial functional testing
1	Crate Trigger Processor	Send for assembly as soon as parts received	Send 9 Feb 2009
2	Signal Distribution	Receive from board house on 21 Jan	Boards back to assembler for repair Should receive by 27Feb09

0. Trigger/Clock/Sync – TI/TD

20 Feb 2009

Sebouh has successfully tested his firmware and GUI with the Wiener USB-VME controller, Trigger Interface and CTP! He will provide a document for the test results and this completes the CTP portion of his work. The I^2C code work will be used also for the SD, and once the SD is tested he will work with Abhishek to control the SD functions.

30 Jan 2008

Sebouh will move his application to the EEL109 lab and test his firmware and GUI for the I^2C read/write functions to the CTP and SD. He is using MSVisual Studio for the GUI and is preparing the lab PC with the proper files, etc for testing his application. He will use the Wiener USB-VME controller to execute VME commands to the Trigger Interface.

1. FIRMWARE TESTING

20 Feb 2009

D64 transfer mode has been de-bugged and the firmware has been updated in the flash modules. New firmware to support VME_SST transfer mode is close to completion and will be initially tested in the Daq lab before implementing the change to all boards in the test stand.

30 JAN 2009

Ben has identified a firmware bug when attempting 64bit bus transfers. Ed acknowledges the problem and troubleshooting has started on the TI and FADC250 modules.
→Work on the VME – SST firmware development and testing will take a higher priority after the 64 bit data transfer 'bug' is understood.

2. *Sub-System Processor (SSP)*

20 Feb 2009

Schematics are progressing at a glacier pace, but progress nonetheless. The components for the Virtex5 series parts that are planned for use are not part of the existing Altium libraries, so these parts will have to be created. Third party sources have the XCV5FX70T part, so that might be a good way to get started. An updated block diagram will be useful for discussion and the schematic work will continue.

30 JAN 2009

For the alert readers, this section has been changed to the SSP activity notes. Chris has transferred the Pcad files for the TI into the Altium "Unified" application and modification to the schematic sheets is a work in progress. The SSP is a VXS payload module, so it makes sense to re-use all of the board components and circuitry that will be used for the SSP. Ben has suggested new Virtex5 series components for the initial board, and I am certain several parts will have to be created with the Altium tools for the SSP design. We will have to revisit the proposed design for the global trigger crate and sort out the details as we continue the schematics.

3. CUSTOMERS

20 Feb 2009

1 Flash board has been installed in Hall A on the present experiment. 12 PMTs are used as the input signals and these channels are also monitored with the old fashioned method (gated 1881) for comparison. Hall Staff will have to use D. Abbott's code to decode the data, and the board is operated in raw data mode. (All samples within a window). May have preliminary results soon for presentation.

→Need to request the 12 bit board from the FCAL group so that we can perform a SNR test. It would be a good comparison to the 10 bit SNR test. We would need the 12bit board for only a few weeks.

→D. Curry at ORNL has a 10 bit board as an evaluation unit until May 1. He has successfully operated the board and will present the Jlab board as an inexpensive solution for a beam diagnostic upgrade application. My hopes are that their group can provide extra money for the next revision (pre-production quantities). Details will be presented soon.

30 JAN 2009

→Ben presented recent measurements of the FADC pulse sum mode, and SNR testing with a 10 bit module at the GlueX collaboration. I talked with Matt Sheppard from IU and he thought it was a good idea to run the SNR testing on the 12 bit FADC module so that we can measure and compare to the 10 bit version. The final version of the FADC250 module will include 12bit parts, so it will be a good test, and we should only need the 12 bit board for a few weeks.

→I have decided to loan a single FADC250 module to the instrumentation group at ORNL for a short period, so that they can run an evaluation/demonstration of the board. The ORNL group has significant upgrade projects for several beamline systems and one of their proposals is a very expensive COTS solution. Our FADC250 design may prove much more cost effective for their application, and since we are both DOE labs, it makes sense to share this type of design and possibly combine funding.

4 "B" Switch - Signal Distribution Module (SD)

20 Feb 2009

The SD boards were received from the assembler and visually inspected. The assembly company completed the job on time and the boards were cleaned very nicely and all looked good, except that 12 QFN packages were mounted on the board incorrectly.
What happened? The pin 1 reference designator was not on the silkscreen, and the pick and place data was not used, nor did the company contact us with any questions. The boards were sent back on Friday 20Feb, and we should receive them by 27Feb. The cost is minimal, but we lose another week.

The test procedure is in place for checking all of the DC voltages and then the initial FPGA code can be loaded and tested. Soon after, Abhishek can verify the clock signals to each of the payload slots. There are many tests to perform before loading the FPGA with the final code, but the test plan is in place.

30 JAN 2009

→The bare boards were tested and two voltage 'polygons' on the power planes will have to be connected together externally with jumper wires. There are zero power to ground connections and the boards have been sent to the assembly house in California along with all the components. Expected delivery should be the week of 9 Feb. Abhishek and Mark will begin DC testing and other initial measurements as soon as the boards are received.
→The front panel design is close to complete and will need to be sent for machining soon.
→Abhishek has completed the firmware that will be used to initially test the functions of the SD. Further firmware development and testing will be generated as required to test ALL functions of the SD in the 20 slot VXS crate.

23 JAN 2009

The three bare boards have been received and look fine. Abhishek and Mark will begin testing the bard board for any defects and send these boards with the parts to the assembler. Schedule to ship on 29Jan09 and we paid for a seven day delivery.

As soon as the assembled SD boards are received there are plenty of preliminary functional tests to perform and these test results will be documented on Abhishek's test plan. Soon after, the SD will be installed in the full 20 slot crate and critical testing of the signal fan-out will begin.

5. System Diagrams & Test Stand Activities

20 FEB 2009

Alex discussed the testing of these boards in the system, and asked about the capability to download 'data' to the front end FPGAs on the flash boards and then run the trigger system to verify that the trigger 'data' truly creates the trigger that was requested. For instance, one could program a certain trigger function for the BCAL, "data' would be loaded into the front end FPGA modules, and then the system should only respond if the trigger data propagated through the system without error. Sub-systems could be verified in this manner before an experiment started. The capability for download exists, and the details of this type of system level test will need to be discussed/documented further.

→Abstract has been submitted to the Real Time Conference. The emphasis of the paper is the two crate trigger test stand results with at least two flash boards per crate. The SD boards will be working soon, and the 2nd CTP will be ordered soon, and there is a great deal of work, but we should be able to present results for the paper/poster by May.

30 JAN 2009
Ben presented results at the GlueX collaboration meeting, and no other report was given at the Trigger meeting. Notes from previous meetings are included below, and there will be many more tests to perform when the CTP and SD are completely tested.

6. Crate Trigger Processor (CTP)

20 FEB 2009
→The 2nd CTP assembly PR has been signed and only one part needs to be received before the kit can be sent to the vendor. The front panel and heat sink material has been received for the 2nd unit, so it will not be long until we have two CTP modules.
→Hai presented heat sink results and the heat sink design will keep the temperature of the three large FPGA at the same temperature. The Virtex5 parts have a nice voltage and temperature monitoring feature, and Hai has used this to measure the die temperature with and without heat sink. Hai mentioned that Sebouh could add the monitoring feature to his I^2C function so that the monitoring features could be read out through the serial link.
→Data alignment testing and verification continues and Hai has been successful with at least two flash boards sending trigger data to the three FPGA devices. (The 16 payload boards are received into 3 FPGAs)
→Some discussions have started regarding the addition of an Ethernet network connection that would facilitate the firmware download to the CTP. Presently all communication to the CTP is through I^2C from the TI, then through VME. If a SBC is selected that has a VXS connection to the switch slots, it may be easy enough to wire these lanes, and then test a connection using the Ethernet protocol. Implementation of the all the Ethernet layers may not be necessary and it depends on how the SBC manages this connection. More details will emerge.

30 JAN 2009
→Successful CTP testing has been accomplished in the test crate with a single FADC250!
→Heat sink material will have to be machined and mounted to the CTP so that adequate cooling is provided as more GTP lanes are activated.
→Hai briefly described the goal of the two crate configuration for testing the CTP, SD and two FADC250 per VXS crate. This configuration will be described in the poster/paper for the Real Time Conference. This will be the first time for testing the Gigabit Transceivers with FADC250 boards in PP15 and PP16, and with the SD boards driving the clocks, trigger and sync signals.

23 JAN 2009
Loopback testing is underway for the initial CTP module. The heat sink material has been ordered and the material will need to be machined to fit properly on the CTP board. The heat sink will cover all three FPGA will provide adequate cooling for the Virtex5 parts when the full code is running all SerDes lanes. We cannot activate all 16 payload slots, but we can certainly test the CTP with up to 8 FADC250 modules.

ACTION ITEMS: Next meeting will be Friday 27 February 2009 → CCF226 @10am