12GeV Trigger meeting notes:

16-Nov-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga, B. Moffit, E. Jastrzembski

9-Nov-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, N. Nganga, B. Moffit

26-October-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, H. Dong, N. Nganga, B. Moffit

19-October-2012: Meeting cancelled

12-October-2012: C. Cuevas, B. Raydo, W. Gu, S. Kaneta, A. Somov, Beni Z. H. Dong, N. Nganga, B. Moffit

5-Oct-2012: Cancelled (Hall D Collaboration Meeting)

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0. Trigger/Clock/Sync – TI/TD

16-Nov-2012

-->20 TD boards have arrived, and 5 have been tested.
→20 TI boards arrived with 2 boards fully tested.
→The P0 connectors should be installed and only a few will have the P0 omitted. Check the SFI to be sure that there is full clearance for the TI with P0.
→Bryan has the updated CODA driver library for the production TI boards and removed the old driver from the site directory.
→TS testing is progressing, and there seems to be an issue with the VXS crate that has the Elma 20 slot backplane. Production boards should be ready to order by March-2013.

9-Nov-2012

→1st article boards will be delivered to customers next week. (Hall B)
→Production deliveries "should" begin next week also. Not clear how many are in a 'lot'.
→Rate register implementation would be nice and useful, but presently the rate is calculated from reading registers at a fixed interval. Counters could be implemented on board to produce a "Rate" that merely has to be read from a register.

2-Nov-2012

→Acceptance test procedure code is proceeding well.
→No news is good news and no update from CEM regarding the production board delivery schedule
→Rate measurement registers? Check to see if this is already included on the trigger boards. TS board will have this feature, and it could be added (if not already there) on the other boards.
→Sounds like requirements to me,,,,, TS 'shall' include deadtime measurement. Does this exist on the TI? Firmware exists for SSP and may be re-usable for other boards.

26-Oct-2012

→Exact delivery schedule with quantities not disclosed by CEM. The contract lists 20 weeks from acceptance date.
→William has reduced the overall latency to 490ns by adjustments to the receiver.
→Updated firmware for TI-D and TS has been released and Bryan is working on updating/creating the new CODA library.
→Pre-production boards have a slightly different pin out from the production versions. 10 TI production boards have been received, and 5 TD production boards have been received. William is distributing these production boards to the hall groups.

12 Oct-2012

→Deliveries of next batch of production boards unknown. Will receive schedule today.
→Repaired board has passed acceptance testing.
→William distributed a message regarding trigger latency measurements and there have been several discussions:

> The minimum TS to TI latency using the 62.5MHz trigger 'link' is rather long and is approximately 570ns. If the internal logic operates on a 125MHz clock this latency period can be reduced. Fiber distribution will add to this latency delay, and in the end the minimum requirement is 3.5us to be sure that timing hits are not lost for the F1TDC board.

→Changes to the TI-TD firmware is close to complete. Testing activities to begin soon after the firmware revision is ready.

1. SUB-SYSTEM PROCESSOR (SSP)

16-Nov-2012

→2 week turn for bare board, then about 1 week for assembly. 1st article production SSP will be delivered soon after the assembly is complete.
→uMegas (Saclay) folks have requested a SSP board and several other trigger board hardware for their test setup in France.
→Firmware modifications for the production boards are progressing and will be ready for the 1st article testing.

9-Nov-2012

→SSP production files have been shipped!! Several people reviewed the files and no show stoppers.
→All components have been ordered by Zentech, and an update for assembly will be delivered soon. 1st article due and 10 days for testing to approve the remaining units.

26-OCT-2012

-->Files have been updated on the M:drive for review. Only a few minor details still in flux, but folks should have a critical review. These are the production files and the goal is to have the files to Zentech by the week of 5-Nov-2012.
→Front panel and other peripheral items will be completed soon.
→Acceptance testing firmware/software procedure is in good shape and time for development while 1st article is under assembly.

12-Oct-2012

→An internal review of the fabrication data is imminent. Ben will continue to verify the new layout and set up a meeting time.
→Front panel and other peripheral work continues.

5-Oct-2012

→90% routed and the manufacturing files will be reviewed by several folks.
→Zentech has ordered the parts
→Still on schedule for sending files. 1st article due 8weeks after files and parts received.
→Acceptance testing code etc needs to be completed. Re-use of many routines from original SSP work can be used.

2. CUSTOMERS

16-Nov-2012

-->1 full duplex lane will be routed from PP17 to the CTP. This is already on the schematic, and Hai has plans to implement the PCIe from the Concurrent CPU.
→More details on the PCIe implementation will be forthcoming.

→5 fully populated crates are in F112 ready for testing. Input range switches need to be verified, including VME address switches.
→Procedure :(Three main sections below)
-"Pedestal" operation. No input cables, and raw data are produced to read back each channel offset and baseline 'noise'.
- All 16 payload boards in the crate, setup with "playback" mode test (all channels), Playback mode (partial occupancy)
- Deterministic alignment test with trigger data passed to the CTP

9-Nov-2012
→Executive decision to implement all four lanes from PP17 to CTP! It is copper traces and 16 capacitors. Transceivers "should" be available.
-->Full crate testing will be performed in F112 and Bryan has the software at the 85% level. The FADC250 boards will be arriving from UMass soon, and the full crate testing will take about an hour for each crate.

2-Nov-2012
→Intel i7 cores, generation 2 are on order. (16) These will be distributed to the hall groups for detector test setups and evaluation.
→Generation 3 boards will probably be the single board computer (ROC) of choice for the production version.
→PCIexpress is used on these ROCs from Concurrent. VITA 41.3 is supported. These lanes have been considered for the CTP and GTP and the plan is to implement these connections on the boards. Is a PCIexpress IP core needed?

26-OCT-2012
→CPU order has been evaluated and decision for initial purchase has been made. The initial purchase is for sixteen (16) units. Larger order for the Hall groups will be later in the year.

12-Oct-2012
→Full crate testing activities are imminent and FADC250 production boards will be here soon. Will need to re-use a CPU and CTP to complete the crate test.
→CPU production order is in the process of receiving evaluation models.

3. "B" Switch - Signal Distribution Module (SD)

16-Nov-2012
→3 repaired boards have been delivered and are working! 100% complete!!!
→Firmware for the SN storage and readback is about 90% complete.
→Trig_Out logic firmware is the next project to complete.
→Implementing the SD→TI link will be another firmware project to complete in the near future.

9-Nov-2012
→2 repaired boards will be delivered next week. These will need to be tested.
→Firmware will be updated to include the SN of each board.
→SN will be readout from SD through an I^2C register.
→To do: Consider solution for SD→TI link path
FPGA firmware download through I^2C
65K LUT for Trig_Out logic

2-Nov-2012
→No update on when the repaired boards will be delivered.
→Hall B SD boards are in the EEL109 locker and at least 4 delivered to the CLAS12 SVT group.

26-Oct-2012
→Open development: Firmware iterations like SD→TI link, 16 bit "Logic" unit to handle the Trig_Out signals. (65K memory LUT)
→Three production boards remain at CEM for rework/repair issues. Once these are received, they will be tested and delivered to Hall group.

12-Oct-2012
→112/115 have been tested and passed.
→Distributed 58/60 to Hall D
→3 have been sent to CEM for rework/repair

4. *System Diagrams/Fiber Optics*

16-Nov-2012
Get the PR written and submitted! (Panels and patch cables only for Hall B & Hall D)

26-Oct-2012
→Prepare PR for Hall B and D order of patch cables and patch panel hardware. Trunk lines will need to be a separate order because exact lengths are not known at this time.

12-Oct-2012
→No update. A recent walk through of Hall D shows virtually zero cable trays or equipment racks. Trunk cable order will be dependent on the accurate lengths from the trigger racks to the various detector readout racks.

5. Global Trigger & Trigger Distribution Testing

9 and 16-Nov-2012
→Scott has slides
→There are three crates in EEL109 and the Global Crate test is configured. Scott presented his latest measurements and the slides are attached.

2-Nov-2012
-->Global crate testing is progressing nicely, and the three crate setup is almost complete. All four GTP (Densishield) output cables will be routed to the TS soon.
→5Gb/s discussion
→Interface work and GUI implementation is still in development and progressing.
→Further discussions on initial global trigger functions and future requirements. Upcoming Lehman review will definitely show that the hardware has plenty of resources to handle the future requirements. Examples are expanding the simple BCAL from summing only to a cluster finding algorithm.

26-OCT-2012
-->SSP→GTP backplane interface testing is progressing @5Gb/s. 4 lane streaming mode on the backplane, and the fiber interface is full blown 4 lane @2.5Gb/s which could be extended to 3.125Gb/s for show.

12-Oct-2012
→SSP->GTP testing is going well. The next step is to integrate the GTP output (all 32 bits) to the TS-SD-TD crate. Run at full trigger rate, use adjustable delay (processing time) in GTP and then ultimately connect to the front end crate to measure FULL system latency.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)
3-June-2011
→Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!
16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

16-Nov-2012
Bids are due today!
→The latest routing file looks good and there are a few changes to the regulator/power section of the board that remain to be completed.
-->Internal fabrication file 'review' 1st week in December?!

26-OCT2012
→New CTP RFQ has been released for company bids (2-Nov-2012). The vendors have 2 weeks to deliver new quotes.
→Jeff and Hai have been busy with the routing strategies and the latest results look promising and the board is almost fully routed. Final route and close scrutiny of manufacturing files will be forthcoming.
→Automated test station procedure and firmware/software for the CTP-V2 acceptance testing is progressing nicely. Are there any other test support boards needed for this test procedure?

12-Oct-2012
→The production order for Hall D CTP was cancelled by the vendor. The new RFQ will be posted soon and there are no changes to the specification or BOM.
➔ Board routing is progressing and with the new bid process we have gained a few weeks of routing and verification time.
➔ Hai is very close to completion with the CTP automated acceptance test procedure.

28-Sept-2012
-->A week away from full time routing on the CTP. F1TDC projects will take some time, but will be finished soon.
→CTP kick off meeting is 2-Oct-2012 with the Zentech folks.
→BOM will be discussed and parts need to be ordered now so any long lead items are available by the time the boards are fabricated.
→Production acceptance test code is at 65%.
→Work by Scott was shown regarding effort at pin swapping to improve routing.

GTP and Global Crate Developments

26-Oct-2012
→Global crate testing s continues. I believe we have all the necessary hardware and stable firmware and library drivers are ready for the production TI-TD. Firmware revisions and drivers for the TS are virtually complete?
→Goal is to completely verify functional operation and performance of the front end crate (CTP), Global crate (SSP→GTP) and the trigger distribution (TS→TD). There are a number of critical and essential timing requirements with full latency of the trigger signal one of the key parameters to measure.

12-Oct-2012
→ECO list prepared for GTP final version
→Work continues with the Global crate test setup.
→2nd GTP prototype has been assembled and tested.

28-Sept-2012
Notes on Global setup and Root development.
Ethernet stack code from Hai appears to work fine and compiles with Altera device.

HAPPY THANKSGIVING!
***ACTION ITEMS*: Next meeting - Friday 30 November @10AM in F226**