12GeV Trigger meeting notes:

18 & 25 Feb 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu; A. Somov

11 Feb 2011: C. Cuevas, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta, J. Gu

14 & 21 Jan 2011: C. Cuevas, A. Somov, B. Raydo, H. Dong, B. Moffitt, J. Wilson, N. Nganga, E. Jastrzembski, S. Kaneta

17-Dec-2010: Meeting canceled

10-Dec-2010: C. Cuevas, N. Nganga, B. Raydo, E. Jastrzembski, S. Kaneta, B. Moffitt, H. Dong, A. Somov, D. Lawrence

3 -Dec-2010: C. Cuevas, N. Nganga, W. Gu, , B. Raydo, E. Jastrzembski, S. Kaneta, B. Moffitt, . D. Lawrence, H. Dong, A. Somov

Updated prototype board status table:--2 March 2011

Quantity	Description	Location	STATUS/Contact
8	**10 bit FADC250**		
	SN001 >>>>>>>>>	**F110**	**DAQ Lab**
	SN002 >>>>>>>>>	**Injector Group**	**J. Grames**
	SN003 >>>>>>>>>	**Injector Group**	**J. Grames**
	SN004 >>>>>>>>>	**EEL – 126**	**FDC test setup**
	SN005 >>>>>>>>>	**Hai's office**	**Needs repair**
	SN006 >>>>>>>>>	**F-Wing Lab**	**F117 (A. Somov)**
	SN007 >>>>>>>>>	**Hall A**	**Moller setup**
	SN008 >>>>>>>>>	**EEL – 126**	**FDC test setup**
1	**12bit FADC250**	**Indiana Univ**	**New timing algorithm firmware loaded Sent to IU for FCAL testing 12Oct2009 '64x crate and LinuX Cpu sent 24Jan10**
4	**Crate Trigger Processor**	**F-Wing F110 EEL109 EEL109 EEL109**	**Initial prototype CODA Library development Initial prototype - EEL109 Tested with SSP Received from CEM. Needs testing**
1	**Sub-System Processor**	**F-Wing(Ben)**	**Successful testing with CTP. SODIMM testing to be completed.**
4	**Signal Distribution V1 V1 V2 V2**	**F-Wing F110 EEL 109 EEL 109 EEL 109 EEL 109**	**CODA Library development Testing with initial TI prototype Assembled and testing is proceeding Assembled and testing is proceeding**

0. Trigger/Clock/Sync – TI/TD

February 2011

William presented a diagram that shows the configuration for the TI-D boards that will be used in the upcoming two crate DAq testing. One module will be operated as the TS for the two crate test. This module will use one transceiver to effectively loop back to another transceiver on this module. 50m of the MTP fiber will be used for crate #1. The second crate will have a TI-D module operated strictly in TI mode and we will plan to used the 150m MTP fiber for crate #2. We will plan to use the patch panels in this test to fully simulate a typical installation in the halls.

Nick presented jitter analysis results that showed the function of the jitter attenuation PLL circuit. The baseline resolution of the DSA70000 is about 1ps, and one of the tests that were performed used the RF generator that has a specified baseline jitter of 500fs. Using the RF source and a single high speed line driver, a baseline jitter measurement was established. Long story short, is that when the PLL is enabled the clock jitter measured at the farthest Payload port (15) is better than the source. (TI slot).

Nick has completed the changes to the 'receiving' I^2C firmware and has tested it with William's new TI-D. Nick is almost finished with the firmware that controls the SPI bus from the SD Fpga to the SiLab PLL components. All other firmware for Token Passing, BUSY Or'ing and other selections is complete and will need to be tested with a few payload boards.

Engineering changes to both the SD_Rev1 and The TI-D can begin and William reports that he has started the changes on the TI-D. PLL verification testing is the highest priority, and once that is complete, the changes to the board can be completed.

William distributed a test report for the TI-D jitter and fiber optic latency testing. We will begin to set up the two crate Daq/Trigger test stand in EEL-109 soon, so repeating the latency measurements for a 50m and 150m fiber including patch panels and patch cables can be completed before March.

January 2011

→William has completed the TI-D I^2C firmware and has distributed the specifications. Nick will modify the 'Receiving" side of the I^2C firmware so that it is compatible with William's changes. William also distributed the test results for the clock distribution jitter and the results are very good with a jitter histogram measured with the Tektronix scope at <2ps!

→Nick was successful in testing the SD board with the original TI board and established I^2C communications to the board before the holidays. There have been several modifications to the SD board, and once the I^2C firmware is fully tested and stable, Nick can proceed to measure the clock jitter with and without the PLL in the distribution chain. All other I/O will also be tested soon after.

→Schedule: The plan is still on track to prepare the TI-D files for production order before the summer. We will use the existing TI-D prototype boards for the two crate tests, but ECO modifications can begin for the schematic and board layout activities.

2. *SUB-SYSTEM PROCESSOR (SSP)*

February 2011

Ben reported that the SODIMM testing was progressing and he has run the memory module at 200MHz. Ben also presented jitter analysis and eye diagrams for the SSP backplane Gigabit transceivers that have been tested with a CTP. Initial test results are impressive and a series of parameters have been adjusted for the Xilinx transceivers to optimize the performance of the transceivers at 2.5Gb/s and at 5Gb/s. The eye diagrams and BitErrorRate (BER) testing at 2.5Gb/s are significantly better that the initial testing at 5Gb/s. Longer periods of testing will be needed to establish a BER lower than 10^-15.

11 February 2011

The SSP documentation has been updated to include a new application (solution) for interfacing up to 32 front-end readout devices from detectors that use custom ICs developed for high density central tracking apparatus. Each of the 32 Tx/Rx links can be run at 3.125 Gbps, and provides an elegant consolidated and isolated method to readout and control the high channel count custom ICs.

SODIMM memory testing to be completed.

January 2011
No test report at the last meeting, and the SODIMM memory test has taken a lower priority given Ben's other projects. We will plan to use the SSP in the two crate test this spring and it may be too early to start development of the CODA library for the SSP. It will be later in the fiscal year before the SSP can be tested with the GTP prototype module.

17-December 2010
→The SSP prototype is virtually complete with SODIMM memory testing and P0 gigabit lane testing still to be fully verified. The SSP BGA issues have been resolved and the design will be virtually unchanged for the production version.
→The SSP has been proposed as a data readout/trigger interface for up to 32 detector readout devices. The proposed idea may be a perfect solution for the Hall B central detector readout scheme and the fiber links from up to 32 custom readout devices can be connected to a single SSP. The SSP engine would manage the data reduction and local trigger algorithms for up to 32 detector readout devices, and as a payload module, the detector data will be read out through VME2eSST. Nice development and further details will emerge soon.

3. CUSTOMERS

January 2011
→Not a specific trigger module topic here, but preparation for the pre-production order for the FADC250 boards is virtually complete. The Medical Imaging group and Injector group will purchase two boards each, in addition to the 35 pre-production units.
→Small pre-production builds for the TI-D and SD boards make sense because there are several Users/Groups that will need to begin testing detectors soon after the two crate testing has been completed.

17-December 2011
→There may be a need from the Medical Imaging group to use a single FADC250 module for verification of new front end electronics designs. The use of a single board will be an interim solution until the new custom readout design is complete.

4 "B" Switch - Signal Distribution Module (SD)

18 February 2011
Jitter analysis results were presented by Nick and the jitter attenuation from the PLL on the SD definitely has a positive effect on the distribution of the clock signal received from the TI. The SPI communication is working and has been mapped internally to the SD FPGA.

The final firmware for the I^2C 'receiver' has been tested and this block of firmware will need to be implemented in each of the four CTP modules. This firmware change should work seamlessly with Bryan's library.

11 February 2011
→The new I^2C firmware that Nick completed can be given to Scott for inclusion in the CTPs. SPI control is a work in progress with a breakthrough soon. Preliminary jitter and clock distribution measurements are forthcoming.
→Engineering changes for the final SD revision can be worked on by Mark when he returns full time. For now, we have the components for at least six more SD, so we should be in good shape to make the last changes and order a pre-production lot.

January 2011
→Some redundancy here, but Nick has modified the I^2C firmware to be compatible with the changes that William created for the latest TI-D design. The new firmware will be loaded in the

SD and thoroughly tested. Bryan requests that the old SD be updated with the latest I^2C firmware. At some point the I^2C firmware can be loaded into the CTP and verified with the TI-D also.
→Initial test results for the SD have been reported, and once the communication firmware is resolved, the jitter analysis for the clock signals will be measured. Full verification of all other SD I/O will be tested also, and then work on revising the schematics and board layout can begin.

17-December 2011
→Progress continues and the two rev-1 SD boards have been updated with the latest ECO for the power supply section. Nick has set up the original SD and TI to establish the I^2C communication link, and has loaded the I^2C firmware on the new SD board. The new TI-D module uses a different I^2C address scheme which does not work with the original I^2C firmware. This will have to be resolved when William and Nick return from the holiday break.
→Hall B purchased components for eight(8) SD boards, so as soon as ALL ECO have been identified and crate testing is complete, the final revision of the SD will be ready to order.
→Nick has updated the SD documentation and the new front panel design is complete and looks nice. Significant testing remains for the thorough analysis of the PLL clock jitter attenuation function including all other SD functions using a full crate of FADC250 are on the horizon.

5. System Diagrams & Test Stand Activities

25 February 2011
Bryan reported that the 1U rack mount LinuX PC has been installed in the EEL109. This unit has plenty of speed to manage the two crate test. Will the disk speed be capable of streaming the data from two crates? (I remember this was a question from Ben)

No budgetary pricing received from fiber optic company yet. A representative from a local installation company was here a few weeks ago to get an idea of the installation project scope. Pricing estimates are due soon!

11 February 2011
We had a significant discussion about the two crate Daq/Trigger testing that will happen in a few more months once the pre-production lot of FADC250 arrive. In the meantime, we have a virtually all the other hardware needed for this test. See below:

Description	Quantity	Firmware Rev	Model#	Notes
VXS Crate	2	n/a	Wiener	EEL-109/Chris
Single Board CPU	2	Linux ?	?	Bryan/Dave?
CTP	2	?	Use latest version	Hai/Scott
SD	2	?	Use Rev1 boards	Nick
TI-D	2	?	1-TI 1-TI-D	William
SSP	1	?	Prototype	Ben
Fiber	2 -50m & 150m	n/a		EEL-109
Fiber patch	1	n/a		EEL-109
Fiber patch cables	4	n/a		EEL-109

For the DAQ/CODA software side:

Description	Quantity	Revision	Model#	Notes
GigEthernet Switch	1 multi port			EEL-109
Linux PC	1	Dell 1U	FAST	Installed by Bryan in EEL109

CODA				Bryan/Dave
CODA board libraries				Bryan/Dave

We have test equipment, pulsers, fanout modules etc so that should not be an issue.
The initial plan is use the playback mode of the FADC250 modules so that we can deterministically test the readout and trigger rates with all the payload modules running 2.5Gbps to the CTP.

There will be plenty of activities to needed for generating displays of readout rates, trigger rates, and a variety of other information needed to claim success.
The list of verification requirements (goals) are listed below:
→**Goals of the integration testing**:
-Verify clock distribution through TID-SD and measure jitter to front end boards
-Verify trigger rate and readout rate for a variety of occupancy levels.
-Verity token passing scheme
-Verify CTP operation with sixteen FADC250 @2.5Gbps
-Test playback mode feature on two crates and verify operation with SSP.
-Measure and record overall trigger latency. (Could include SSP)
-Verify full 2eSST readout from payload modules
-Verify TI-D features and use one TI-D in TS 'mode'
-Synchronization testing. Quantify number of out of sync events, clock counters etc.
-I am sure there are more milestone tests, but we can iterate the list.

January 2011
→The Hall D trigger fiber optic drawings are complete and have been sent to at least one company for price estimates. The price estimates will include installation labor and testing. Final lengths will be ***required*** before the final order is placed. Drawings for Hall B will need to be started soon.
→1st article VXS crate has been received and will be tested in the EEL109 lab. This crate will be used for the two crate daq/trigger testing. I believe we have all peripheral hardware/fiber to perform the two crate testing in the spring.

→We had a brief discussion about the software effort needed for testing and operating all of the modules needed for the two crates DAQ/Trigger test. CODA can be used to configure all the modules and will certainly be the engine to collect the data from the modules. Displays of plots for trigger rate, data readout rates and all other essential test results will be needed. There was also a discussion on what single board computers (CPU) will be used for the two crate testing and Bryan described the existing CPU that have been evaluated by the DAQ group.

17-December 2010
→Mark and Chris have revived the CD3 drawings for the trigger fiber optic infrastructure drawings. Ben and Chris met with a supplier of the fiber and patch panels and we will request a price estimate for the fiber trunk cables included the patch panels and patch cables. The drawings will be updated to reflect the cable lengths as shown in the Hall D 3D CAD model. (Tim and Chuck) This work will have to be completed for Hall B at some point before FY12.

16 July 2010 (Keep this because it needs to be implemented and tested at some point)
So this is a good place for the discussion about pedestal subtraction and trigger signals that occur close together. These topics were raised at the recent trigger workshop and it was suggested that we dedicate some time to these topics.

A) How are pedestals handled in the trigger summation scheme, and how are they handled during data extraction? (We will certainly need to develop a consistent scheme for determining pedestals and subtracting them from the raw samples).
B) When multiple triggers fire (in short succession), what is the implication for duplicate data recorded in the event stream?

Discussion points for each topic below:

A) Some form of pedestal subtraction has always been part of the firmware plan for each channel and for the summing of the signals. Ben presented a few methods for this pedestal subtraction at the workshop, and the pedestal subtraction has not been implemented on the flash board firmware. We did not implement pedestal subtraction for any of the tests using the two crates last year, so optimization of this method will need some work.

The pulse window charge value (sum of points for a given pulse) will need to have a pedestal correction. This pedestal correction will be stored in a register for each channel and the method for collecting the pedestal value will need to be determined.

Gerard uses some method (or is planning a firmware method?) so it would be a good idea to request his VHDL code and Hai can verify if it can be re-used for the FADC250.

B) Multiple triggers will occur for a given trigger 'window'. The implication of duplicate data seems to be a concern, and for triggers that are close together, some detector signals (data) will appear in both triggers. The GTP can record the number of times the global trigger equation has produced a valid trigger within the global trigger 'window'. The GTP window allows the alignment of the subsystem detectors and will be able to determine if the global trigger equation has been validated. Multiple validations are possible within the GTP 'window' and these valid trigger pulses will be sent to the TS. The TS will receive this information and will also control the separation of triggers that are driven to the front end crates. The number of valid triggers within the global trigger window can be stored as a trigger type or scaled. There is a minimum trigger signal separation requirement at the FADC250 which is approximately 70ns.

6. Crate Trigger Processor (CTP)

125-February 2011

→The two latest CTP boards have been reworked by CEM and received. One has been used with an SSP @5Gb/s. Ben shows nice plots with BER testing between SSP in PPort15 and CTP. Plots shown for transmission @5Gb/s and various receiver attribute settings.
→Scott will continue testing both of the latest units and at some point soon, all four of the CTP should be loaded with the latest firmware in preparation for the two crate DAq testing.

11-February 2011
Scott has identified a few problems with each of the new CTP and these have been sent back to CEM for part replacement. Once they return from CEM, Scott can continue his testing and prepare these units for the two crate tests.

January 2011
→Nick will produce the new I^2C firmware that is compatible with William's TI-D interface. This block of code will be instantiated into the CTP as soon as reasonable.
→Scott has started testing with one of the original CTP modules and will also test the two 'new' CTP. The 'new' CTP includes different FPGA (FX70T) but other than that, the modules are identical. Goal is to report test results by 14-February-2011.
17-December 2010
→The old I^2C firmware in the CTP is not compatible with the new I^2C revision that was implemented by William in the new TI-D. Brain has a CTP and new TI-D but will need to have

William modify his I^2C firmware so that he can complete the work needed for the CTP software library.
→The heat sink material has been machined and the front panels also. The machined panels and heat sinks will be ready for assembly by the New Year.
→One of the CTP has been assembled with a high speed grade V5FX70T FPGA and will be used to fully qualify the v2 FADC250 at 5Gbps/lane.
→Scott will work with one of the original CTP to become familiar with the design, Chipscope, and other features of the board. Scott can then begin testing the new CTP assemblies in January.
→Scott has completed the design for two switch card test boards and these have been assembled and are in use by Hai and Nick for testing their boards. The documentation for these switch card test boards has been completed by Scott.

Bryan has one of the initial prototypes CTP and will continue testing the software library with the latest TID firmware.

7. Projects for FY11 (GTP and Global Crate Developments)

25 Feb 2011
Scott explains the latest progress on the CTP and we will review the schematics, global pair map and other details soon. The GTP will use an interswitch pair for clock to take advantage of the beautiful clock signal from the SD jitter attenuating PLL. The Schematic is virtually complete, and the power distribution/analysis is almost done. The Densishield cables have been received and the Altera FPGA has been ordered.

11-February 2011
Scott continues to make progress on the schematic and will be prepared to have a review before he begins the significant work of board layout. Scott has been pre-planning the FPGA resource layout so that the routing on the board should be reasonable. The power distribution section of the design is under careful analysis also.

January 2011
→Scott has shifted to working on the CTP for a few weeks, but the effort for the GTP schematic continues to show good progress. Virtually all the integrated circuits for the GTP design have been specified.
→The interface between the GTP (front panel) and the TS (P2-rear panel) has been defined and library parts created for the GTP. We should consider purchasing the cable and connectors soon, and any other GTP components that may show a long lead time.

17-December 2010
→We dedicated a significant portion of the 10-Dec meeting to discussion of the trigger board and system schedule for the remainder of FY11 and test integration activities planned for FY12 including what I call “Pre-commissioning” activities that will need significant resources once the crates and modules are installed in the hall(s).
→The preliminary schedule was distributed and the engineers for each board development project provided feedback and adjustments were made to show the activities needed to achieve a reasonable estimate-to-completion for almost all the trigger system board designs. It is realistic to expect that the final board designs will be ready for production orders as soon as FY12 begins and possibly sooner. Budget allocations for the volume purchases of SD and TI-D for instance, may need to be moved to FY12, but the goal is to have the board design files ready for order by end of FY11.
→Alex and Chris have created schedules that show activities from the Hall D P6 schedules and there are several activities that will need to be assigned new IDs.

12-November 2010

→Large portion of the meeting was to discuss the 'integration' testing required for all of the latest revisions of the front end trigger modules. Virtually all the boards are at the first revision stage and will need to be tested with in a full crate. The FADC250 pre-production schedule is progressing well, so the SD & TID will need to be fully tested by the time we have more than 16 FADC250.

I have an integration test schedule developed and we can discuss the dateline at the meeting.

ACTION ITEMS: **Next meeting → Friday 4 March 2011 10AM in F226**