Trigger meeting notes:

10 July 2009: C. Cuevas, A. Gupta, B. Raydo, M. Taylor, H. Dong, E. Jastrzembski, J. Wilson

8 July 2009: 12GeV Trigger Workshop @ CNU

19 June 09: C. Cuevas, A. Gupta, B. Raydo, M. Taylor; E. Jastrzembski, J. Wilson

12 June 09: C. Cuevas, A. Gupta, B. Raydo, M. Taylor; A. Somov, J. Wilson

5 June 09: C. Cuevas, A. Gupta, B. Raydo, E. Jastrzembski, M. Taylor; A. Somov, J. Wilson

Updated prototype board status table:--10 July 2009

Quantity	Description	Location	STATUS
4	10bit FADC250	EEL109 SN002 SN004 SN006 SN008	4 board high trigger rate testing has been completed One of these boards has been given to Beni (FDC readout)
3	10bit FADC250	DAQ Lab SN003 Moeller SN007 Moeller SN001 Spare	2 boards reserved for August Hall A experiment 1 'spare'
1	10bit FADC250	DAQ Lab SN005	Needs repair; Clock Issues
1	12bit FADC250	EEL109	Returned to Jlab for firmware check Reserved for IU for FCAL readout
4	Trigger Interface Trigger Distribution	EEL109/DAQ Lab	Modules used for system testing
5	VME -- FP-SD Front Panel – Signal Distribution	EEL109/DAQ Lab	Complete Use in test crates
1	Crate Trigger Processor	EEL 109	Successful testing with multiple FADC250!!
1	Crate Trigger Processor	EEL 109	Successful testing with multiple FADC250 and in SSP mode!!
2	Signal Distribution	EEL109	Programmable Token passing scheme works. Enable register has been added. BUSY signals are OR'ed and enable register works. FADCTrigOut signals are OR'ed and have an enable register

0. Trigger/Clock/Sync – TI/TD

10 July 2009

No report

19 June 2009

Please see the Firmware section for updates.

12 June 2009

Several iterations of Altera firmware have produced a working Token passing and control scheme. Abhishek has firmware that implements an enable register for each payload port, and the token passing scheme was measured with four (4) FADC in the VXS crate with the Wiener backplane. The payload port map enable firmware was mapped for the Elma 20 slot backplane, but after writing the correct port enable pins, the boards were read out with 2eVME and token passing. FADC were in PP16, PP12, PP10 and PP14.

Trigger Rate: 100 KHz
128 Block Events: TI setting
30MB/s data transfer rate. (6 input signals distributed to 4 FADC modules)

1. FIRMWARE TESTING

10 July 2009
Two FADC250 modules are presently in the final phase of testing for the Hall A application with the Moeller apparatus. Two boards have been reserved for the new application and the library will need to be modified slightly to allow for the new register parameters required for the application logic.

19 June 2009
→Ed reports that the BUSY level assertion register has been added and that it functions correctly. This will allow programming of the FADC250 so that a BUSY signal will be generated at increments smaller than the full front end buffer time.
→Maximum trigger rate testing.
The discussion started with Ed explaining a few issues with the 2eSST software patch that is a 'work-around' a few issues with the Tundra 2eSST chip and large blocks of data. There are several combinations of backplane readout modes with and without token passing that have been accomplished so far. For example, the data results for the IEEE-RT conference poster were transferred with 2eSST but without token passing through the SD.

To achieve the highest trigger rate we will have to implement 2eSST, with token passing through the SD, and with the BUSY signals OR'ed through the SD to provide feedback to the Trigger Interface. To achieve the maximum trigger rate and not saturate the VME readout bandwidth, the FADC250 modules will need to be in 'pulse' mode. The maximum trigger rate and data rate testing has not been completed yet, but it sounds like all the hardware and firmware is in place. Ben has been very busy with a few other projects, but hopefully we can set this up before the trigger workshop.

12 June 2009
→Ed reported at the 5 June meeting that he will implement a register to program a BUSY assertion 'pointer'. (My definition for lack of a better term) Presently the BUSY from each FADC will almost never be asserted because the buffer size is large. For testing the BUSY it will be necessary to be able to set the point at which the BUSY is asserted.
→There has been other firmware work but it is primarily associated with the Hall A Moller application and I have placed the information under the 'customer' section.

2. *SUB-SYSTEM PROCESSOR (SSP)*

10 July 2009
No report and we briefly discussed the schedule for this project for upcoming FY10 activities. Schematic is progressing and many other details will follow in the coming months.

19 June 2009
Ben showed the progress of the SSP schematics at our Electronics Group meeting and it is impressive and the Altium tools will be put to the test for the management of the FPGA netlist. It is not clear that the Altium tools provide a seamless connection to the Xilinx design tools, especially since we are using a Xilinx library part (V5LX110) that is pin compatible with the V5FX70 that will be used on the board. One step at a time, and so far the Altium tool shows some very nice features for managing pin/gate swapping, hierarchy functions, and enhancements to the board layout methods especially for replication of sub-circuit sections.

12 June 2009
No report, but Ben has started with this design process and has figured a way to use the FPGA tools in Altium to connect the necessary signals for the Gigabit Transceivers and other important nets to what is defined as the "manual" page in the FPGA schematic design tool. The SSP is schedule for FY10, and takes 2nd priority to the 16 channel discriminator project.

3. CUSTOMERS

10 July 2009
→Notes from 19 June are still accurate with the Moeller application for the FADC250 very close to final delivery. The experiment will start mid-August, so the board will have to be delivered soon so that the module can be connected and tested in the hall.
→Beni requested two FADC250 and has one module in the EEL/126 lab. The FDC full scale prototype is being assembled and tested and they have requested at least two boards for the readout system. He has been given a FADC_FrontPanel_Control board to interface the older style VME TriggerInterface to the flash board.
→The Hall D TOF group (Florida State) is requesting a FADC250 but I need to know that their backplane has been modified to accommodate the VXS connector. –OPEN-

19 June 2009
→The firmware for the Hall A Moller system is complete and tests are progressing in the Daq Lab. Two FADC250 boards will be allocated for this experiment period; one board is a spare.
→Ben reports that the 12 bit FADC250 board has been received from the IU FCAL group. Apparently there is something wrong with a channel on the board. The last thing that was changed was an 'upgrade' to the latest firmware revision. Hai mentioned that he suspects the problem might be a timing issue between the 12 bit Maxim parts and the 10 bit Maxim parts. It is not clear how soon the IU FCAL folks need the 12 bit board returned, but it will take a few weeks to understand the problem and provide a fix.
→Chris mentioned that Paul Eugenio was seeking to use a FADC250 module and it is not clear if the IU FCAL group was willing to let Paul use it for his TOF testing. It is probably a long shot, but worth talking to both groups to see if something can be worked out. Paul has another issue with a non-VXS crate, so the 12bit FADC250 would work fine because the J0 connector is not populated.

12 June 2009
Hai reports that Ed is finished with the firmware for the Altera FPGA and is testing the new firmware with the new firmware implemented on the FX20 for the Hall A Moller experiment. There was a recent meeting with Brad S. from Hall A to discuss implementation details, and two FADC will be allocated for the duration of the Moller experiment. The experiment begins 21 August, so there is time to verify the new firmware, and install the module in its final configuration in the Hall, and test in the Hall before beam delivery.

4 "B" Switch - Signal Distribution Module (SD)

10 July 2009
Nothing new to report, but the description and instructions document has been updated to reflect the final prototype functions and circuit changes. Abhishek could certainly add scaler (counter) registers to the module, but this firmware change is not a high priority.

19 June 2009
Abhishek reported that the final changes to the control register firmware have been tested. The Token In/Out signals can be enabled via a register and this prevents signals from passing to empty payload slots. The Token bypass testing was performed in the Wiener 21 slot VXS crate, and the 'special' payload port mapping is handled by programming the SD to bypass the

required slots. The BUSY signals from each payload port are managed in the same fashion and this was also tested.

The SD document needed significant updates and the final draft is in circulation for edits. There will be a few modifications to the next revision, and Mark will handle the transfer of the SD PCAD design to Altium. The initial steps will be to include all ECOs and gather any new requirements for the SD features as we progress with other trigger modules.

12 June 2009

→Ben has included the SD module in the test stand configuration GUI and is able to program the SD modules to bypass the empty slots. The SD firmware appears to work properly and transfers the token passing signal to the FADC that are configured in the VXS crate. The 2eSST mode was not attempted (I do not recall what the reason was) but this mode will be verified soon. The BUSY and FADC_TrigOut signals have programmable mask registers and presently both of these signals are simply OR'ed in the SD Altera FPGA. The BUSY signal is transferred to the TI and SD front panel, and the FADC_TrigOut signal is driven only to the SD front panel.

→After some discussion, Ben suggests that it would be a nice feature to use the FADC_TrigOut signal in a way that the SD board could automatically configure during initialization. The CTP could also use this method too, except the CTP would have to use some special message from each FADC's serial stream during the initialization process. The TI could verify that both CTP and SD report that the same PayloadPorts are functional, and set the PayloadPort mask register to the SD and CTP. More details and explanation at the Trigger meeting.

5. System Diagrams & Test Stand Activities

10 July 2009

→This is a good place for the discussion about the workshop. The four sessions were very informative and generated plenty of questions and discussions about how each of the new modules in the trigger system function. The overall trigger and readout system were described in greater detail by Ed and Dave Abbott with the Trigger Supervisor and DAQ system as the topics. There were interesting issues regarding the compatibility of the new 'pipelined' electronics with legacy equipment that is part of the 12GeV plan for the other halls. There are many details to investigate about compatibility, and the discussion also included the need for I/O on the TI and CTP for the applications where only a few crates would be used.

Ed and Dave Abbott's presentations were very informative and they addressed the idea of running several trigger 'sessions' with the new trigger supervisor and CODA3. Without going into too much detail here, the idea is to be able to configure detector systems and establish separate trigger configurations/sessions for multiple sections of the detector.

Alex covered the requirements for Hall D, and described the needs of the global trigger processors to handle the trigger equations predicted for GlueX. He also described a proposal to use pre-described data for the front end flash FPGA so that the trigger hardware could be tested online using data that is generated in the flash FPGA which is then processed by the global trigger modules. This would be a very nice way to commission and test all of the readout crates during the initial installation period.

Elliott coordinated the final session which covered the need for handling the calibration triggers, and implementing scalers for the monitoring of dead time and other important parameters of the trigger system.

June 19 2009

Nothing new to report on system diagrams, but this is the best spot to list the discussion on the price estimates from Wiener on their 21 slot VXS backplanes. It is clear that they want us to use their "Hartman" payload port map. Hartman will design a 21 slot VXS backplane with the ELMA payload port map, but it will include significant cost for the NRE. It is clear that we want to use the ELMA map because there are several vendors that have these VXS backplanes as

stock items. The Harman backplane design includes a VME64x slot which is a nice feature but not a requirement. It was mentioned that another option would be to approach CAEN because their VME card enclosures and power supplies are almost identical to the Wiener. CAEN would have to provide a VXS 20 slot ELMA mapped backplane, but that is up to them to meet the specification.

June 12 2009
The IEEE-NPSS Real-Time conference papers have been uploaded and accepted. If you would like to browse the presentations please visit:
http://indico.ihep.ac.cn/conferenceTimeTable.py?confId=456

6. Crate Trigger Processor (CTP)

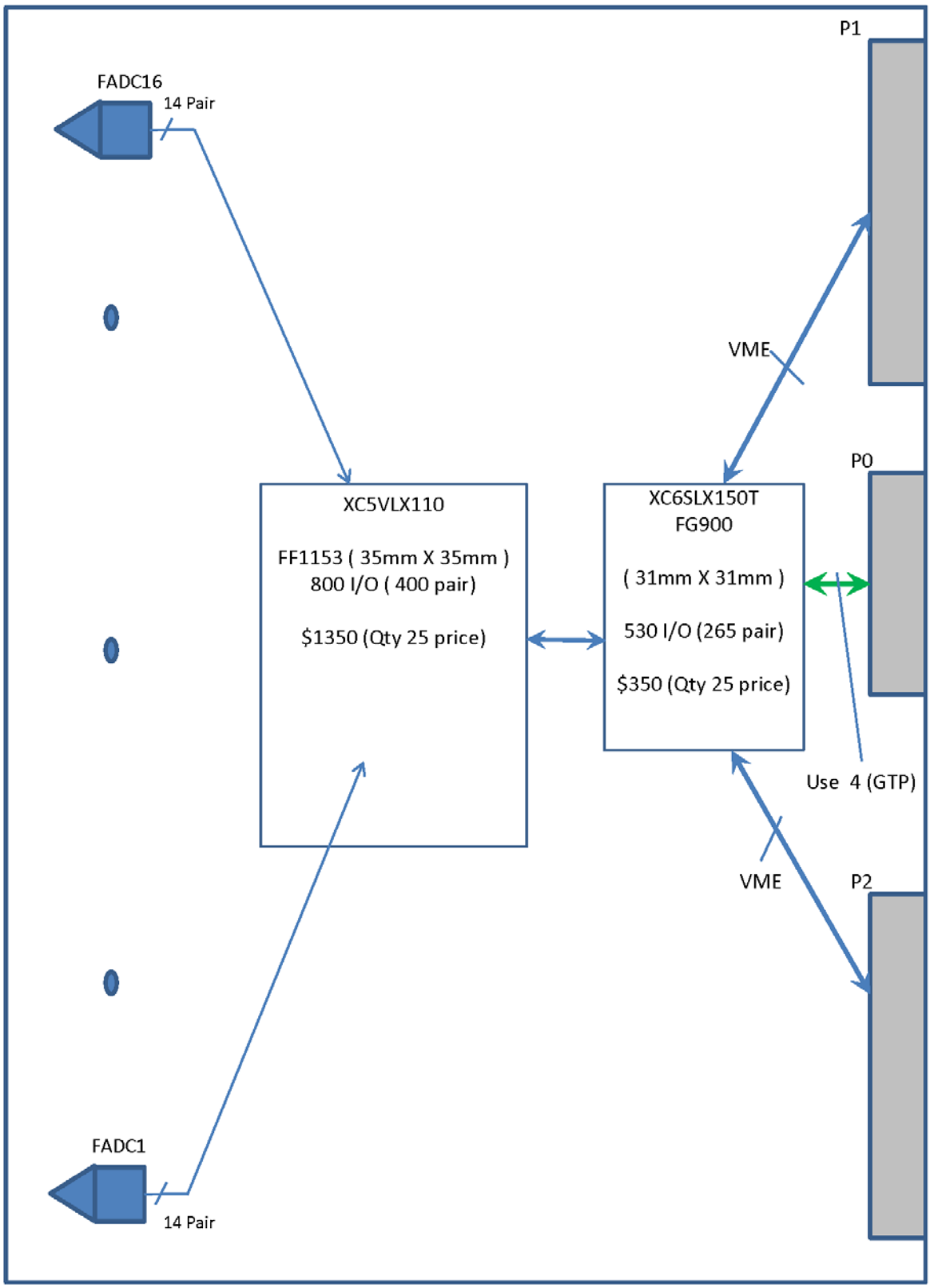
10 July 2009
CTP activities are complete.
19 June 2009
CTP is ready for the maximum trigger rate testing!

12 June 2009
Hai reports that the CTP is ready for use with one crate, four board testing plan. We will set this up using the programmable SD, with token passing, and 2eSST and record the maximum trigger rate. BUSY will need to be working and sent to the TI so that the system is stable during the test.

7. Projects for FY10
Schedules are looming and the plethora of funding distributions for BIA, 12GeV, etc, is in progress for FY10. We discussed the projects that are high priority (according to the 12GeV project schedule) and I have outlined the details in a spreadsheet calendar for FY10. Quick summary as follows:

a) FADC250 Rev-1: We briefly discussed a proposal for reducing the FPGA count. This proposal uses one FPGA to handle the ADC and one FPGA to manage the VME interface and GigBit transceivers. These selections will reduce the components needed for the design revision, and eliminate many parts. ***See figure on the following page***.
b) SSP Rev-: Ben has started this schematic. Many details to decide soon especially the pair definitions for the global trigger crate.
c) GTP Rev-: This board looks an awful lot like the CTP, but of course it is much different. Not too early to begin the selection process to optimize the best FPGA.
d) F1TDC Rev 2: Good news is that we have plenty of experience with this design, and there will be a large amount of effort to change over to Altium, and then begin the design to accommodate the requirements for Hall D. (48 channel mode, etc)

ACTION ITEMS: **Next meeting scheduled for 17 July 2009 at 10:30am in CC-F228**


P1
FADC16
14 Pair
VME
P0
XC5VLX110
FF1153 (35mm X 35mm)
800 I/O (400 pair)
$1350 (Qty 25 price)
XC6SLX150T
FG900
(31mm X 31mm)
530 I/O (265 pair)
$350 (Qty 25 price)
Use 4 (GTP)
VME
P2
FADC1
14 Pair