12GeV Trigger meeting notes:

31-Aug-2012: C. Cuevas, B. Raydo, W. Gu, J. Wilson, S. Kaneta, A. Somov

24-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, W. Gu, J. Wilson, S. Kaneta, A. Somov

17-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, W. Gu, J. Wilson, E. Jastrzembski

10-Aug-2012: C. Cuevas, B. Moffit, B. Raydo, N. Nganga, J. Wilson, H. Dong, W. Gu, S. Kaneta

3 Aug 2012: Cancelled

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0. Trigger/Clock/Sync – TI/TD

31-Aug-2012

→First shipment has been delivered. 8 are configured as TI with 7 as TD.
→Acceptance test plan will proceed as planned. A few initial problems so far.
→20 days to complete the 1st article testing and submit a report to CEM.

24-Aug-2012

→1st article shipping this week. Should receive boards week of 27-Aug.
→Acceptance test procedure not released, but William is prepared to verify the functionality of the new assemblies.
→Probably a good idea to post the test procedure so a few other folks become test 'experts'
→2nd TS prototype board has been used to test the partitioning feature. Progress is being made.

17-Aug-2012

→No news from CEM which is not bad news.
→TID or TI? What identifies the board difference?
--Front panel label:
--Firmware version is read from register
→Initial 15 units can be configured as TI or TD. The boards will require component rework at JLAB for proper TI or TD configuration.
→Production units will be assembled as TI or TD and identified with labels on the PCB.

10-Aug-2012

→CEM has made phone contact! Some change request for silkscreen.
→Delivery of 1st article boards remains the same; 22-Aug.
→Setup 1st article test stand in the DAQ lab.

1. *SUB-SYSTEM PROCESSOR (SSP)*

31-Aug-2012

→1st article delivery is based on long lead components plus PCB fabrication.
→PCB fab/assembly files are progressing but will take a few more weeks for final review.
→Hall A requested an additional SSP and the PR was submitted and approved

24-Aug-2012

→Zentech wins the award. 1st article delivery will be due after the vendor receives the fabrication files. BOM will be ordered, and schematics/Gerber will be ready for review soon.
→18 layer board! A new JLAB record.
→Board will use new fiber transceivers (QSFP)

17-Aug-2012
→Not officially awarded, but bidders have been evaluated and lowest cost selected.
→Schematics complete and will be reviewed.
→Layout is progressing well and will need careful check before sending to vendor for 1st article build.
→Firmware files have been sent to the Saclay folks and more discussions/meetings will develop for final implementation plans.

10-Aug-2012
→Production SSP boards will use new Avago Transceiver (40 GB) QSFP
→Savings of $35K!!!
→SSP has been awarded but not publicly released
→Schematic changes and board layout is progressing well
→1st article delivery will be based on when the fabrication files are ready
→Coming soon, new front panel

2. CUSTOMERS

31-Aug-2012
→The Pre-Production batch of FADC250 boards has certainly been used extensively for testing and of course for HPS and other beam tests.
→No details on the PCAL group's request and we will have to shuffle boards around because there are other essential tests that are ongoing that require a full crate of FADC250 boards.

24-Aug-2012
→No boards to the Hall B PCAL group yet, but request has not reached an urgent state.
→A quick meeting with the Hall A folks produced a request for another FADC250, and other trigger hardware for their Compton detector test station. Orders for SSP and CTP were requested also and should be added to new contract orders.

17-Aug-2012
→Same note as 10-Aug.
→Crate and other modules sent to UConn for Tagger electronics testing.
→Use a TD (production version) in the Global Trigger crate test
→2nd FADC250 pre-production board given to Brad S. (Hall C) for detector testing in EEL-126

10-Aug-2012
→PCAL group to receive at least one FADC250 and a front panel distribution board
→No news is good news, and the Hall C folks are happy for now. (Or everyone is on vacation)

3. "B" Switch - Signal Distribution Module (SD)

31-Aug-2012
Same note as 24-Aug-2012.

24-Aug-2012
→No report. Nick will return 4-Sept.

17-Aug-2012
→Delivery of production boards will be mid-September
→No issues as far as we know
→Test procedure is in good shape, and minor edits have been added the documentation.

10-Aug-2012
→Balance of the order is due in September.
→Will need to keep the FADC250s, CTP and TI together for production testing
→CTP firmware modified and tested and works with the SD automated test procedure.

4. System Diagrams/Fiber Optics

31-Aug-2012
→Fluke fiber test equipment has been delivered to Scott.
→Expect Hall C fiber to arrive in about a month
→Need to finalize the specification and quantities for trunk, patch, and patch panels, for the Hall B and Hall D order. Order in last part of 2013 first quarter. (Dec-2012)

24-Aug-2012
→PO issued to Tiger Controls for the Hall C system. Prices were slightly lower than expected. Large order for Halls D & B should bring prices even lower.
→Fluke MTP fiber test equipment has been purchased. Due in 3-weeks.

17-Aug-2012
-->PR for Hall C is written and in the system, but not sent yet. Need to verify total cost etc, with Brad S.
→Halls D & B will share the cost of the Fluke MTP fiber optic test unit. (Scott's the owner)

10-Aug-2012
-->PR needs to be submitted to purchasing by end of August.
→Still have not received pricing from vendors.

5. Two Crate DAq test configuration

31-Aug-2012
→TI communications established through I^2C to GTP
→Register map definitions created by Scott and drivers developed by Bryan

24-Aug-2012
→Time to get the hardware mounted in the rack:
--1st crate – Global – SSP (FADC250), GTP, SD, TI
--2nd TS, SD, TD
--Densi-shield cables. Use two cables for now (15 trigger bits + clock)

17-Aug-2012
→Scott continues to test the GTP using FADC250 boards as the data generators. VXS Gigabit serial links are running @5Gb/s with a few errors, but long term data is needed to increase our confidence level to operate at the higher bit rates.
→No VME backplane readout is exercised during the serial tests, and 2eSST readout should be exercised during the 5Gb/s serial data transmission testing to replicate a real system test. What should the duration of the testing?

10-Aug-2012
→16 FADC250s used as data generators to GTP @5Gb/s with some errors, but over a 48 hour period. Good news. No equalization parameter adjustments yet, but this could be tested and documented.

20-JAN-2012 (Keep this date to reference full DAq crate procedure)

3-June-2011
→***Successful testing with the two crates each with a single FADC250-V2, CTP, TI, SD and one SSP!!***

16-July-2010 (Keep this note because it needs to be implemented and tested at some point) See older note dates for the list of items.

Crate Trigger Processor (CTP)

31-Aug-2012
→1 CTP added to the PR for the Hall A group.
→Bid packages due after Labor Day.
→Placement is in progress, and then will progress to optimizing the routing file.
→Development of the CTP acceptance test program is progressing.

24-Aug-2012
→Hai is on vacation and the bid packages are due 30-Aug
→Routing and placement are progressing well. Power fan-out and plane layers going well.
→Lowest price wins!

17-Aug-2012
→RFQ is on the public site and we have started to receive questions.
→Bid packages for the thirty-two (32) production boards are due 30-Aug-2012.
→New circuit board routing is progressing
→CTP production acceptance test stand procedure and firmware is under development
→CLAS12 CTP requirements. We want to develop CTP to use all 4 'lanes' from FADC250 boards. Imagine (6.25Gb/s *4 *0.8) data rate! Many things to discuss, but the CLAS12 folks have a great deal of experiments that will require higher bandwidth and trigger functions that will exceed the Hall D CTP design.

10-Aug-2012
→Project has started. Mountain of routing work.
→Ready for RFQ, paperwork signed and delivered
→Automatic test procedure will be developed.

GTP and Global Crate Developments

31-Aug-2012
-->Consolidation of separate firmware projects is progressing.
→Register map under implementation. More definitions and driver development will occur.
→Keep progressing toward goal of the Global Crate test. Several minor details still to complete but getting closer to the goal!

24-Aug-2012
→2.5 days running @5Gb/s with 16 FADC250 boards without errors recorded.
→The serial tests are performed without VME bus activity
→Serial testing should be performed with VME bus activity
→Embedded controller on the Altera part to manage serial testing? Sidetrack,
→GTP driver development started. i.e.(I^2C control, etc)
→Final Physics equation loading? Are we going to use Playback mode?

17-Aug-2012
→Full crate testing with 16-FADC250 boards @5Gb/s from all boards. BER data will be collected for the long test durations.
→Assemble 2nd prototype GTP. Quote from Advanced Assembly in the queue.
→Densi-Shield cables on order. Delivery date?
→Keep pushing forward to get the Global Trigger system configured and tested.

10-Aug-2012

→Full crate testing with FADC250s and GTP
→Radiated fiber has been tested. See results
→GTP second board assembly quotes are coming in and some parts may be consigned

ACTION ITEMS: **Next meeting - Friday 7 September @ 10AM in F226**