Trigger meeting notes:

16 Jan 09: B. Raydo, C. Cuevas, A. Gupta, H. Dong, A. Somov, E. Jastrzembski

12 Dec 08: B. Raydo, C. Cuevas, A. Gupta, H. Dong, J. Wilson, F. Barbosa

Updated prototype board status table:--16 Jan 2009

Quantity	Description	Location	STATUS
8	**10bit FADC250**	**EEL109/DAQ Lab**	**Trigger testing**
1	**12bit FADC250**	**Indiana University**	**FCAL testing**
4	**Trigger Interface Trigger Distribution**	**EEL109/DAQ Lab**	**Trigger testing**
5	**VME -- FP-SD** **F**ront **P**ane**l** **– S**ignal **D**istribution	**EEL109/DAQ Lab**	**Complete Use in test crates**
1	**Crate Trigger Processor**	**EEL 109**	**Initial functional testing**
1	**Crate Trigger Processor**	**Send for assembly as soon as parts received**	**Send 9 Feb 2009**
2	**Signal Distribution**	**Receive from board house on 21 Jan**	**All parts ready to send to assembler**

0. Trigger/Clock/Sync – TI/TD

12 DEC 2008
No update, and Sebouh will continue this work when he returns for school.

7 NOV 2008
Sebouh has made progress on the GUI development with MSVisual C++. This GUI will be the user interface for controlling and displaying the registers from the CTP and SD modules. He has developed the I^2C communication code, and will also develop more firmware for the Atmel micro-controller that resides on the Trigger Interface (TI).

1. FIRMWARE TESTING

16 JAN 2009
No problems to report and the new readout parameters have been added to Ben's test stand data displays and records.

Hai has completed the development of the firmware download procedure that describes the method to reconfigure and download the FADC250 FPGA from VME. The discussion that followed focused on the method to verify that the new firmware download was successful. This download procedure will be refined, and the main point is that Hai has developed the code that manages the transfer of the new firmware via VME to the Xilinx Eproms.

12 DEC 2008
Ben reported that the latest firmware changes to the Trigger Interface have been tested and no problems have been noted.

2. *FADC250 Control board (SD-FP == Signal Distribution – Front Panel)*

16 JAN 2009

See prototype board status table. This board project is complete and the boards are being used in the test stand until we have the fully functional SD board.

3. CUSTOMERS

16 JAN 2009

No new progress to report. Hai has focused his time on the CTP testing.

Alex Somov had a few questions about the ability to readout raw data AND 'Q' value from each channel for every trigger event. This may be a method used during commissioning to verify the 'Q' mode function that is performed in the Fpga. Other system level trigger questions were discussed and it is clear that further discussion is needed to document/clarify overall trigger system requirements/functions.

12 DEC 2008

Hai has started researching methods to implement the function that was presented by the group at IU. The FCAL IU group has the 12 bit FADC250 module and have performed offline analysis with the data gathered from their detector setup. The Sqrt (ln(x)) function produces timing resolution of less than a nanosecond, and Hai has investigated the use of a CORDIC algorithm for use in the Fpga. Further implementation will develop.

4 "B" Switch - Signal Distribution Module (SD)

16 JAN 2009

Abhishek presented his latest Altera functional timing verification for the FPGA that will control the Clock, Trigger, Sync, Busy and Token passing signals. He has successfully synthesized the firmware, and has instantiated the block of code that was developed by Sebouh Paul that will manage the serial control interface to/from the Trigger Interface module.

The SD boards will be shipped on 21 January, and two boards will be sent to the assembly company by next week (26Jan09). The assembly process is at least a week, and then Abhishek can begin the initial test plan for the SD board. Soon after, the SD board will be used to distribute signals in a full VXS crate and plenty of other tests can be performed.

There was a discussion about how to handle "half" crates that may be installed on experiments. In a 12 slot VXS crate, the payload slot that would normally have the Trigger Interface module does not exist.(PP18) This means that the SD and CTP would have to receive the global clock/sync/trigger signals from a front panel module. For Hall D, I believe we have specified full 20 slot VXS crates for all the detector readout systems, so this should not be an issue.

In cases where a VXS "half" crate is used, the CTP will have to receive the common signals (CLK,Trigger,Sync) from the front panel. This detail will have to be discussed further and implemented on the final board design.

12 DEC 2008

Abhishek presented his analysis on the latest SD layout using the HyperLynx BoardSim application. There were a few questions regarding his results, and the analysis was performed to verify the layer stack(impedance) and to gain experience with the HyperLynx tool for board layout verification.

Mark and Abhishek have corrected and reviewed all the details of the SD board layout and the board has been ordered(19Dec08). We ordered 3 modules and two will be sent off site to be

fully assembled by the week of 19Jan09. Work has started on the final assembly kit, and the initial test plan document has been drafted. We will need to design front panels for these prototype boards soon, so that we are prepared to test these boards as soon as they are received from the assembler.

5. System Diagrams & Test Stand Activities

16 JAN 2009

As a quick review, the following tests have been completed with the FADC250 boards, TI/TD, and front panel signal distribution boards:

- ✓ Test LX25 with high rate trigger pulse train on all inputs simultaneously
- ✓ "System" clock jitter with fiber distribution and existing front panel signal distribution boards. These tests will need to be repeated once the SD module is ready.
- ✓ Signal to Noise Ratio (SNR) Plenty of test data, and the results so far will establish the baseline SNR value. These tests should be performed with multiple channels per board, and with multiple boards transferring VME data and with all the Gigabit links active to measure differences from the baseline results. VME data transfers are not dual edge yet, but testing SNR with higher the higher bus rates will be important
- ✓ 10 bit FADC250 charge mode Vs 12 bit charge integrating ADC(LeCroy 1182) Ben presented the initial results from the test, and further details will be presented at the Hall D collaboration meeting.

GUI and data display software will continue to be developed by Ben for the upcoming CTP and SD test stand activities.

- Real Time Conference 2009 – Beijing, China 10-15 May, 2009
  Dave Abbott proposed that abstracts be created for submission and that the 12GeV trigger system offers an abundant source of topics to present at the conference. The overall Trigger/DAQ system could be the main presentation, and the poster sessions could present details of new results from the CTP and SD crate tests. Abstract submission deadline is 20Feb2009

12 DEC 2008

The bias circuitry for the LVPECL clock receivers has been modified on all boards for the front panel receivers only. The receiver circuits that interface to the SD (VXS P0) will need to be modified for all boards so that the proper termination and Pecl biasing is applied.

The test stand activities are a work in progress and there continues to be a good deal of work to measure and record the test results. Ben has refined several tests for the boards in the system, and has very nice results for the tests listed in the notes from 21 Nov 2008.

These test documents will be stored on the M:drive for reference. M:\FE\12GevTrigger\Trigger_Teststand

6. Crate Trigger Processor (CTP)

16 JAN 2009

Functional testing with the first module is going well. A heat sink will be added to cover the three large Fpga on the module. Hai will follow his test plan for the initial functional testing and then begin the testing with multiple FADC250 modules in a crate. Discussions about how to use the CTP output data were presented, and since we will not have a SSP module for awhile, we could implement the testing of the CTP fiber optic output data stream with a Xilinx evaluation board. We may not be able to fully implement the 4 lanes of fiber optic data, but the final CTP sum data can be tested.

12 DEC 2008

The power section tests for the initial module passed and the results have been recorded on Hai's test document. Clock circuitry was populated also on this power section test board, and since no problems were identified, the entire assembly kit was sent to the assembler. The fully assembled CTP will be at JLAB on 5 Jan 2009.

The initial test document for the CTP has been drafted and there are numerous tests to perform before establishing the gigabit links with the FADC250 payload modules.

ACTION ITEMS: Next meeting will be 23 January 2009 → CCF228 @10am